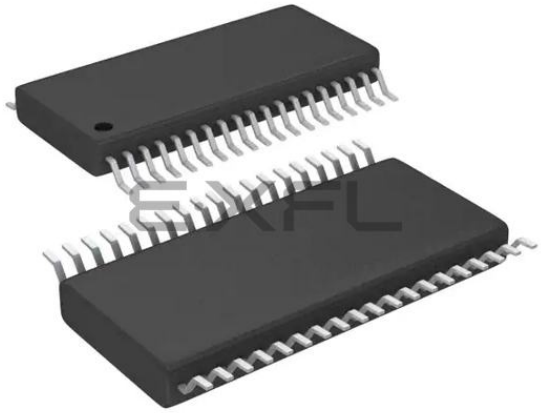

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc8664fribefxuma1

3.2.1 Memory Protection Strategy

The XC866 memory protection strategy includes:

- Read-out protection: The Flash Memory can be enabled for read-out protection and ROM memory is always protected.
- Program and erase protection: The Flash memory in all devices can be enabled for program and erase protection.

Flash memory protection is available in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

Table 4 Flash Protection Modes

Mode	0	1
Activation	Program a valid password via BSL mode 6	
Selection	MSB of password = 0	MSB of password = 1
P-Flash contents can be read by	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
P-Flash program and erase	Not possible	Not possible
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash or D-Flash
D-Flash program	Possible	Not possible
D-Flash erase	Possible, on the condition that bit DFLASHEN in register MISC_CON is set to 1 prior to each erase operation	Not possible

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. A password match triggers an automatic erase of the read-protected Flash contents, see **Table 5** and **Table 6**, and the programmed password is erased. The Flash protection is then disabled upon the next reset.

For XC866-2FR and XC866-4FR devices:

The selection of protection type is summarized in **Table 5**.

Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$B1_H$	**P3_ALTSEL1** **Reset: 00_H** P3 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 3										
80_H	**P0_OD** **Reset: 00_H** P0 Open Drain Control Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_OD** **Reset: 00_H** P1 Open Drain Control Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$B0_H$	**P3_OD** **Reset: 00_H** P3 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 11 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$D1_H$	**ADC_PAGE** **Reset: 00_H** Page Register for ADC	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, Page 0										
CA_H	**ADC_GLOBCTR** **Reset: 30_H** Global Control Register	Bit Field	ANON	DW	CTC		0			
		Type	rw	rw	rw		r			
CB_H	**ADC_GLOBSTR** **Reset: 00_H** Global Status Register	Bit Field	0		CHNR			0	SAMPLE	BUSY
		Type	r		rh			r	rh	rh
CC_H	**ADC_PRAR** **Reset: 00_H** Priority and Arbitration Register	Bit Field	ASEN1	ASEN0	0	ARBM	CSM1	PRIO1	CSM0	PRIO0
		Type	rw	rw	r	rw	rw	rw	rw	rw
CD_H	**ADC_LCBR** **Reset: $B7_H$** Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE_H	**ADC_INPCR0** **Reset: 00_H** Input Class Register 0	Bit Field	STC							
		Type	rw							
CF_H	**ADC_ETRCR** **Reset: 00_H** External Trigger Control Register	Bit Field	SYNEN1	SYNEN0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, Page 1										
CA_H	**ADC_CHCTR0** **Reset: 00_H** Channel Control Register 0	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CB_H	**ADC_CHCTR1** **Reset: 00_H** Channel Control Register 1	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CC_H	**ADC_CHCTR2** **Reset: 00_H** Channel Control Register 2	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CD_H	**ADC_CHCTR3** **Reset: 00_H** Channel Control Register 3	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CE_H	**ADC_CHCTR4** **Reset: 00_H** Channel Control Register 4	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CF_H	**ADC_CHCTR5** **Reset: 00_H** Channel Control Register 5	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
$D2_H$	**ADC_CHCTR6** **Reset: 00_H** Channel Control Register 6	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
$D3_H$	**ADC_CHCTR7** **Reset: 00_H** Channel Control Register 7	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
RMAP = 0, Page 2										

Table 13 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FF_H	**CCU6_TRPCTRH** **Reset: 00_H** Trap Control Register High	Bit Field	TRPPEN	TRPEN13	TRPEN					
		Type	rw	rw	rw					
RMAP = 0, Page 3										
$9A_H$	**CCU6_MCMOUTL** **Reset: 00_H** Multi-Channel Mode Output Register Low	Bit Field	0	R	MCMP					
		Type	r	rh	rh					
$9B_H$	**CCU6_MCMOUTH** **Reset: 00_H** Multi-Channel Mode Output Register High	Bit Field	0		CURH			EXPH		
		Type	r		rh			rh		
$9C_H$	**CCU6_ISL** **Reset: 00_H** Capture/Compare Interrupt Status Register Low	Bit Field	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9D_H$	**CCU6_ISH** **Reset: 00_H** Capture/Compare Interrupt Status Register High	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9E_H$	**CCU6_PISEL0L** **Reset: 00_H** Port Input Select Register 0 Low	Bit Field	ISTRP		ISCC62		ISCC61		ISCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_PISEL0H** **Reset: 00_H** Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2		ISPOS1		ISPOS0	
		Type	rw		rw		rw		rw	
$A4_H$	**CCU6_PISEL2** **Reset: 00_H** Port Input Select Register 2	Bit Field	0						IST13HR	
		Type	r						rw	
FA_H	**CCU6_T12L** **Reset: 00_H** Timer T12 Counter Register Low	Bit Field	T12CVL							
		Type	rwh							
FB_H	**CCU6_T12H** **Reset: 00_H** Timer T12 Counter Register High	Bit Field	T12CVH							
		Type	rwh							
FC_H	**CCU6_T13L** **Reset: 00_H** Timer T13 Counter Register Low	Bit Field	T13CVL							
		Type	rwh							
FD_H	**CCU6_T13H** **Reset: 00_H** Timer T13 Counter Register High	Bit Field	T13CVH							
		Type	rwh							
FE_H	**CCU6_CMPSTATL** **Reset: 00_H** Compare State Register Low	Bit Field	0	CC63ST	CCPOS2	CCPOS1	CCPOS0	CC62ST	CC61ST	CC60ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH** **Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A9_H$	**SSC_PISEL** **Reset: 00_H** Port Input Select Register	Bit Field	0					CIS	SIS	MIS
		Type	r					rw	rw	rw
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low *Programming Mode*	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
	Operating Mode	Bit Field	0				BC			
		Type	r				rh			

3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC866 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to **Figure 17** give a general overview of the interrupt sources and illustrates the request and control flags.

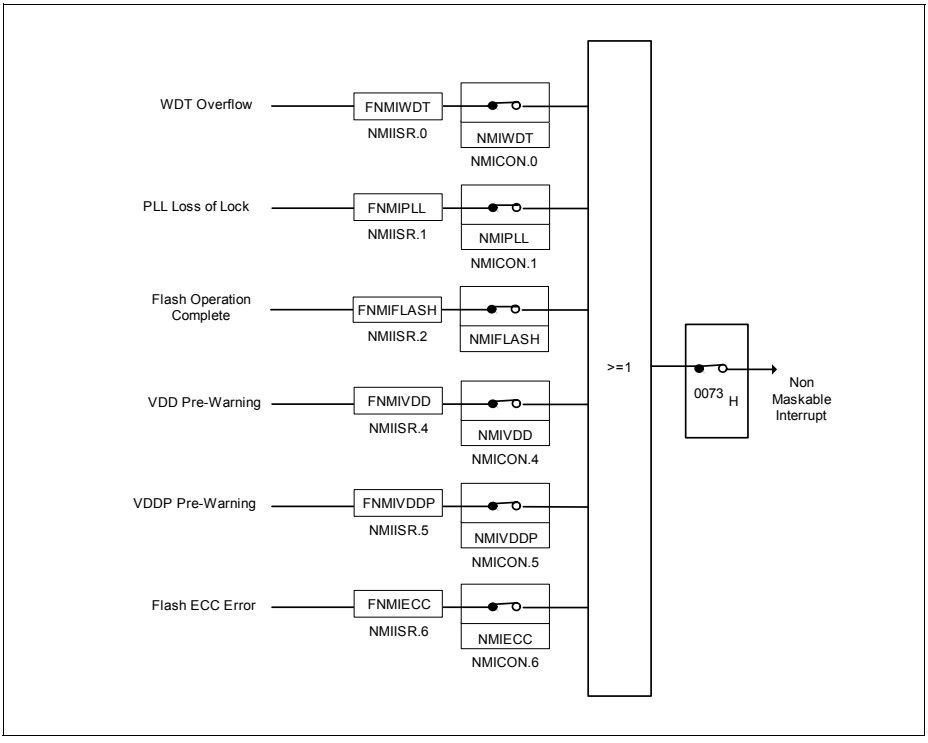


Figure 13 Non-Maskable Interrupt Request Sources

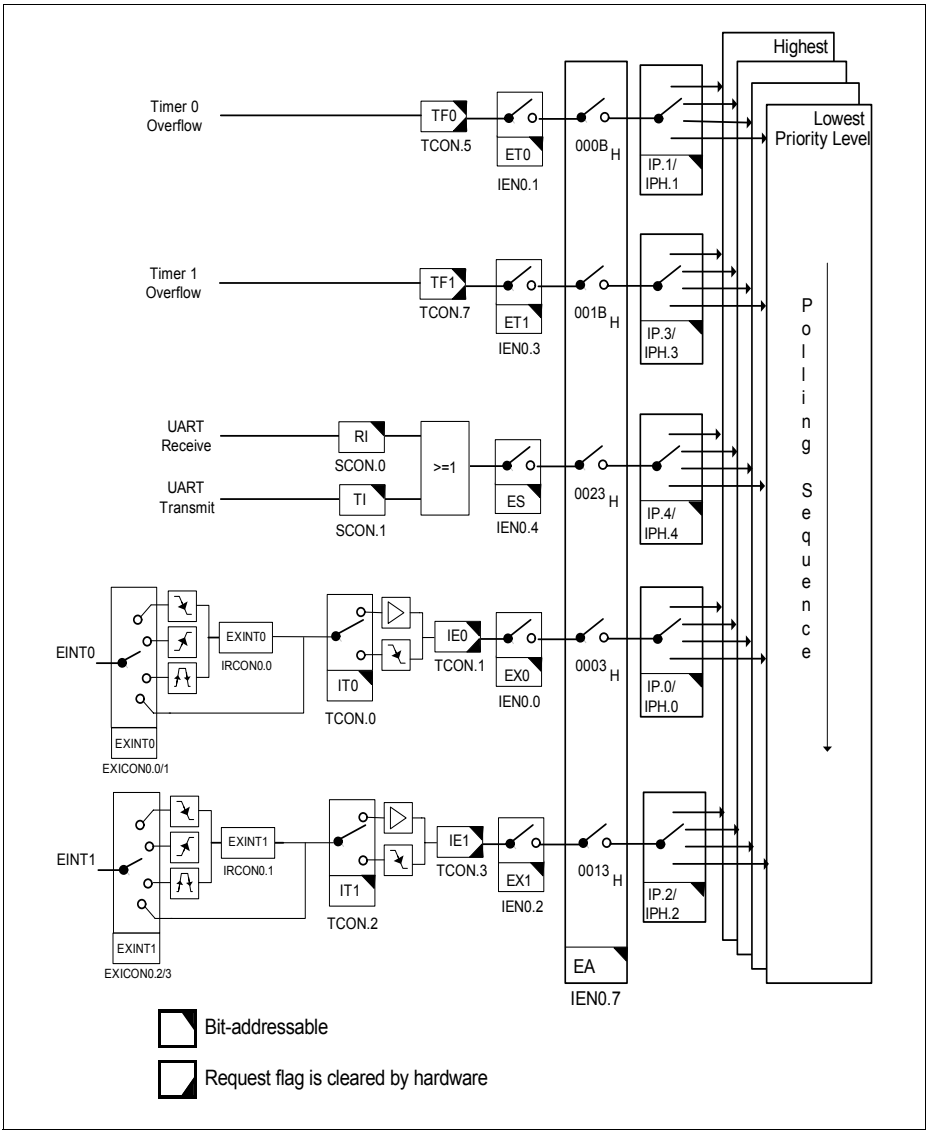


Figure 14 Interrupt Request Sources (Part 1)

3.4.2 Interrupt Source and Vector

Each interrupt source has an associated interrupt vector address. This vector is accessed to service the corresponding interrupt source request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC866 interrupt sources to the interrupt vector addresses and the corresponding interrupt source enable bits are summarized in **Table 17**.

Table 17 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC866	Enable Bit	SFR
NMI	0073_H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003_H	External Interrupt 0	EX0	IEN0
XINTR1	$000B_H$	Timer 0	ET0	
XINTR2	0013_H	External Interrupt 1	EX1	
XINTR3	$001B_H$	Timer 1	ET1	
XINTR4	0023_H	UART	ES	
XINTR5	$002B_H$	T2	ET2	
		Fractional Divider (Normal Divider Overflow)		
		LIN		

The clock system provides three ways to generate the system clock:

PLL Base Mode

The system clock is derived from the VCO base (free running) frequency clock divided by the K factor.

$$f_{SYS} = f_{VCObase} \times \frac{1}{K}$$

Prescaler Mode (VCO Bypass Operation)

In VCO bypass operation, the system clock is derived from the oscillator clock, divided by the P and K factors.

$$f_{SYS} = f_{OSC} \times \frac{1}{P \times K}$$

PLL Mode

The system clock is derived from the oscillator clock, multiplied by the N factor, and divided by the P and K factors. Both VCO bypass and PLL bypass must be inactive for this PLL mode. The PLL mode is used during normal system operation. .

$$f_{SYS} = f_{OSC} \times \frac{N}{P \times K}$$

Table 3-1 shows the settings of bits OSCDISC and VCOBYP for different clock mode selection.

Table 3-1 Clock Mode Selection

OSCDISC	VCOBYP	Clock Working Modes
0	0	PLL Mode
0	1	Prescaler Mode
1	0	PLL Base Mode
1	1	PLL Base Mode

Note: When oscillator clock is disconnected from PLL, the clock mode is PLL Base mode regardless of the setting of VCOBYP bit.

System Frequency Selection

For the XC866, the values of P and K are fixed to “1” and “2”, respectively. In order to obtain the required system frequency, f_{sys}, the value of N can be selected by bit NDIV for different oscillator inputs. **Table 21** provides examples on how f_{sys} = 80 MHz can be obtained for the different oscillator sources.

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 26.7 MHz
- CCU6 clock: FCLK = 26.7 MHz
- Other peripherals: PCLK = 26.7 MHz
- Flash Interface clock: CCLK3 = 80 MHz and CCLK = 26.7 MHz

In addition, different clock frequency can output to pin CLKOUT(P0.0). The clock output frequency can further be divided by 2 using toggle latch (bit TLEN is set to 1), the resulting output frequency has 50% duty cycle. **Figure 25** shows the clock distribution of the XC866.

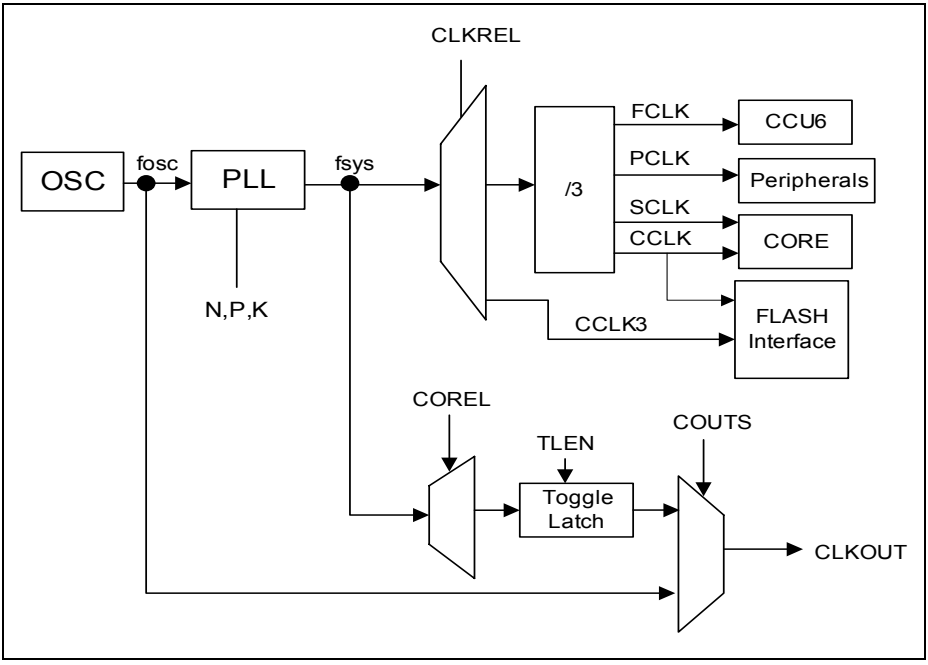


Figure 25 Clock Generation from f_{sys}

3.9 Power Saving Modes

The power saving modes of the XC866 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 26**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

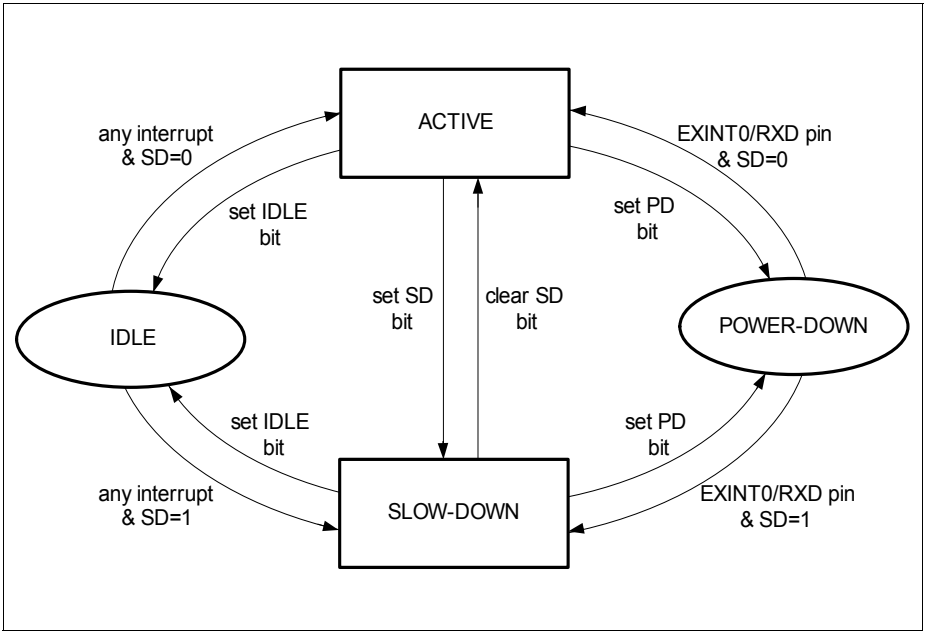


Figure 26 Transition between Power Saving Modes

3.11.1 Baud-Rate Generator

The baud-rate generator is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 29**.

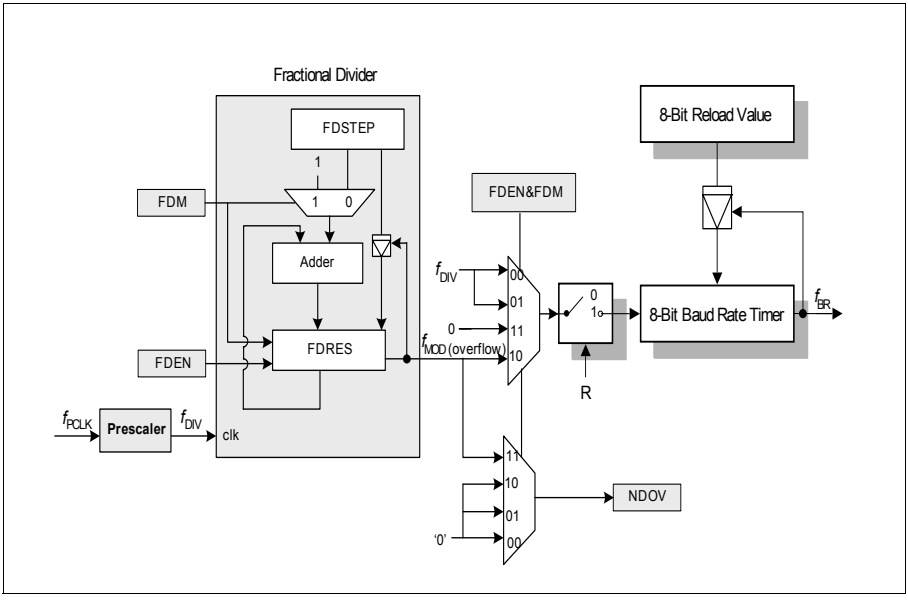


Figure 29 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.12**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)

3.11.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

[3.1]

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)}$$

3.12 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 29**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV}, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

[3.2]

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP}$$

For module clock f_{ADC} = 26.7 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 30**.

Table 30 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
26.7 MHz	00_B	÷ 2	13.3 MHz (N.A)
	01_B	÷ 3	8.9 MHz
	10_B	÷ 4	6.7 MHz
	11_B (default)	÷ 32	833.3 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 26.7 MHz. During slow-down mode where f_{ADC} may be reduced to 13.3 MHz, 6.7 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.18.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

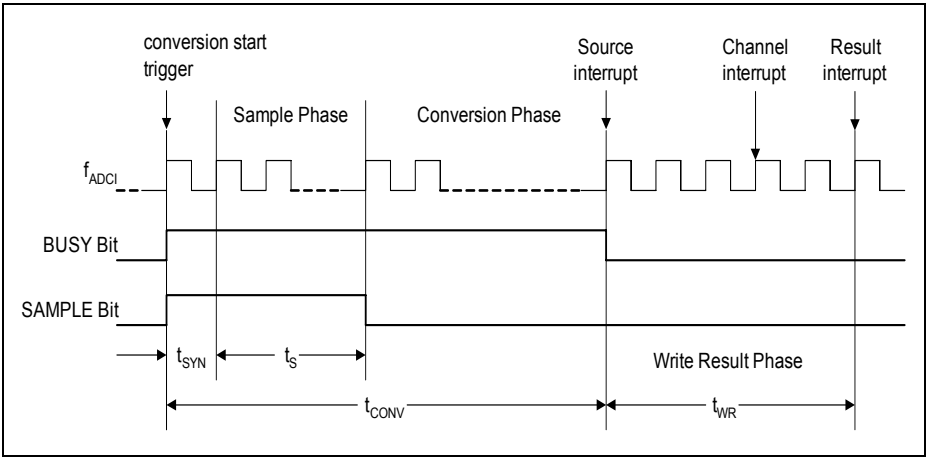


Figure 34 ADC Conversion Timing

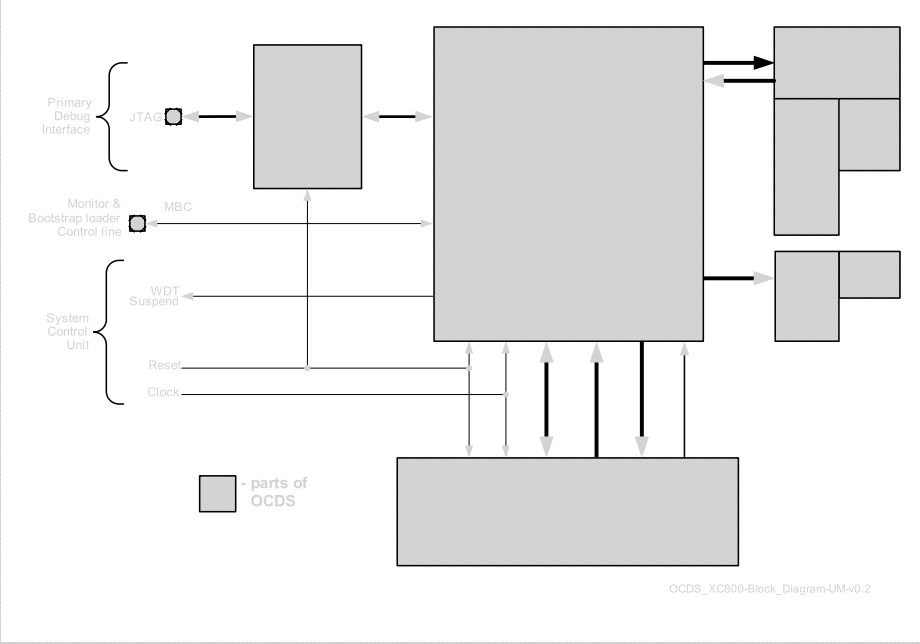


Figure 35 OCDS Block Diagram

3.19.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC866 devices are given in **Table 31**.

Table 31 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC866L-4FR	1010 0083_H
	XC866-4FR	100F 5083_H
	XC866L-2FR	1010 2083_H
	XC866-2FR	1010 1083_H
	XC866L-1FR	1013 8083_H
	XC866-1FR	1013 8083_H

Table 34 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions Remarks
			min.	max.		
V_{DDP} = 3.3V Range						
Output low voltage	V_{OL}	CC	–	1.0	V	I_{OL} = 8 mA
			–	0.4	V	I_{OL} = 2.5 mA
Output high voltage	V_{OH}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -8 mA
			V_{DDP} - 0.4	–	V	I_{OH} = -2.5 mA
Input low voltage on port pins (all except P0.0 & P0.1)	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on P0.0 & P0.1	V_{ILP0}	SR	-0.2	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on $\overline{\text{RESET}}$ pin	V_{ILR}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on TMS pin	V_{ILT}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins (all except P0.0 & P0.1)	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on P0.0 & P0.1	V_{IHP0}	SR	0.7 × V_{DDP}	V_{DDP}	V	CMOS Mode
Input high voltage on $\overline{\text{RESET}}$ pin	V_{IHR}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on TMS pin	V_{IHT}	SR	0.75 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1] on Port pins	HYS	CC	0.03 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis[1] on XTAL1	$HYSX$	CC	0.07 × V_{DDC}	–	V	
Input low voltage at XTAL1	V_{ILX}	SR	V_{SS} - 0.5	0.3 × V_{DDC}	V	
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when VDDP is powered off.

Table 38 Power Down Current (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Condition Remarks
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Power-Down Mode[3]	I_{PDP}	1	10	µA	T_A = + 25 °C.[4]
		-	30	µA	T_A = + 85 °C, XC866-4FR, XC866-2FR [4][5]
		-	35	µA	T_A = + 85 °C, XC866-1FR, ROM device[4][5]

1) The typical I_{PDP} values are measured at V_{DDP} = 5.0 V.

2) The maximum I_{PDP} values are measured at V_{DDP} = 5.5 V.

3) I_{PDP} (power-down mode) has a maximum value of 200 µA at T_A = + 125 °C.

4) I_{PDP} (power-down mode) is measured with: $\overline{\text{RESET}}$ = V_{DDP}, V_{AGND}= V_{SS}, RXD/INT0 = V_{DDP}; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subject to production test, verified by design/characterization.

4.3 AC Parameters

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 38**, **Figure 39** and **Figure 40**.

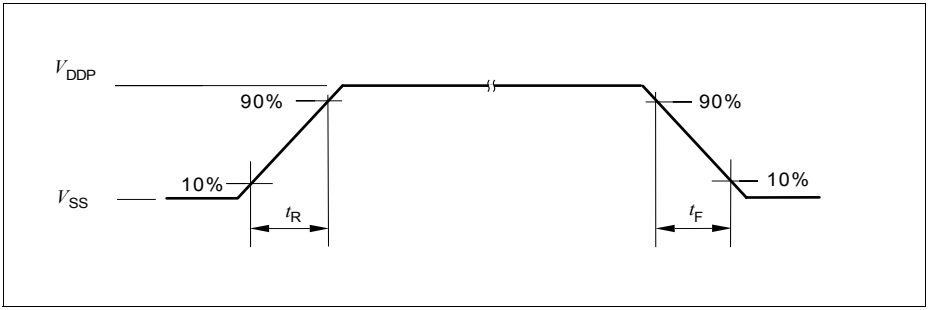


Figure 38 Rise/Fall Time Parameters

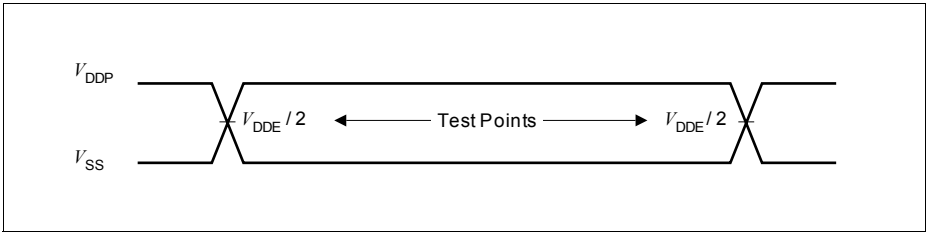


Figure 39 Testing Waveform, Output Delay

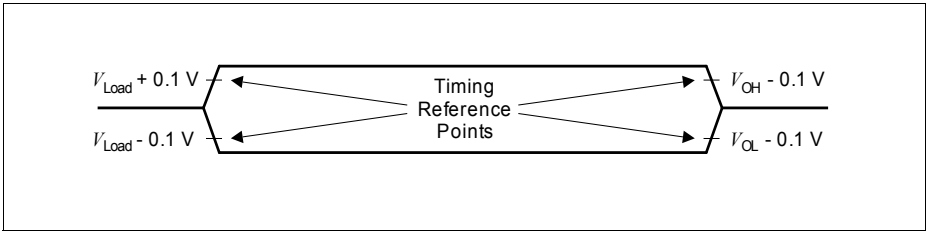


Figure 40 Testing Waveform, Output High Impedance

4.3.2 Output Rise/Fall Times

Table 41 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
V_{DDP} = 5V Range					
Rise/fall times [1] [2]	t_R, t_F	–	10	ns	20 pF. [3]
V_{DDP} = 3.3V Range					
Rise/fall times [1] [2]	t_R, t_F	–	10	ns	20 pF. [4]

1) Rise/Fall time measurements are taken with 10% - 90% of the pad supply.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.125 ns/pF.

4) Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.225 ns/pF.

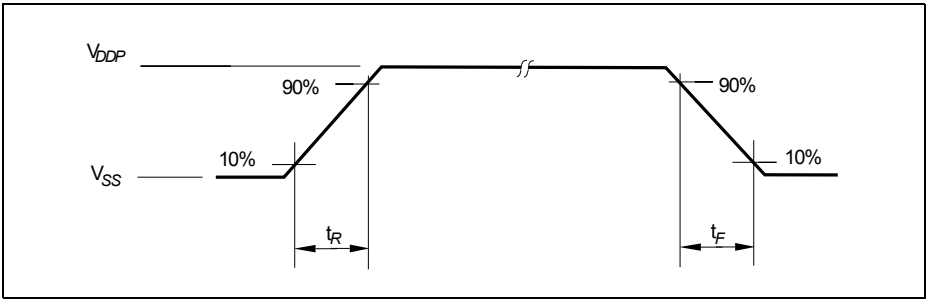


Figure 41 Rise/Fall Times Parameters

4.3.4 On-Chip Oscillator Characteristics

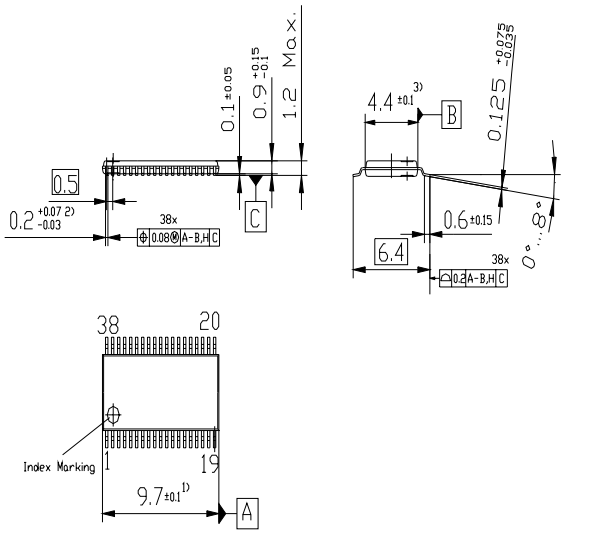
Table 43 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Nominal frequency	f_{NOM} CC	9.75	10	10.25	MHz	under nominal conditions[1] after IFX-backend trimming
Long term frequency deviation[2]	Δf_{LT} CC	-5.0	–	5.0	%	with respect to f_{NOM}, over lifetime and temperature (–10°C to 125°C), for one device after trimming
		-6.0	–	0	%	with respect to f_{NOM}, over lifetime and temperature (–40°C to -10°C), for one device after trimming
Short term frequency deviation	Δf_{ST} CC	-1.0	–	1.0	%	with respect to f_{NOM}, within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

5.2 Package Outline



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

2) DOES NOT INCLUDE DAMBAR PROTRUSION OF 0.08 MAX. PER SIDE

3) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.25 MAX. PER SIDE

Figure 46 PG-TSSOP-38-4 Package Outline