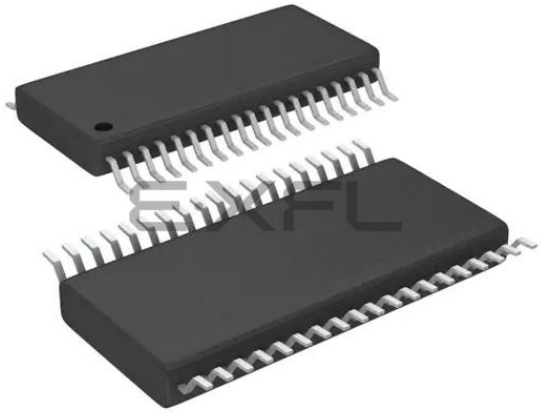

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	XC800
Core Size	8-Bit
Speed	86MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc866l4fribekxuma1

XC866

8-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number	Type	Reset State	Function
P3		I		**Port 3** Port 3 is a bidirectional general purpose I/O port. It can be used as alternate functions for the CCU6.
P3.0	32		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0
P3.1	33		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0
P3.2	34		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 CC61_0 Input/Output of Capture/Compare channel 1
P3.3	35		Hi-Z	COUT61_0 Output of Capture/Compare channel 1
P3.4	36		Hi-Z	CC62_0 Input/Output of Capture/Compare channel 2
P3.5	37		Hi-Z	COUT62_0 Output of Capture/Compare channel 2
P3.6	30		PD	$\overline{\text{CTRAP\_0}}$ CCU6 Trap Input
P3.7	31		Hi-Z	EXINT4 External Interrupt Input 4 COUT63_0 Output of Capture/Compare channel 3

Table 5 Flash Protection Type for XC866-2FR and XC866-4FR devices

PASSWORD	Type of Protection	Flash Banks to Erase when Unprotected
$1XXXXXXX_B$	Flash Protection Mode 1	All Banks
$0XXXXXXX_B$	Flash Protection Mode 0	P-Flash Bank

For XC866-1FR device and ROM devices:

The selection of protection type is summarized in **Table 6**.

Table 6 Flash Protection Type for XC866-1FR device and ROM devices

PASSWORD	Type of Protection (Applicable to the whole Flash)	Sectors to Erase when Unprotected	Comments
$1XXXXXXX_B$	Read/Program/Erase	All Sectors	Compatible to Protection mode 1
$00001XXX_B$	Erase	Sector 0	
$00010XXX_B$	Erase	Sector 0 and 1	
$00011XXX_B$	Erase	Sector 0 to 2	
$00100XXX_B$	Erase	Sector 0 to 3	
$00101XXX_B$	Erase	Sector 0 to 4	
$00110XXX_B$	Erase	Sector 0 to 5	
$00111XXX_B$	Erase	Sector 0 to 6	
$01000XXX_B$	Erase	Sector 0 to 7	
$01001XXX_B$	Erase	Sector 0 to 8	
$01010XXX_B$	Erase	All Sectors	
Others	Erase	None	

Although no protection scheme can be considered infallible, the XC866 memory protection strategy provides a very high level of protection for a general purpose microcontroller.

In order to access a register located in a page different from the actual one, the current page must be left. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and finally, the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or
- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

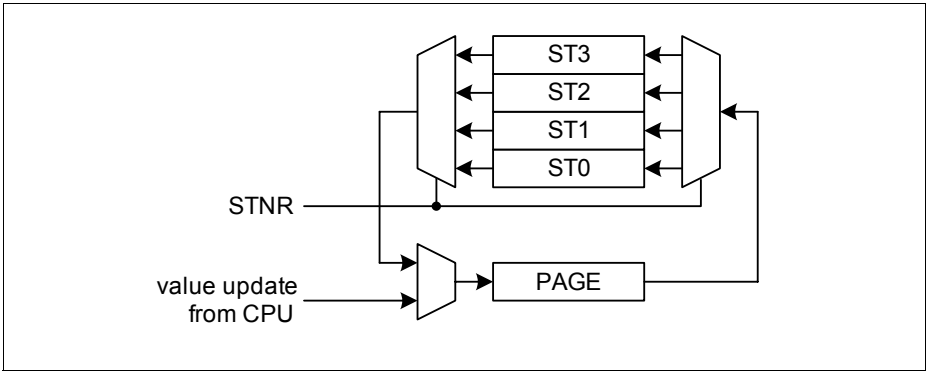


Figure 10 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC866 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register for PORT	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rwh		
RMAP = 0, Page 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rwh	rwh	rwh	rwh	rwh	rwh
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rwh	rwh	rwh	r			rwh	rwh
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$A0_H$	**P2_DATA** **Reset: 00_H** P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$A1_H$	**P2_DIR** **Reset: 00_H** P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 1										
80_H	**P0_PUDSEL** **Reset: FF_H** P0 Pull-Up/Pull-Down Select Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
86_H	**P0_PUDEN** **Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_PUDSEL** **Reset: FF_H** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
91_H	**P1_PUDEN** **Reset: FF_H** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$A0_H$	**P2_PUDSEL** **Reset: FF_H** P2 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_PUDEN** **Reset: 00_H** P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_PUDSEL** **Reset: BF_H** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_PUDEN** **Reset: 40_H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, Page 2										
80_H	**P0_ALTSEL0** **Reset: 00_H** P0 Alternate Select 0 Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
86_H	**P0_ALTSEL1** **Reset: 00_H** P0 Alternate Select 1 Register	Bit Field	0		P5	P4	P3	P2	P1	P0
		Type	r		rw	rw	rw	rw	rw	rw
90_H	**P1_ALTSEL0** **Reset: 00_H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
91_H	**P1_ALTSEL1** **Reset: 00_H** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	0			P1	P0
		Type	rw	rw	rw	r			rw	rw
$B0_H$	**P3_ALTSEL0** **Reset: 00_H** P3 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CA_H	**ADC_RESR0L** **Reset: 00_H** Result Register 0 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB_H	**ADC_RESR0H** **Reset: 00_H** Result Register 0 High	Bit Field	RESULT[9:2]							
		Type	rh							
CC_H	**ADC_RESR1L** **Reset: 00_H** Result Register 1 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD_H	**ADC_RESR1H** **Reset: 00_H** Result Register 1 High	Bit Field	RESULT[9:2]							
		Type	rh							
CE_H	**ADC_RESR2L** **Reset: 00_H** Result Register 2 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF_H	**ADC_RESR2H** **Reset: 00_H** Result Register 2 High	Bit Field	RESULT[9:2]							
		Type	rh							
$D2_H$	**ADC_RESR3L** **Reset: 00_H** Result Register 3 Low	Bit Field	RESULT[1:0]		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
$D3_H$	**ADC_RESR3H** **Reset: 00_H** Result Register 3 High	Bit Field	RESULT[9:2]							
		Type	rh							
RMAP = 0, Page 3										
CA_H	**ADC_RESRA0L** **Reset: 00_H** Result Register 0, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB_H	**ADC_RESRA0H** **Reset: 00_H** Result Register 0, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
CC_H	**ADC_RESRA1L** **Reset: 00_H** Result Register 1, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD_H	**ADC_RESRA1H** **Reset: 00_H** Result Register 1, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
CE_H	**ADC_RESRA2L** **Reset: 00_H** Result Register 2, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF_H	**ADC_RESRA2H** **Reset: 00_H** Result Register 2, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
$D2_H$	**ADC_RESRA3L** **Reset: 00_H** Result Register 3, View A Low	Bit Field	RESULT[2:0]			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
$D3_H$	**ADC_RESRA3H** **Reset: 00_H** Result Register 3, View A High	Bit Field	RESULT[10:3]							
		Type	rh							
RMAP = 0, Page 4										
CA_H	**ADC_RCR0** **Reset: 00_H** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CB_H	**ADC_RCR1** **Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2** **Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3** **Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR** **Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, Page 5										

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width[1] of 32-byte for D-Flash and 32-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time: 3 × t_{CCLK} = 112.5 ns[2]
- Program time: 209440 / f_{SYS} = 2.6 ms[3]
- Erase time: 8175360 / f_{SYS} = 102 ms[3]

1) P-Flash: 32-byte wordline can only be programmed once, i.e., one gate disturb allowed.
D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) f_{sys} = 80 MHz ± 7.5% (f_{CCLK} = 26.7 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

3) f_{sys} = 80 MHz ± 7.5% is the only frequency range for Flash programming and erasing. f_{sysmin} is used for obtaining the worst case timing.

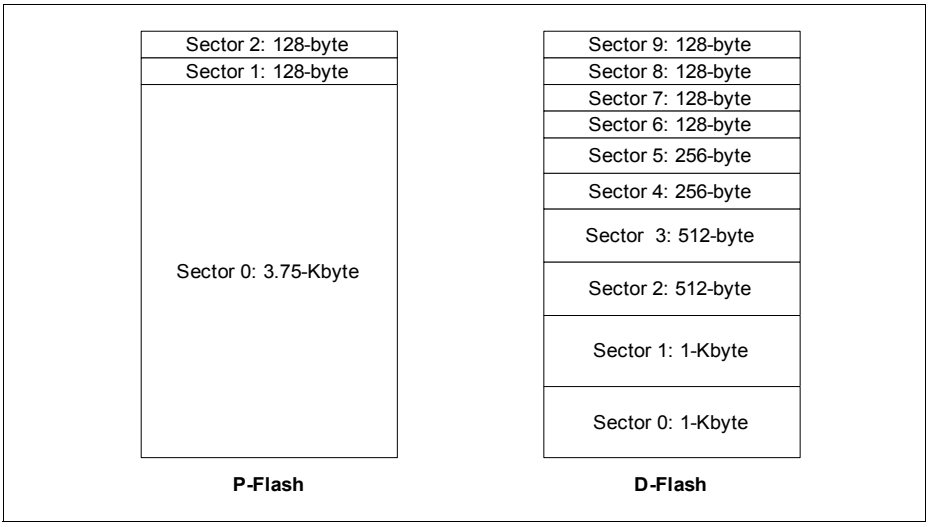


Figure 11 Flash Bank Sectorization

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

3.7.1 Module Reset Behavior

Table 19 shows how the functions of the XC866 are affected by the various reset types. A "■" means that this function is reset to its default state.

Table 19 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core	■	■	■	■	■
Peripherals	■	■	■	■	■
On-Chip Static RAM	Not affected, reliable	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
Oscillator, PLL	■	Not affected	■	■	■
Port Pins	■	■	■	■	■
EVR	The voltage regulator is switched on	Not affected	■	■	■
FLASH	■	■	■	■	■
NMI	Disabled	Disabled	■	■	■

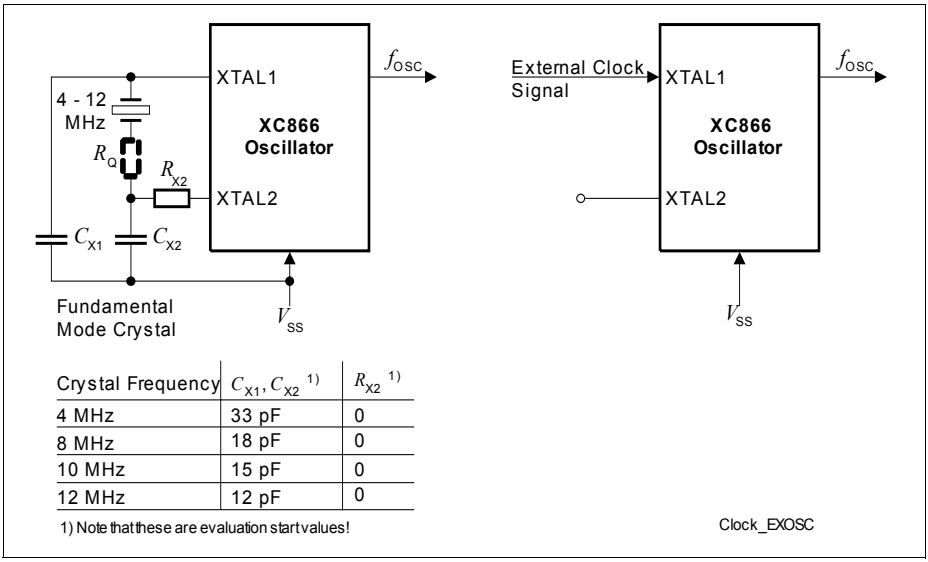
3.7.2 Booting Scheme

When the XC866 is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. Table 20 shows the available boot options in the XC866.

Table 20 XC866 Boot Selection

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	x	User Mode; on-chip OSC/PLL non-bypassed	0000_H
0	0	x	BSL Mode; on-chip OSC/PLL non-bypassed	0000_H
0	1	0	OCDS Mode[1]; on-chip OSC/PLL non-bypassed	0000_H
1	1	0	Standalone User (JTAG) Mode[2]; on-chip OSC/PLL non-bypassed (normal)	0000_H

1) The OCDS mode is not accessible if Flash is protected.
2) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.



Crystal Frequency	C_{X1}, C_{X2} 1)	R_{X2} 1)
4 MHz	33 pF	0
8 MHz	18 pF	0
10 MHz	15 pF	0
12 MHz	12 pF	0

1) Note that these are evaluation start values!

Figure 24 External Oscillator Circuitries

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC866 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC866 will be aborted in a user-specified time period. In debug mode, the WDT is suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features:

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 27** shows the block diagram of the WDT unit.

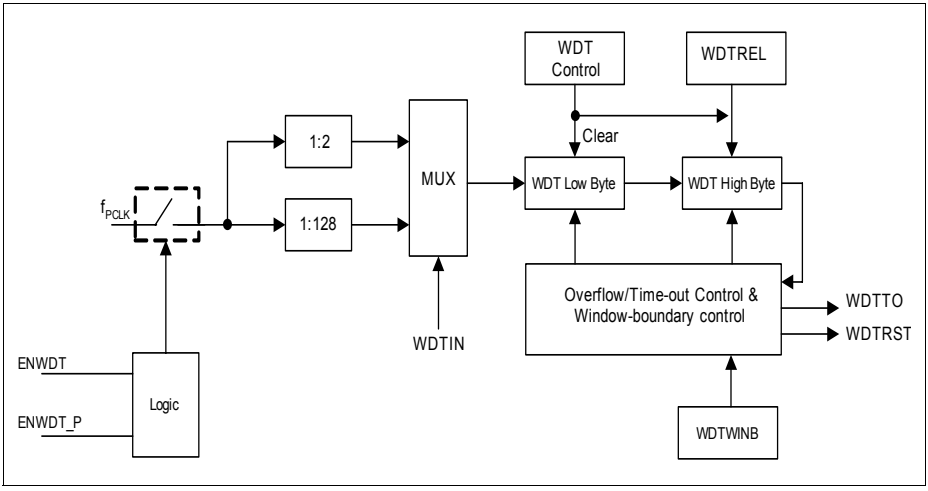


Figure 27 WDT Block Diagram

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert WDTTO) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2^8). The time period for an overflow of the WDT is programmable in two ways:

- the input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- the reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT}, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 28**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB should not be smaller than WDTREL.

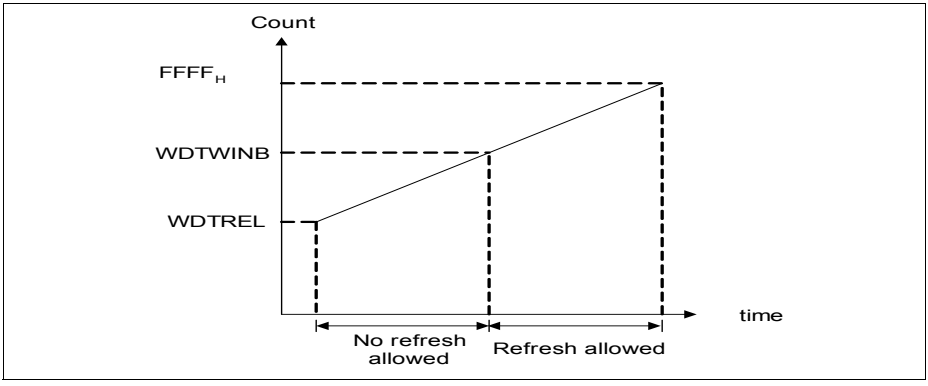


Figure 28 WDT Timing Diagram

3.11 Universal Asynchronous Receiver/Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) provides a full-duplex asynchronous receiver/transmitter, i.e., it can transmit and receive simultaneously. It is also receive-buffered, i.e., it can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features:

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART can operate in the four modes as shown in **Table 25**. Data is transmitted on TXD and received on RXD.

Table 25 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$
Mode 3: 9-bit shift UART	Variable

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. The variable baud rate is set by either the underflow rate on the dedicated baud-rate generator, or by the overflow rate on Timer 1.

- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

The following formulas calculate the final baud rate without and with the fractional divider respectively:

$$\text{baud rate} = \frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR\_VALUE + 1)} \quad \text{where} \quad 2^{BRPRE} \times (BR\_VALUE + 1) > 1$$

$$\text{baud rate} = \frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR\_VALUE + 1)} \times \frac{STEP}{256}$$

The maximum baud rate that can be generated is limited to $f_{PCLK}/32$. Hence, for a module clock of 26.7 MHz, the maximum achievable baud rate is 0.83 MBaud.

Standard LIN protocal can support a maximum baud rate of 20kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20kHz to 115.2kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

Table 26 lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 26.7 MHz is used.

Table 26 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2^{BRPRE})	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000_B)	87 (57_H)	-0.22 %
9600 Baud	1 (BRPRE=000_B)	174 (AE_H)	-0.22 %
4800 Baud	2 (BRPRE=001_B)	174 (AE_H)	-0.22 %
2400 Baud	4 (BRPRE=010_B)	174 (AE_H)	-0.22 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 27** lists the resulting deviation errors from generating a baud rate of

3.18.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

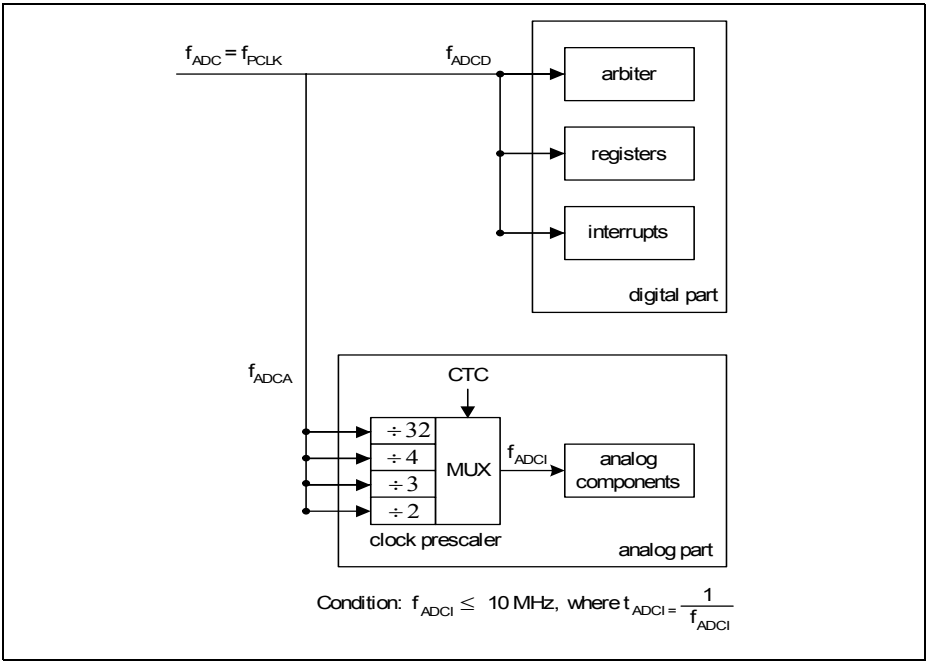


Figure 33 ADC Clocking Scheme

3.19 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- use the built-in debug functionality of the XC800 Core
- add a minimum of hardware overhead
- provide support for most of the operations by a Monitor Program
- use standard interfaces to communicate with the Host (a Debugger)

Features:

- Set breakpoints on instruction address and within a specified address range
- Set breakpoints on internal RAM address
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks
- Step through the program code

The OCDS functional blocks are shown in **Figure 35**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals. After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack). The OCDS system is accessed through the JTAG[1)], which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC866 has been started in OCDS mode.

1) The pins of the JTAG port can be assigned to either Port 0 (primary) or Ports 1 and 2 (secondary). User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when VDDP is powered off.

4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 36 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol	Limit Values			Unit	Test Conditions/ Remarks
		min.	typ .	max.		
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1	V_{DDP}	V_{DDP} + 0.05	V	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	V_{SS}	V_{AREF} - 1	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}	–	20	40	MHz	module clock
	f_{ADCI}	–	–	10	MHz	internal analog clock See **Figure 33**
Sample time	t_S CC	(2 + INPCR0.STC) × t_{ADCI}			µs	
Conversion time	t_C CC	See **Section 4.2.3.1**			µs	
Total unadjusted error	TUE[1] CC	–	–	±1	LSB	8-bit conversion.[2]
		–	–	±2	LSB	10-bit conversion.
Differential Nonlinearity	DNL CC	–	±1	–	LSB	10-bit conversion[2]
Integral Nonlinearity	INL CC	–	±1	–	LSB	10-bit conversion[2]
Offset	OFF CC	–	±1	–	LSB	10-bit conversion[2]
Gain	GAIN CC	–	±1	–	LSB	10-bit conversion[2]
Switched capacitance at the reference voltage input	C_{AREFSW} CC	–	10	20	pF	[2][3]

4.2.4 Power Supply Current

Table 37 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Condition Remarks
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	22.6	24.5	mA	[3]
Idle Mode	I_{DDP}	17.2	19.7	mA	XC866-4FR, XC866-2FR [4]
		12.5	14	mA	XC866-1FR, ROM device[4]
Active Mode with slow-down enabled	I_{DDP}	7.2	8.2	mA	XC866-4FR, XC866-2FR [5]
		5.6	7.5	mA	XC866-1FR, ROM device[5]
Idle Mode with slow-down enabled	I_{DDP}	7.1	8	mA	XC866-4FR, XC866-2FR [6]
		5.1	7.2	mA	XC866-1FR, ROM device[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 26.7 MHz(set by on-chip oscillator of 10 MHz and NDIV in PLL_CON to 0010_B), $\overline{RESET}$ = V_{DDP}, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 26.7 MHz, $\overline{RESET}$ = V_{DDP} , no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 833 KHz by setting CLKREL in CMCON to 0101_B, $\overline{RESET}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 833 KHz by setting CLKREL in CMCON to 0101_B, $\overline{RESET}$ = V_{DDP}, no load on ports.

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