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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	768
Total RAM Bits	-
Number of I/O	81
Number of Gates	30000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl030v2-qng132

2 – IGLOO DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 •   **Absolute Maximum Ratings**

Symbol	Parameter	Limits[1]	Units
VCC	DC core supply voltage	−0.3 to 1.65	V
VJTAG	JTAG DC voltage	−0.3 to 3.75	V
VPUMP	Programming voltage	−0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	−0.3 to 1.65	V
VCCI and VMV [2]	DC I/O buffer supply voltage	−0.3 to 3.75	V
VI	I/O input voltage	−0.3 V to 3.6 V (when I/O hot insertion mode is enabled) −0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage Temperature	−65 to +150	°C
T_J [3]	Junction Temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
3. *For flash programming and retention, maximum limits refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC®3* and *ProASIC3E* FPGA fabric user guides for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.
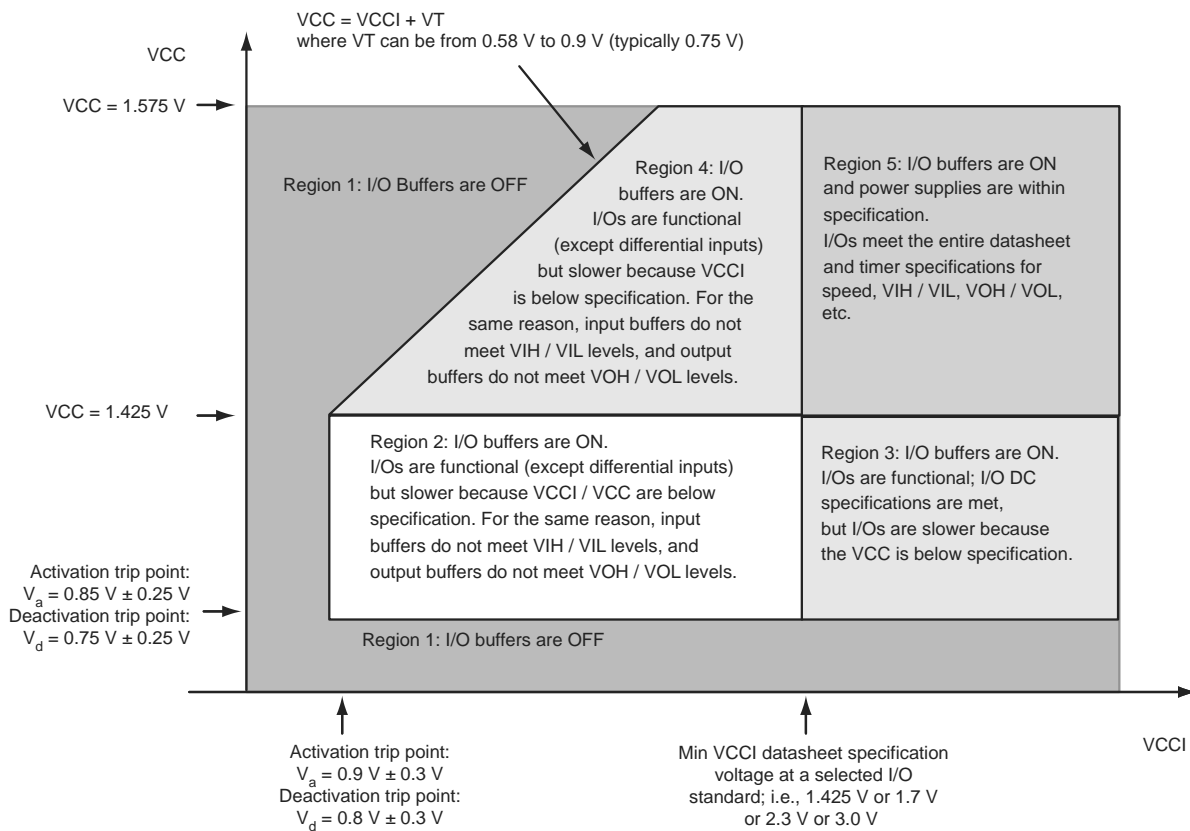

Figure 2-1 • **V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

Table 2-179 • **AGL600 Global Resource**
      Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t$_{RCKL}$	Input Low Delay for Global Clock	1.48	1.82	ns
t$_{RCKH}$	Input High Delay for Global Clock	1.52	1.94	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-180 • **AGL1000 Global Resource**
      Commercial-Case Conditions: T$_J$ = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t$_{RCKL}$	Input Low Delay for Global Clock	1.55	1.89	ns
t$_{RCKH}$	Input High Delay for Global Clock	1.60	2.02	ns
t$_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
t$_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t$_{RCKSW}$	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

FG144	
Pin Number	**AGL250 Function**
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL400 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL400 Function
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

FG256		FG256		FG256	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
H3	GFB1/IO146PPB3	K9	GND	M15	GDC1/IO77UDB1
H4	VCOMPLF	K10	GND	M16	IO75NDB1
H5	GFC0/IO147NPB3	K11	VCC	N1	IO140NDB3
H6	VCC	K12	VCCIB1	N2	IO138PPB3
H7	GND	K13	IO71NPB1	N3	GEC1/IO137PPB3
H8	GND	K14	IO74RSB1	N4	IO131RSB2
H9	GND	K15	IO72NPB1	N5	GNDQ
H10	GND	K16	IO70NDB1	N6	GEA2/IO134RSB2
H11	VCC	L1	IO142NDB3	N7	IO117RSB2
H12	GCC0/IO67NPB1	L2	IO141NPB3	N8	IO111RSB2
H13	GCB1/IO68PPB1	L3	IO125RSB2	N9	IO99RSB2
H14	GCA0/IO69NPB1	L4	IO139RSB3	N10	IO94RSB2
H15	NC	L5	VCCIB3	N11	IO87RSB2
H16	GCB0/IO68NPB1	L6	GND	N12	GNDQ
J1	GFA2/IO144PPB3	L7	VCC	N13	IO93RSB2
J2	GFA1/IO145PDB3	L8	VCC	N14	VJTAG
J3	VCCPLF	L9	VCC	N15	GDC0/IO77VDB1
J4	IO143NDB3	L10	VCC	N16	GDA1/IO79UDB1
J5	GFB2/IO143PDB3	L11	GND	P1	GEB1/IO136PDB3
J6	VCC	L12	VCCIB1	P2	GEB0/IO136NDB3
J7	GND	L13	GDB0/IO78VPB1	P3	VMV2
J8	GND	L14	IO76VDB1	P4	IO129RSB2
J9	GND	L15	IO76UDB1	P5	IO128RSB2
J10	GND	L16	IO75PDB1	P6	IO122RSB2
J11	VCC	M1	IO140PDB3	P7	IO115RSB2
J12	GCB2/IO71PPB1	M2	IO130RSB2	P8	IO110RSB2
J13	GCA1/IO69PPB1	M3	IO138NPB3	P9	IO98RSB2
J14	GCC2/IO72PPB1	M4	GEC0/IO137NPB3	P10	IO95RSB2
J15	NC	M5	VMV3	P11	IO88RSB2
J16	GCA2/IO70PDB1	M6	VCCIB2	P12	IO84RSB2
K1	GFC2/IO142PDB3	M7	VCCIB2	P13	TCK
K2	IO144NPB3	M8	IO108RSB2	P14	VPUMP
K3	IO141PPB3	M9	IO101RSB2	P15	TRST
K4	IO120RSB2	M10	VCCIB2	P16	GDA0/IO79VDB1
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO135PDB3
K6	VCC	M12	VMV2	R2	GEA0/IO135NDB3
K7	GND	M13	IO83RSB2	R3	IO127RSB2
K8	GND	M14	GDB1/IO78UPB1	R4	GEC2/IO132RSB2

FG484	
Pin Number	**AGL400 Function**
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

FG484	
Pin Number	**AGL400 Function**
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO154VDB3
F5	IO155VDB3
F6	IO11RSB0
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO45RSB0
F15	GBC0/IO54RSB0
F16	IO48RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	NC
G2	NC
G3	NC
G4	IO151VDB3

FG484	
Pin Number	**AGL400 Function**
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3