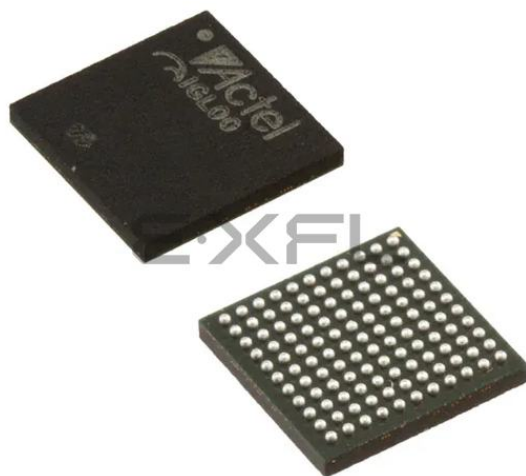




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-CSP (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v2-cs121

1 – IGLOO Device Family Overview

General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO devices enables entering and exiting an ultra-low power mode that consumes as little as 5 μ W while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low power consumption (from 12 μ W) while the IGLOO device is completely functional in the system. This allows the IGLOO device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is Instant On. IGLOO is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL015 and AGL030 devices have no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

M1 IGLOO devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low power consumption and speed when implemented in an M1 IGLOO device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Microsemi for use in M1 IGLOO FPGAs.

The ARM-enabled devices have ordering numbers that begin with M1AGL and do not support AES decryption.

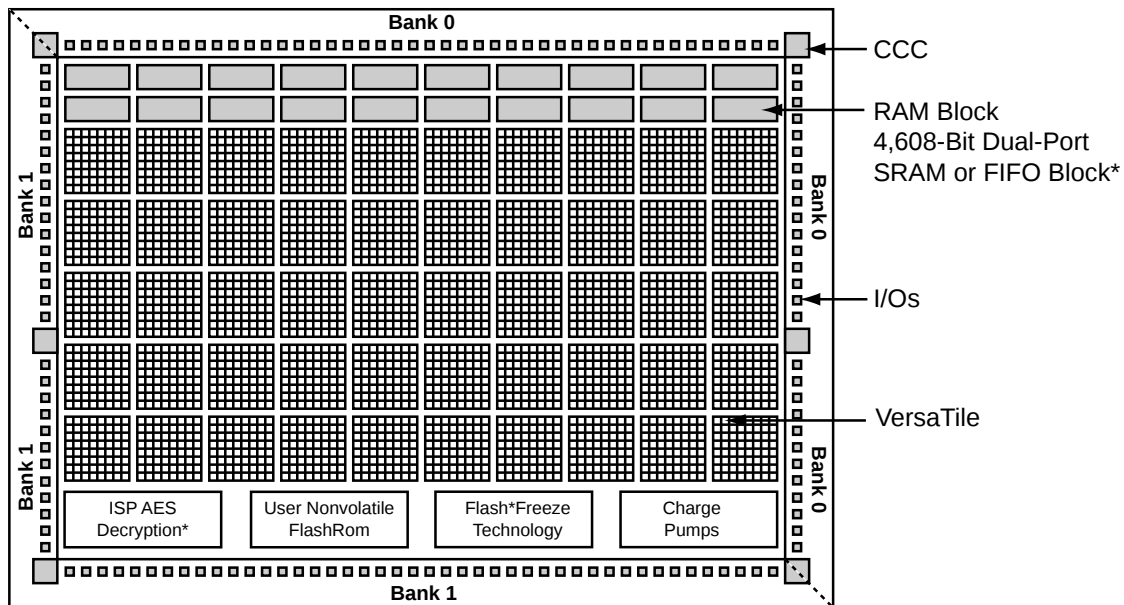
Flash*Freeze Technology

The IGLOO device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low power Flash*Freeze mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOO devices the best fit for portable electronics.

VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.



Note: *Not supported by AGL015 and AGL030 devices

Figure 1-1 • IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)

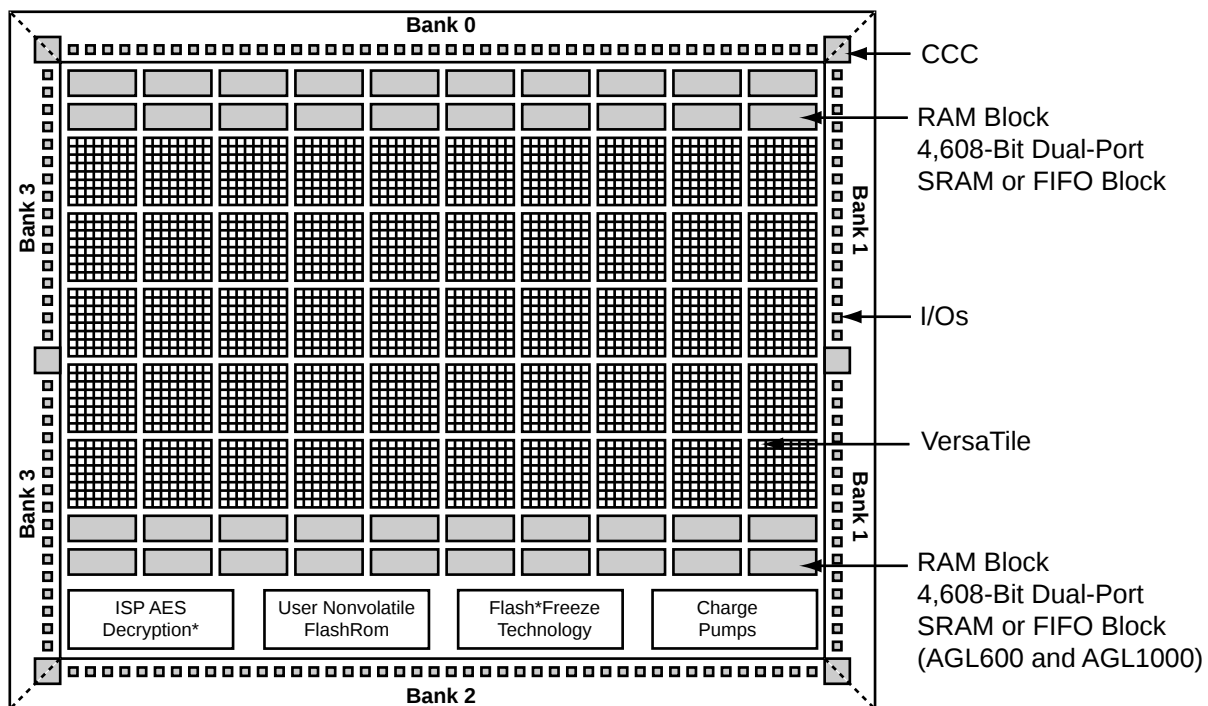


Figure 1-2 • IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% $\pm$ 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% $\times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μ s (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps $\times$ 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • I/O Standards Supported

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west banks of AGL250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of AGL250 and larger devices All banks of AGL060 and AGL125K	✓	✓	Not supported
Standard	All banks of AGL015 and AGL030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note: $IDD = N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode¹

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
ICCA Current²										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	μA
	1.5 V	14	16	20	28	44	66	82	137	μA
ICCI or IJTAG Current³										
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} \times ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VPUMP, and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

Power Consumption of Various Internal Resources

Table 2-19 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Definition	Device Specific Dynamic Power ($\mu\text{W}/\text{MHz}$)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PAC1	Clock contribution of a Global Rib	7.778	6.221	6.082	4.460	4.446	2.736	0.000	0.000
PAC2	Clock contribution of a Global Spine	4.334	3.512	2.759	2.718	1.753	1.971	3.483	3.483
PAC3	Clock contribution of a VersaTile row	1.379	1.445	1.377	1.483	1.467	1.503	1.472	1.472
PAC4	Clock contribution of a VersaTile used as a sequential module	0.151	0.149	0.151	0.149	0.149	0.151	0.146	0.146
PAC5	First contribution of a VersaTile used as a sequential module	0.057							
PAC6	Second contribution of a VersaTile used as a sequential module	0.207							
PAC7	Contribution of a VersaTile used as a combinatorial module	0.276	0.262	0.279	0.277	0.280	0.300	0.281	0.273
PAC8	Average contribution of a routing net	1.161	1.147	1.193	1.273	1.076	1.088	1.134	1.153
PAC9	Contribution of an I/O input pin (standard-dependent)	See Table 2-13 on page 2-10 through Table 2-15 on page 2-11.							
PAC10	Contribution of an I/O output pin (standard-dependent)	See Table 2-16 on page 2-11 through Table 2-18 on page 2-12.							
PAC11	Average contribution of a RAM block during a read operation	25.00							
PAC12	Average contribution of a RAM block during a write operation	30.00							
PAC13	Dynamic PLL contribution	2.70							

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case
Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	—	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
2.5 V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns
1.8 V LVCMOS	8 mA	8	High	5	—	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
1.5 V LVCMOS	4 mA	4	High	5	—	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns
3.3 V PCI	Per PCI spec	—	High	10	25 ²	0.97	1.97	0.18	0.73	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns
3.3 V PCI-X	Per PCI-X spec	—	High	10	25 ²	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-75 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 μA	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 μA	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 μA	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 μA	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 μA	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-76 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 μA	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 μA	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 μA	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 μA	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 μA	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-95 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	45	51	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12	91	74	10	10
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	16	16	91	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-96 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	35	44	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-135 • 1.2 V LVC MOS High SlewCommercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	8.57	0.26	1.53	1.10	8.23	7.38	2.51	2.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-136 • 1.2 V LVC MOS High Slew – Applies to 1.2 V DC Core VoltageCommercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V LVC MOS Wide Range

Table 2-137 • Minimum and Maximum DC Input and Output Levels for LVC MOS 1.2 V Wide Range

Applicable to Advanced I/O Banks

1.2 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁴	Max. mA ⁴	μA^5	μA^5
100 μA	2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

- The minimum drive strength for the default LVC MOS 1.2 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.
- IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 85°C junction temperature.
- Software default selection highlighted in gray.

1.2 V DC Core Voltage

Table 2-193 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

CS121	
Pin Number	AGL060 Function
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

CS196	
Pin Number	AGL250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0

CS196	
Pin Number	AGL250 Function
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3

CS196	
Pin Number	AGL250 Function
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1

QN68	
Pin Number	AGL030 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	AGL030 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132	
Pin Number	AGL060 Function
C16	IO60RSB1
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

QN132	
Pin Number	AGL125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	AGL125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	AGL125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

FG256	
Pin Number	AGL600 Function
H3	GFB1/IO163PPB3
H4	VCOMPLF
H5	GFC0/IO164NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	AGL600 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO117RSB2
M9	IO110RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1

FG256	
Pin Number	AGL600 Function
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	VJTAG
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2

FG484	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

FG484	
Pin Number	AGL600 Function
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC

FG484	
Pin Number	AGL600 Function
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	AGL1000 Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1