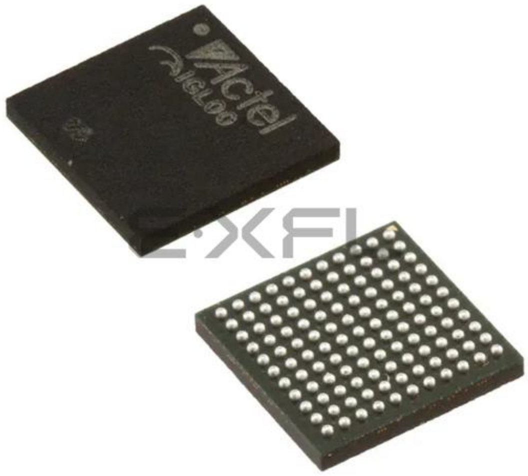
Microsemi Corporation - AGL060V2-CSG121 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-CSP (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v2-csg121

IGLOO Ordering Information

AGL1000 V2 – FG G 144 Y I

Application (Temperature Range)
Blank = Commercial (0°C to +85°C Junction Temperature)
I = Industrial (–40°C to +100°C Junction Temperature)
PP = Pre-Production
ES = Engineering Sample (Room Temperature Only)

Security Feature
Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G= RoHS-Compliant Packaging (some packages also halogen-free)

Package Type
UC = Micro Chip Scale Package (0.4 mm pitch)
CS = Chip Scale Package (0.4 mm and 0.5 mm pitches)
QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitch)
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)

Supply Voltage
2 = 1.2 V to 1.5 V
5 = 1.5 V only

Part Number

IGLOO Devices

AGL015 = 15,000 System Gates
AGL030 = 30,000 System Gates
AGL060 = 60,000 System Gates
AGL125 = 125,000 System Gates
AGL250 = 250,000 System Gates
AGL400 = 400,000 System Gates
AGL600 = 600,000 System Gates
AGL1000 = 1,000,000 System Gates

IGLOO Devices with Cortex-M1

M1AGL250 = 250,000 System Gates
M1AGL600 = 600,000 System Gates
M1AGL1000 = 1,000,000 System Gates

Note: Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.

Table 2-26 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-28 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions

	Commercial[1]		Industrial[2]	
	IIL[4]	IIH[5]	IIL[4]	IIH[5]
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[3]	10	10	15	15
1.2 V LVCMOS Wide Range[3]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
5. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*

Table 2-31 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 [2]	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 [2]	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-83 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-84 • **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-85 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-92 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
4 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
6 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
8 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
12 mA	Std.	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-93 • 2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
4 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
6 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns
8 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-94 • 2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
4 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
6 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
8 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-138 **• Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard Plus I/O Banks**

1.2 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

Table 2-139 **• Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard I/O Banks**

1.2 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 100°C junction temperature and maximum voltage.
5. Currents are measured at 85°C junction temperature.
6. Software default selection highlighted in gray.

Table 2-140 **• 1.2 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-75 for worst-case timing.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

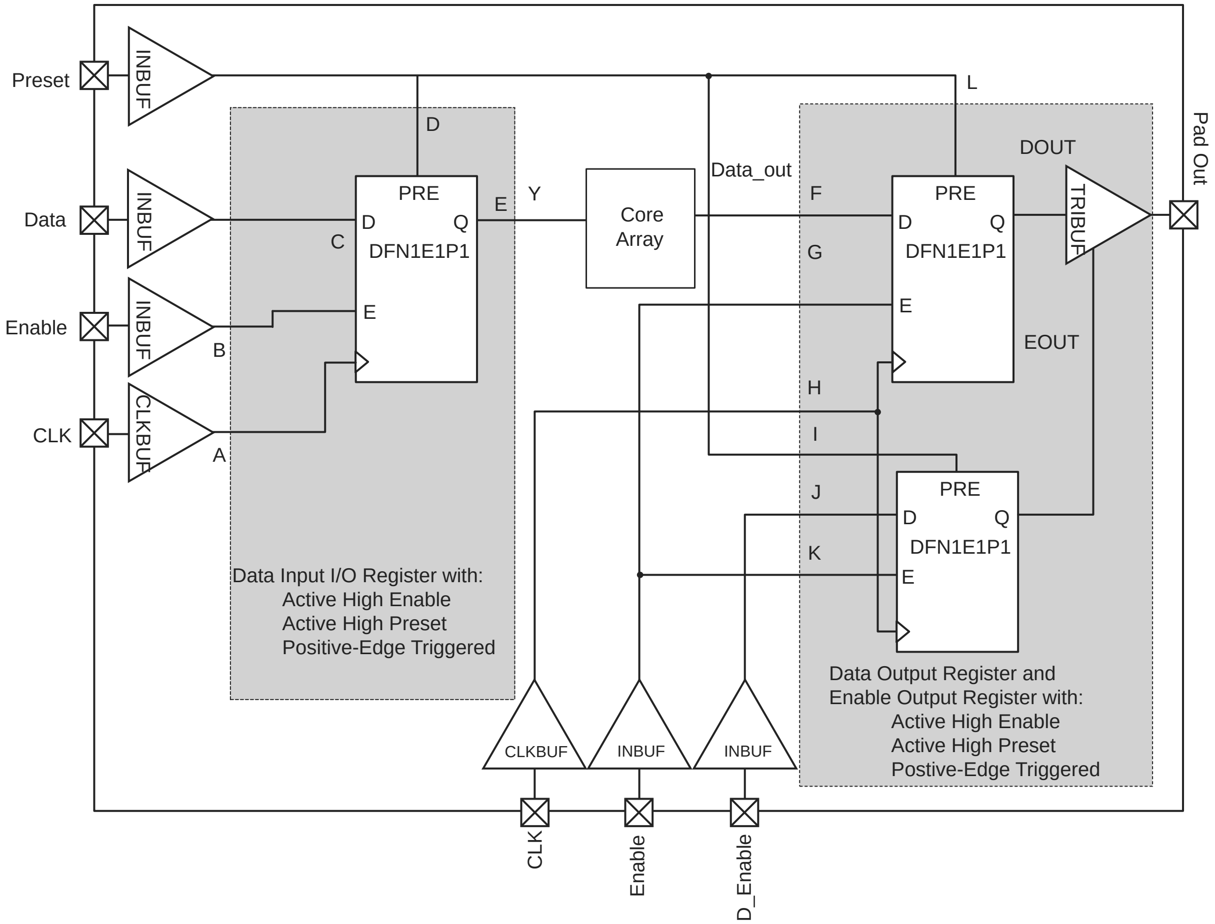

Figure 2-16 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

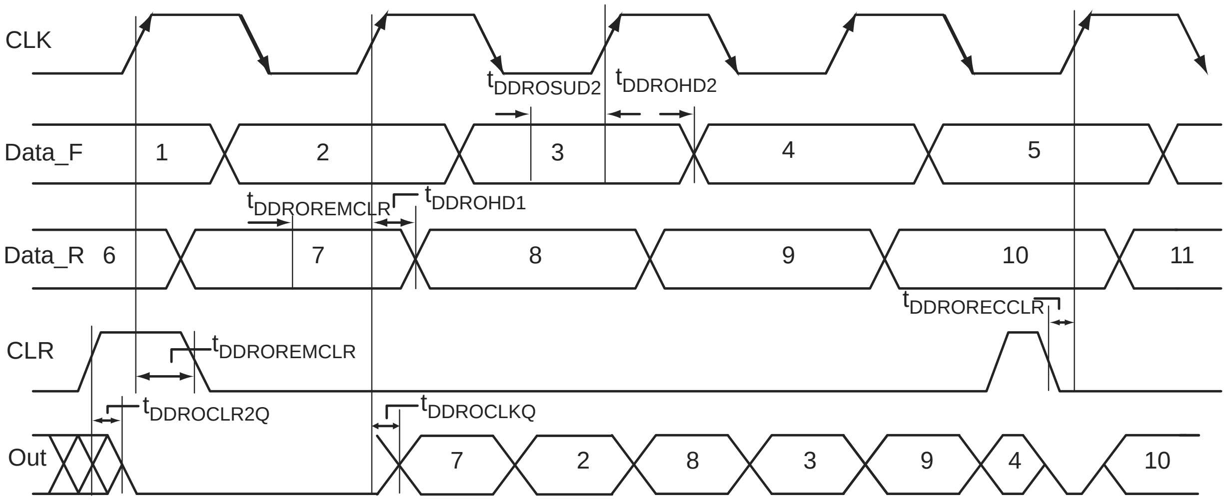

***Figure 2-24* • Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-167* • Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Global Resource Characteristics

AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 2-29 is an example of a global tree used for clock routing. The global tree presented in Figure 2-29 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

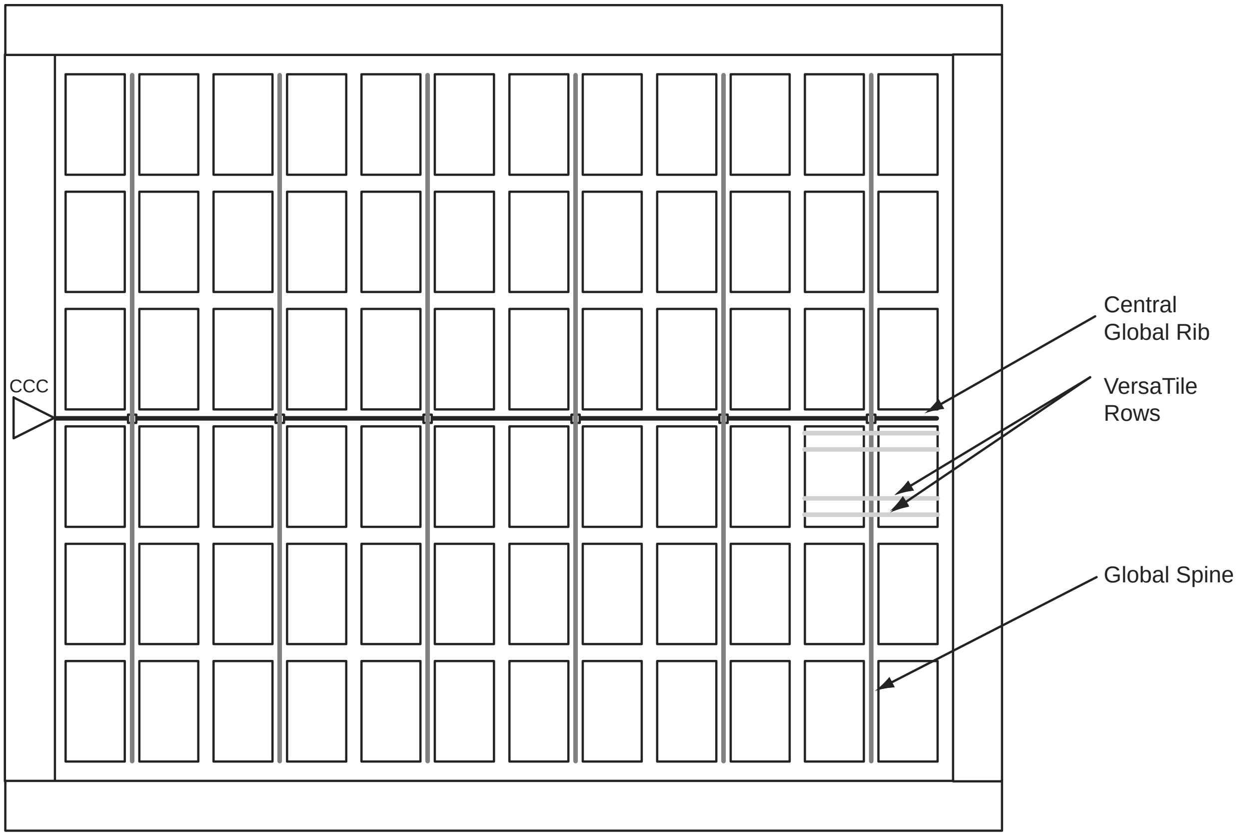

Figure 2-29 • **Example of Global Tree Use in an AGL250 Device for Clock Routing**

Table 2-187 • AGL600 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-188 • AGL1000 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-189 **• IGLOO CCC/PLL Specification**
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	**Min.**	**Typ.**	**Max.**	**Units**
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360[3]		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[4, 5]			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter[6]				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2]	0.469		15.65	ns
Delay Range in Block: Fixed Delay [1, 2]		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data[7]			
	SSO ≥ 4[8]	SSO ≥ 8[8]	SSO ≥ 16[8]	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.*
4. *The AGL030 device does not support a PLL.*
5. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
7. *Measurements done with LVTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. VCC/VCCPLL = 1.14 V, VQ/PQ/TQ type of packages, 20 pF load.*
8. *Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within ±200 ps of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.*

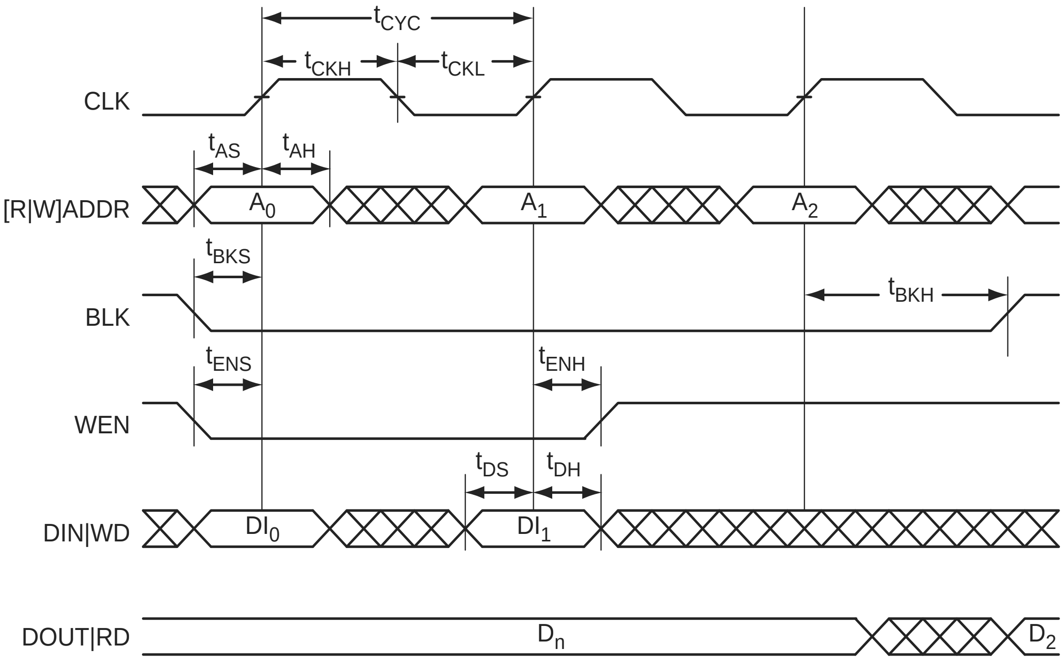

Figure 2-34 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

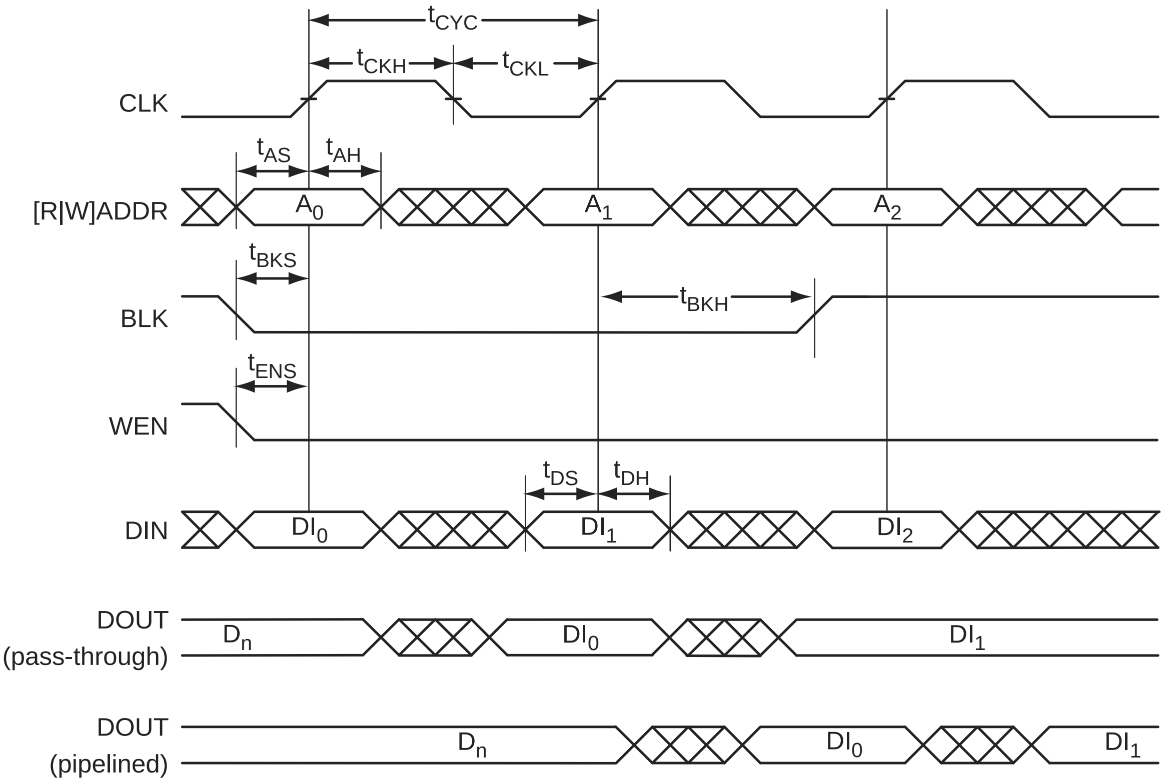

Figure 2-35 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

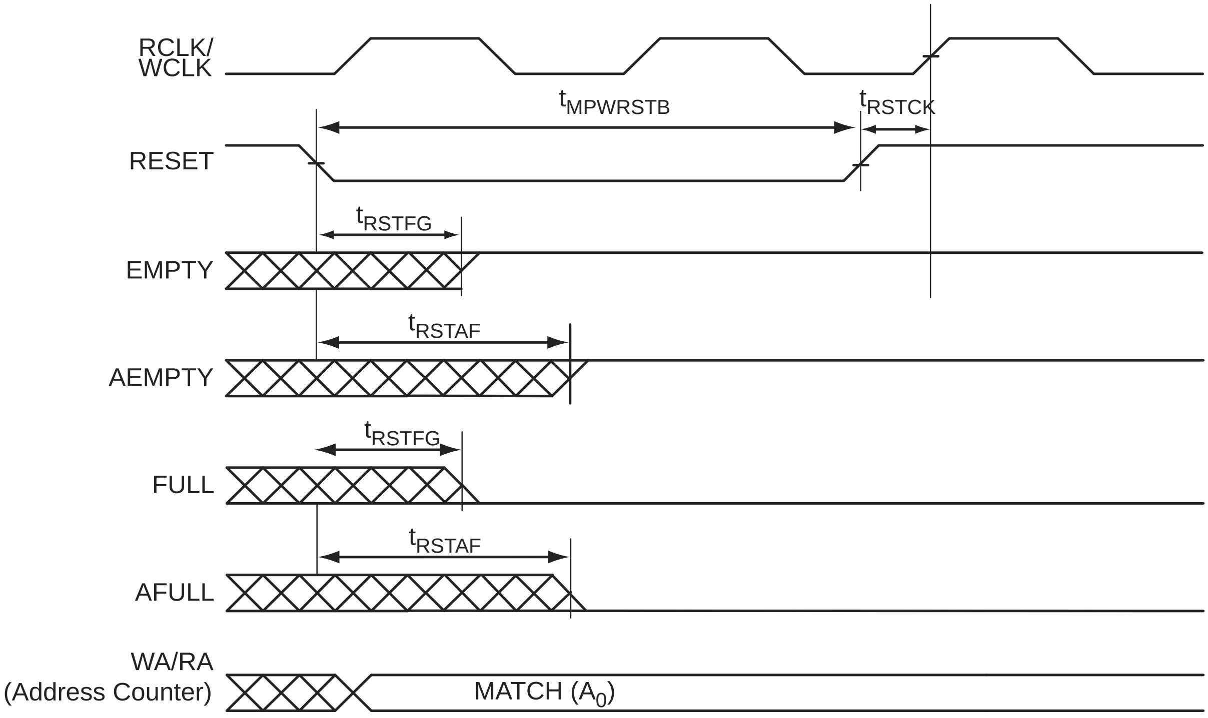

Figure 2-40 • **FIFO Reset**

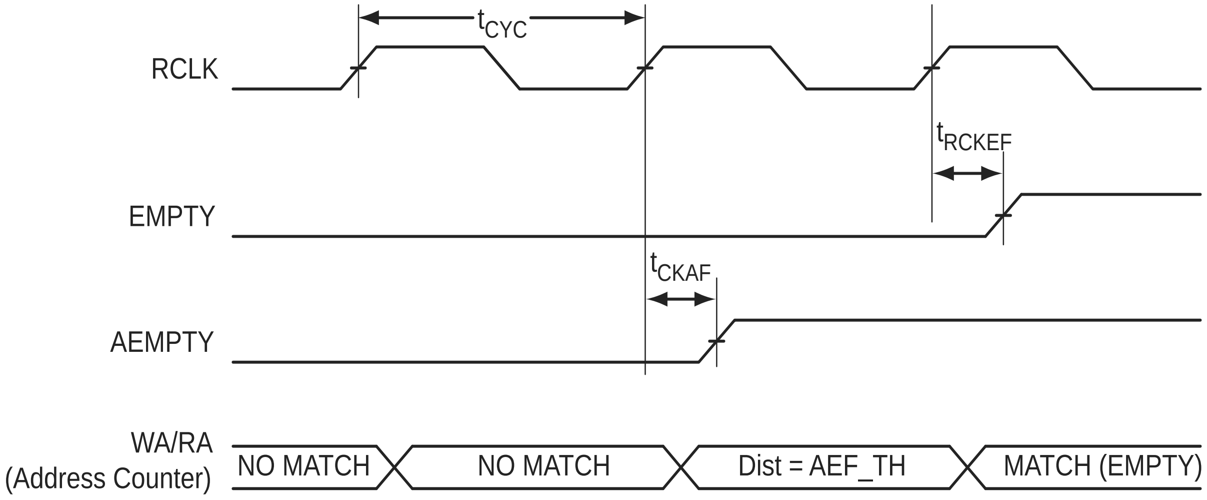

Figure 2-41 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

CS81	
Pin Number	**AGL030 Function**
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS196	
Pin Number	**AGL125 Function**
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	VCC
J8	VCC
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	VCCIB1
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	VCCIB0
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	VPUMP
L12	VJTAG
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	VCCIB1
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	VCCIB1
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	VCCIB1
M12	VMV1
M13	TRST
M14	VCCIB0
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

QN132	
Pin Number	**AGL060 Function**
C16	IO60RSB1
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

QN132	
Pin Number	**AGL250 Function**
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	FF/GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

FG144	
Pin Number	**AGL125 Function**
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	FF/GEB2/IO105RSB1
L4	IO102RSB1
L5	VCCIB1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG484	
Pin Number	**AGL600 Function**
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC