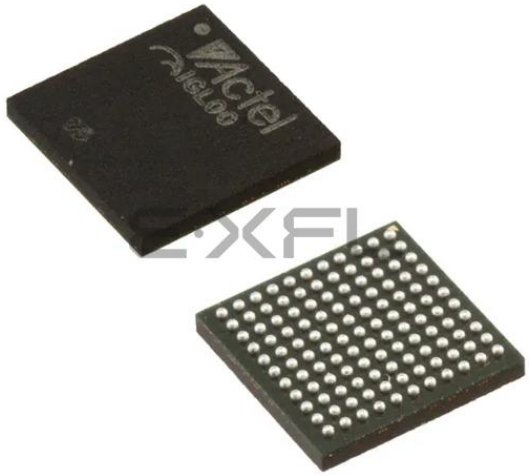

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-CSP (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v2-csg121i

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature [2]		0 to +85	40 to +100	℃
VCC[3]	1.5 V DC core supply voltage[5]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V 1.5 V wide range DC core supply voltage [4,6]		1.14 to 1.575	1.14 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [7]	0 to 3.6	0 to 3.6	V
VCCPLL[8]	Analog power supply (PLL)	1.5 V DC core supply voltage[5]	1.425 to 1.575	1.425 to 1.575	V
		1.2 V 1.5 V DC core supply voltage[4,6]	1.14 to 1.575	1.14 to 1.575	V
VCCI and VMV [9]	1.2 V DC core supply voltage[6]		1.14 to 1.26	1.14 to 1.26	V
	1.2 V DC wide range DC supply voltage[6]		1.14 to 1.575	1.14 to 1.575	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.0 V DC supply voltage [10]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.
2. Software Default Junction Temperature Range in the Libero SoC software is set to 0℃ to +70℃ for commercial, and -40℃ to +8 5℃ for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.
3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-25 on page 2-24. VCCI should be at the same voltage within a given I/O bank.
4. All IGLOO devices (V5 and V2) must be programmed with the VCC core voltage at 1.5 V. Applications using the V2 devices powered by 1.2 V supply must switch the core supply to 1.5 V for in-system programming.
5. For IGLOO^{fi} V5 devices
6. For IGLOO V2 devices only, operating at VCCI t VCC.
7. VPUMP can be left floating during operation (not programming mode).
8. VCCPLL pins should be tied to VCC pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information.
9. VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information.
10. 3.3 V wide range is compliant to the JESD-8B specification and supports 3.0 V VCCI operation.

Table 2-65 • **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard I/O Banks**

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-66 • **3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Table 2-192 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN, WEN setup time	0.73	ns
t_{ENH}	REN, WEN hold time	0.08	ns
t_{DS}	Input data (WD) setup time	0.71	ns
t_{DH}	Input data (WD) hold time	0.36	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	4.21	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.71	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	2.06	ns
	RESET Low to data out Low on RD (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET removal	0.61	ns
$t_{RECRSTB}$	RESET recovery	3.21	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.