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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	80
Number of Gates	60000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v2-qng132i

User I/O Characteristics

Timing Model

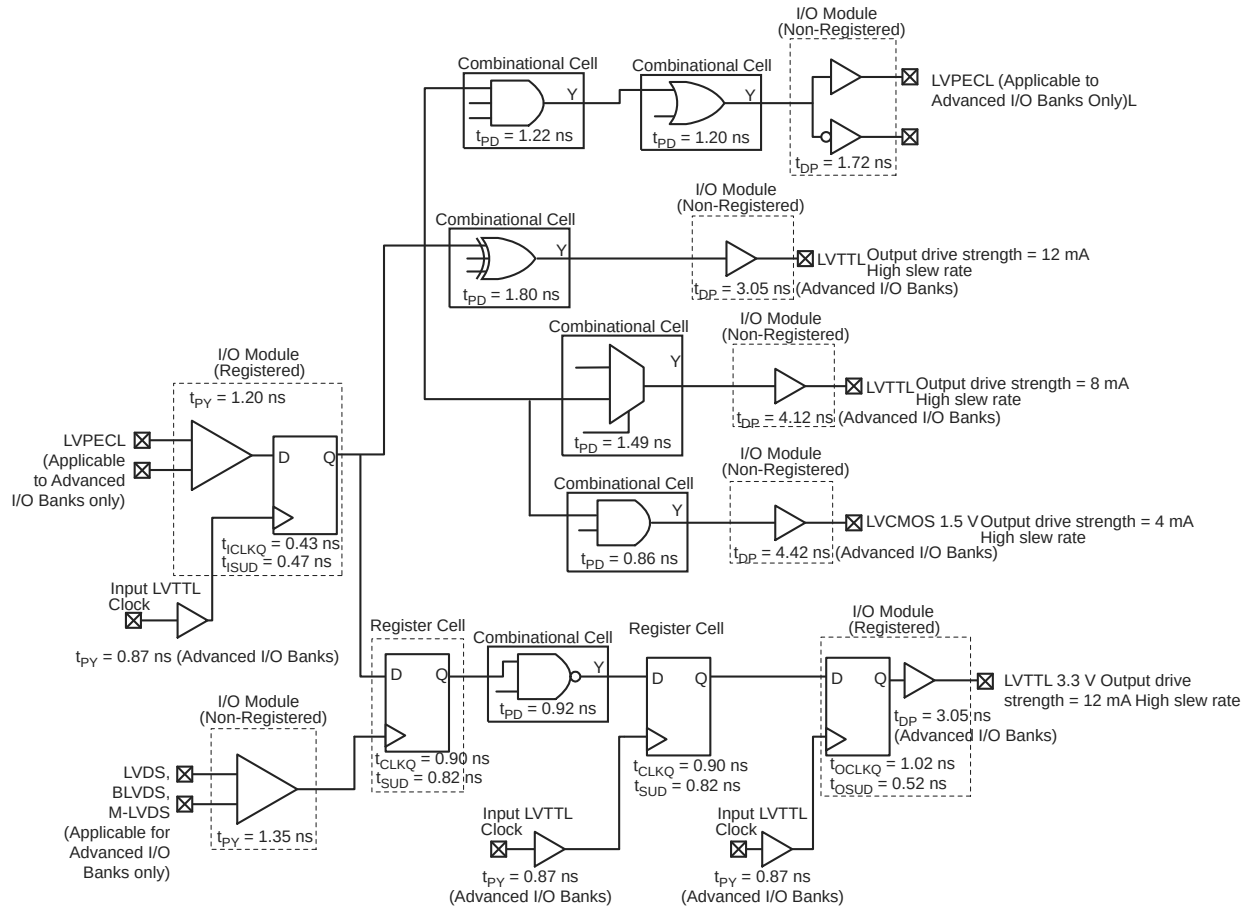


Figure 2-3 • Timing Model

Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst-Case $V_{CC} = 1.425$ V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Table 2-49 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		V _{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

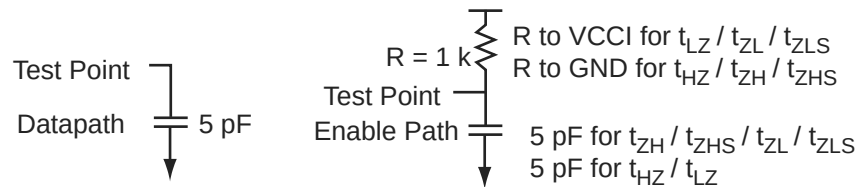


Figure 2-7 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-115 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-116 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-117 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-118 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-162 • Output Enable Register Propagation Delays****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-193 • RAM4K9

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

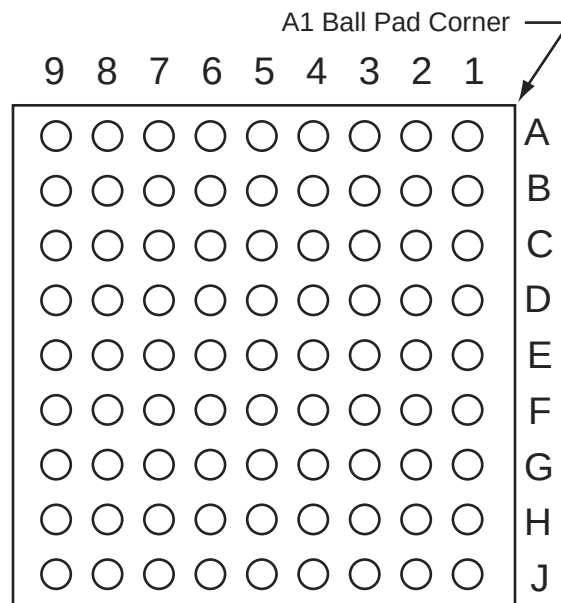
When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

UC81	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

UC81	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

UC81	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS81

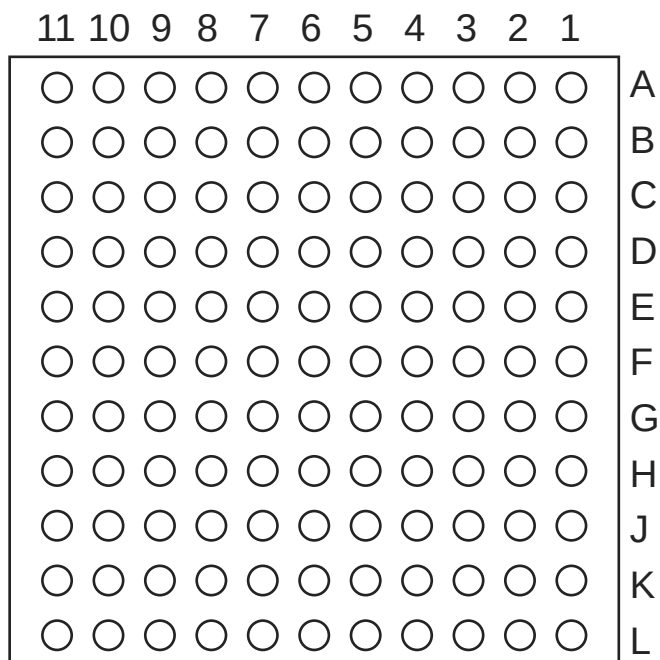


Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS121



Note: This is the bottom view of the package.

Note

For more information on package drawings, see PD3068: *Package Mechanical Drawings*.

CS121	
Pin Number	AGL060 Function
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

QN132	
Pin Number	AGL030 Function
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	VCCIB0
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC
C35	VCCIB0
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

QN132		QN132		QN132	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
A1	GAB2/IO117UPB3	A37	GBB1/IO38RSB0	B25	GND
A2	IO117VPB3	A38	GBC0/IO35RSB0	B26	IO54PDB1
A3	VCCIB3	A39	VCCIB0	B27	GCB2/IO52PDB1
A4	GFC1/IO110PDB3	A40	IO28RSB0	B28	GND
A5	GFB0/IO109NPB3	A41	IO22RSB0	B29	GCB0/IO49NDB1
A6	VCCPLF	A42	IO18RSB0	B30	GCC1/IO48PDB1
A7	GFA1/IO108PPB3	A43	IO14RSB0	B31	GND
A8	GFC2/IO105PPB3	A44	IO11RSB0	B32	GBB2/IO42PDB1
A9	IO103NDB3	A45	IO07RSB0	B33	VMV1
A10	VCC	A46	VCC	B34	GBA0/IO39RSB0
A11	GEA1/IO98PPB3	A47	GAC1/IO05RSB0	B35	GBC1/IO36RSB0
A12	GEA0/IO98NPB3	A48	GAB0/IO02RSB0	B36	GND
A13	GEC2/IO95RSB2	B1	IO118VDB3	B37	IO26RSB0
A14	IO91RSB2	B2	GAC2/IO116UDB3	B38	IO21RSB0
A15	VCC	B3	GND	B39	GND
A16	IO90RSB2	B4	GFC0/IO110NDB3	B40	IO13RSB0
A17	IO87RSB2	B5	VCOMPLF	B41	IO08RSB0
A18	IO85RSB2	B6	GND	B42	GND
A19	IO82RSB2	B7	GFB2/IO106PSB3	B43	GAC0/IO04RSB0
A20	IO76RSB2	B8	IO103PDB3	B44	GNDQ
A21	IO70RSB2	B9	GND	C1	GAA2/IO118UDB3
A22	VCC	B10	GEB0/IO99NDB3	C2	IO116VDB3
A23	GDB2/IO62RSB2	B11	VMV3	C3	VCC
A24	TDI	B12	FF/GEB2/IO96RSB2	C4	GFB1/IO109PPB3
A25	TRST	B13	IO92RSB2	C5	GFA0/IO108NPB3
A26	GDC1/IO58UDB1	B14	GND	C6	GFA2/IO107PSB3
A27	VCC	B15	IO89RSB2	C7	IO105NPB3
A28	IO54NDB1	B16	IO86RSB2	C8	VCCIB3
A29	IO52NDB1	B17	GND	C9	GEB1/IO99PDB3
A30	GCA2/IO51PPB1	B18	IO78RSB2	C10	GNDQ
A31	GCA0/IO50NPB1	B19	IO72RSB2	C11	GEA2/IO97RSB2
A32	GCB1/IO49PDB1	B20	GND	C12	IO94RSB2
A33	IO47NSB1	B21	GNDQ	C13	VCCIB2
A34	VCC	B22	TMS	C14	IO88RSB2
A35	IO41NPB1	B23	TDO	C15	IO84RSB2
A36	GBA2/IO41PPB1	B24	GDC0/IO58VDB1	C16	IO80RSB2

VQ100	
Pin Number	AGL060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	VCOMPLF
13	GFA0/IO85RSB1
14	VCCPLF
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	VCC
18	VCCIB1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1

VQ100	
Pin Number	AGL060 Function
37	VCC
38	GND
39	VCCIB1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0

VQ100	
Pin Number	AGL060 Function
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	VCCIB0
88	GND
89	VCC
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

FG144	
Pin Number	AGL1000 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

FG144	
Pin Number	AGL1000 Function
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

FG144	
Pin Number	AGL1000 Function
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

FG256	
Pin Number	AGL400 Function
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	AGL400 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1

FG256	
Pin Number	AGL400 Function
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2

FG256	
Pin Number	AGL1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	AGL600 Function
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1

FG484	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

FG484	
Pin Number	AGL600 Function
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

Revision / Version	Changes	Page
Revision 8 (cont'd)	Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, and Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹ were updated to change PDC2 to PDC6 and PDC3 to PDC7. The table notes were updated to reflect that power was measured on VCCI.	2-10 through 2-11
	In Table 2-19 • Different Components Contributing to Dynamic Power Consumption in IGLOO Devices, the description for PAC13 was changed from Static to Dynamic.	2-13
	Table 2-20 • Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-22 • Different Components Contributing to the Static Power Consumption in IGLOO Device were updated to add PDC6 and PDC7, and to change the definition for PDC5 to bank quiescent power. Subtitles were added to indicate type of devices and core supply voltage.	2-14, 2-16
	The "Total Static Power Consumption—PSTAT" section was updated to revise the calculation of P _{STAT} , including PDC6 and PDC7.	2-17
	Footnote † was updated to include information about PAC13. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-18
Revision 7 (Jun 2008) Packaging v1.5	The "QN132" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-28
Revision 6 (Jun 2008) Packaging v1.4	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	Pin numbers were added to the "QN68" package diagram. Note 2 was added below the diagram.	4-25
Revision 5 (Mar 2008) Packaging v1.3	The "CS196" package and pin table was added for AGL250.	4-12
Revision 4 (Mar 2008) Product Brief v1.0	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 12 μW)" was removed from "Low Power Active FPGA Operation."	I
	1.2_V was added to the list of core and I/O voltages in the "Advanced I/O" and "I/Os with Advanced I/O Standards" section sections.	I, 1-7
	The "Embedded Memory" section was updated to remove the footnote reference from the section heading and place it instead after "4,608-Bit" and "True Dual-Port SRAM (except ×18)."	I