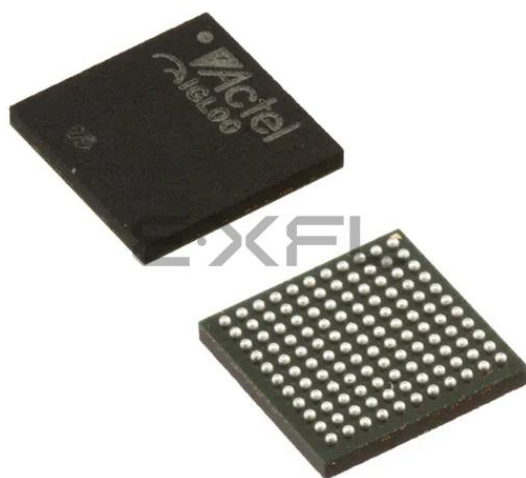




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	121-VFBGA, CSBGA
Supplier Device Package	121-CSP (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v5-csg121

Flash Advantages

Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

Security

Nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry-standard security, making remote ISP possible. An IGLOO device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based IGLOO devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 μ s) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and

2 – IGLOO DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits ¹	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV ²	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ³	Storage Temperature	–65 to +150	°C
T _J ³	Junction Temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.
2. VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information.
3. For flash programming and retention, maximum limits refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.

Ramping up (V2 devices): $0.65\text{ V} < \text{trip_point_up} < 1.05\text{ V}$
 Ramping down (V2 devices): $0.55\text{ V} < \text{trip_point_down} < 0.95\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the ProASIC®3 and ProASIC3E FPGA fabric user guides for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

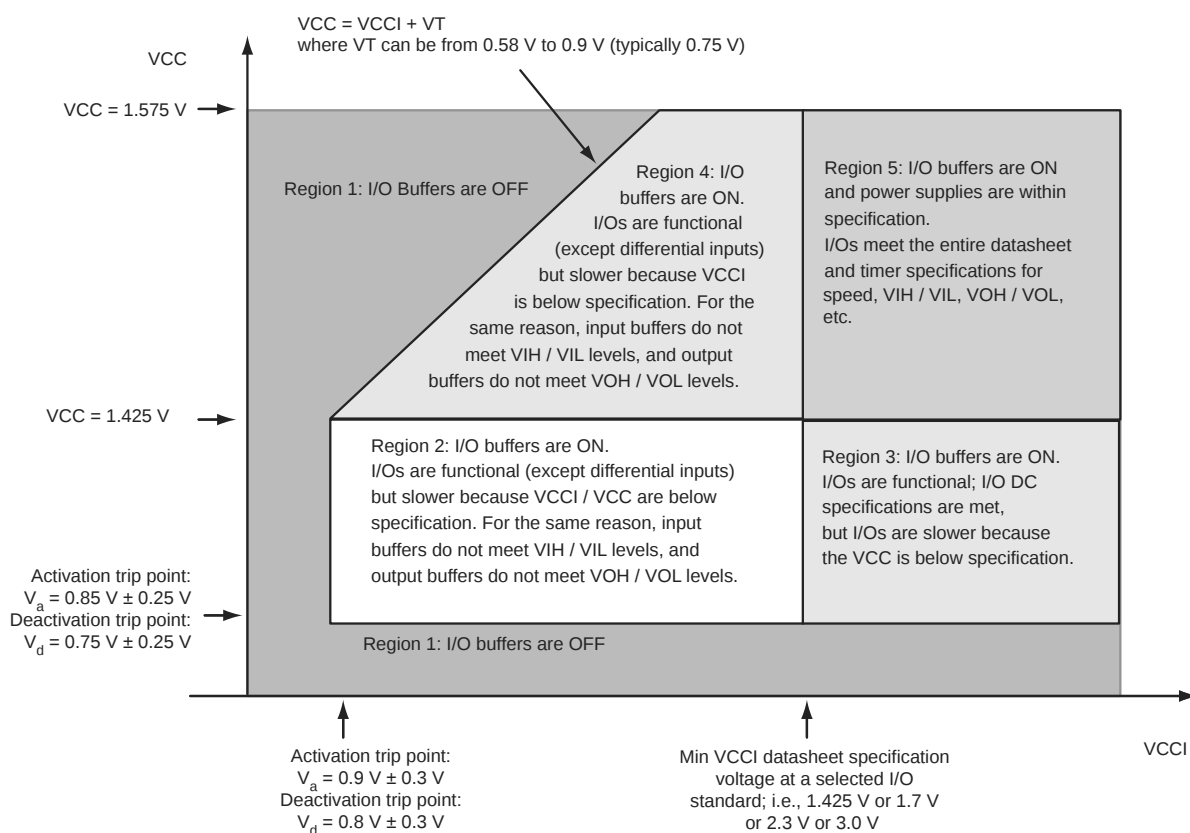


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.27
3.3 V LVCMOS Wide Range ³	3.3	–	16.27
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.61
1.5 V LVCMOS (JESD8-11)	1.5	–	0.96
1.2 V LVCMOS ⁴	1.2	–	0.58
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.58
3.3 V PCI	3.3	–	17.67
3.3 V PCI-X	3.3	–	17.67
Differential			
LVDS	2.5	2.26	23.39
LVPECL	3.3	5.72	59.05

Notes:

1. P_{DC6} is the static power (where applicable) measured on VCCI.
2. P_{AC9} is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO V2 devices only

Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.41
3.3 V LVCMOS Wide Range ³	3.3	–	16.41
2.5 V LVCMOS	2.5	–	4.75
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.00
1.2 V LVCMOS ⁴	1.2	–	0.61
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.61
3.3 V PCI	3.3	–	17.78
3.3 V PCI-X	3.3	–	17.78

Notes:

1. P_{DC6} is the static power (where applicable) measured on VCCI.
2. P_{AC9} is the total dynamic power measured on VCCI.
3. Applicable for IGLOO V2 devices only.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

Timing Characteristics***Applies to 1.5 V DC Core Voltage***

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-53 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Characteristics*Applies to 1.5 V DC Core Voltage***Table 2-83 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.***Table 2-84 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-85 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-95 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	45	51	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12	91	74	10	10
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	16	16	91	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-96 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	17	22	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	35	44	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	35	44	10	10

Notes:

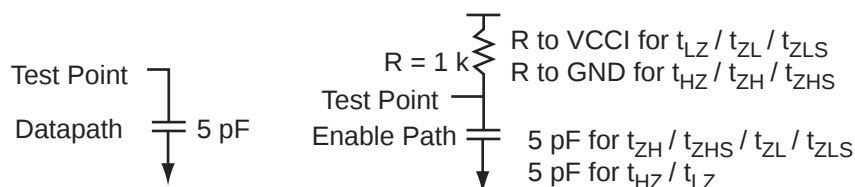
1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-97 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-9 • AC Loading****Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-99 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-100 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-101 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-102 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-103 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

Table 2-127 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-128 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-129 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.2 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
1 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	20	26	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-155 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-16 on page 2-84 for more information.

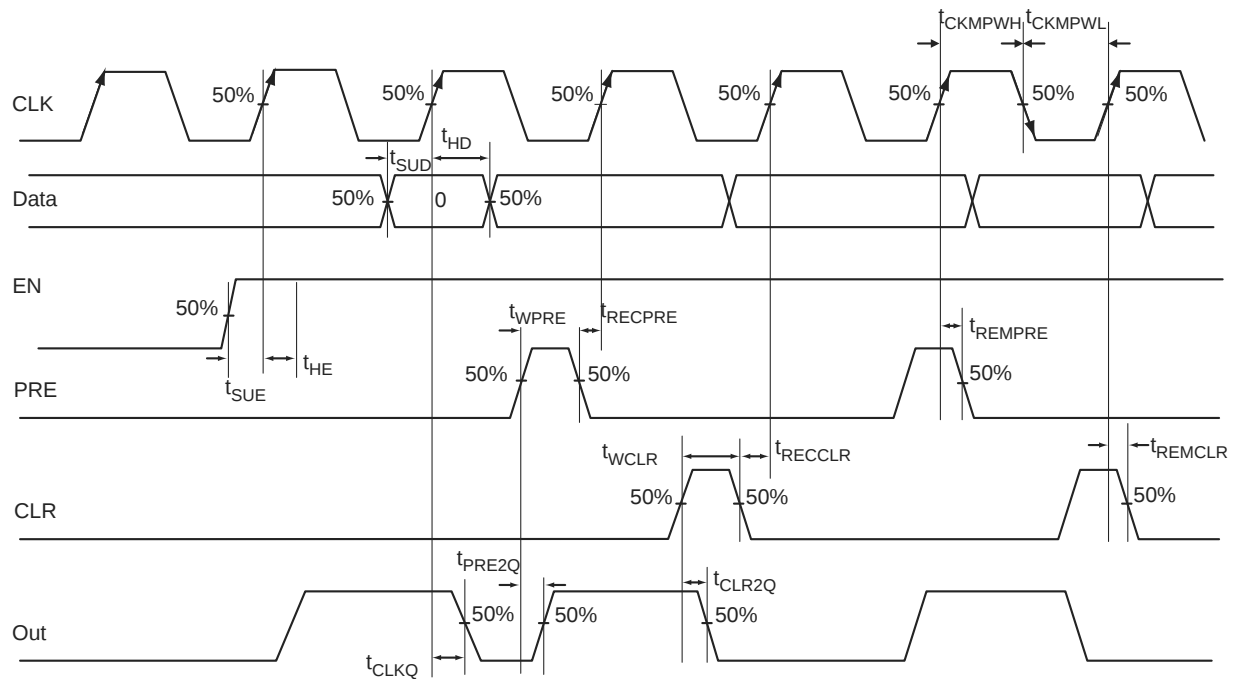


Figure 2-28 • Timing Model and Waveforms

Timing Characteristics

1.5 V DC Core Voltage

Table 2-171 • Register Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-175 • AGL060 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.35	1.62	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-176 • AGL125 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-199 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
t_{TRSTREM}	ResetB Removal Time	0.58	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-200 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
t_{TRSTREM}	ResetB Removal Time	1.18	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

CS196	
Pin Number	AGL125 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	AGL125 Function
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	AGL125 Function
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

CS196	
Pin Number	AGL250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0

CS196	
Pin Number	AGL250 Function
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3

CS196	
Pin Number	AGL250 Function
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1

CS281	
Pin Number	AGL1000 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO13RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO20RSB0
A8	IO24RSB0
A9	IO29RSB0
A10	VCCIB0
A11	IO39RSB0
A12	IO45RSB0
A13	IO48RSB0
A14	IO58RSB0
A15	IO61RSB0
A16	IO62RSB0
A17	GBC1/IO73RSB0
A18	GBA0/IO76RSB0
A19	GND
B1	GAA2/IO225PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO12RSB0
B6	GND
B7	IO21RSB0
B8	IO26RSB0
B9	IO34RSB0
B10	IO35RSB0
B11	IO36RSB0
B12	IO46RSB0
B13	IO52RSB0
B14	GND
B15	IO59RSB0
B16	GBC0/IO72RSB0
B17	GBA1/IO77RSB0

CS281	
Pin Number	AGL1000 Function
B18	VCCIB1
B19	IO79NDB1
C1	GAB2/IO224PPB3
C2	IO225NPB3
C6	IO18RSB0
C14	IO63RSB0
C18	IO78NPB1
C19	GBB2/IO79PDB1
D1	IO219PPB3
D2	IO223NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO15RSB0
D7	IO19RSB0
D8	IO27RSB0
D9	IO32RSB0
D10	GND
D11	IO38RSB0
D12	IO44RSB0
D13	IO47RSB0
D14	IO60RSB0
D15	GBB0/IO74RSB0
D16	GBA2/IO78PPB1
D18	GBC2/IO80PPB1
D19	IO88NPB1
E1	IO217NPB3
E2	IO221PPB3
E4	IO221NPB3
E5	IO10RSB0
E6	IO14RSB0
E7	IO25RSB0
E8	IO28RSB0
E9	IO31RSB0
E10	IO33RSB0
E11	IO42RSB0
E12	IO49RSB0

CS281	
Pin Number	AGL1000 Function
E13	IO53RSB0
E14	GBB1/IO75RSB0
E15	IO80NPB1
E16	IO85PPB1
E18	IO83PPB1
E19	IO84NPB1
F1	IO214NPB3
F2	GND
F3	IO217PPB3
F4	IO219NPB3
F5	IO224NPB3
F15	IO85NPB1
F16	IO84PPB1
F17	IO83NPB1
F18	GND
F19	IO90PPB1
G1	IO212NPB3
G2	IO211NDB3
G4	IO214PPB3
G5	IO212PPB3
G7	GAC2/IO223PPB3
G8	VCCIB0
G9	IO30RSB0
G10	IO37RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO88PPB1
G15	IO89NDB1
G16	IO89PDB1
G18	GCC0/IO91NPB1
G19	GCB1/IO92PPB1
H1	GFB0/IO208NPB3
H2	IO211PDB3
H4	GFC1/IO209PPB3
H5	GFB1/IO208PPB3
H7	VCCIB3

QN132	
Pin Number	AGL125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	AGL125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	AGL125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

FG256	
Pin Number	AGL400 Function
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	FF/GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

FG484	
Pin Number	AGL1000 Function
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2