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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	1536
Total RAM Bits	18432
Number of I/O	80
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl060v5-qng132

Table 2-3 • **Flash Programming Limits – Retention, Storage, and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 on page 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits [1]**

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI **Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 Devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

VCC **Trip Point:**
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for the AGL1000-FG484 package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{23.3\text{°C/W}} = 1.28\ \text{W}$$

EQ 2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Unit
				Still Air	1 m/s	2.5 m/s	
Quad Flat No Lead (QN)	AGL030	132	13.1	21.4	16.8	15.3	C/W
	AGL060	132	11.0	21.2	16.6	15.0	C/W
	AGL125	132	9.2	21.1	16.5	14.9	C/W
	AGL250	132	8.9	21.0	16.4	14.8	C/W
	AGL030	68	13.4	68.4	45.8	43.1	C/W
Very Thin Quad Flat Pack (VQ)*		100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CS)	AGL1000	281	6.0	28.0	22.8	21.5	C/W
	AGL400	196	7.2	37.1	31.1	28.9	C/W
	AGL250	196	7.6	38.3	32.2	30.0	C/W
	AGL125	196	8.0	39.5	33.4	31.1	C/W
	AGL030	81	12.4	32.8	28.5	27.2	C/W
	AGL060	81	11.1	28.8	24.8	23.5	C/W
	AGL250	81	10.4	26.9	22.3	20.9	C/W
Micro Chip Scale Package (UC)	AGL030	81	16.9	40.6	35.2	33.7	C/W
Fine Pitch Ball Grid Array (FG)	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL400	144	6.8	37.6	31.2	29.0	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

*Note: *Thermal resistances for other device-package combinations will be posted in a later revision.*

Disclaimer:

The simulation for determining the junction-to-air thermal resistance is based on JEDEC standards (JESD51) and assumptions made in building the model. Junction-to-case is based on SEMI G38-88. JESD51 is only used for comparing one package to another package, provided the two tests uses the same condition. They have little relevance in actual application and therefore should be used with a degree of caution.

Table 2-65 • **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard I/O Banks**

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	µA	µA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-66 • **3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Table 2-71 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 µA	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-72 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	4 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	6 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 µA	8 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-79 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-80 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-151* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

***Table 2-152* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

*Note: *Measuring point = Vtrip. See Table 2-28 on page 2-104 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-153* • LVPECL – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

***Table 2-154* • LVPECL – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-185 • **AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-186 • **AGL400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.18	2.64	ns
t_{RCKH}	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-187 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-188 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Timing Waveforms

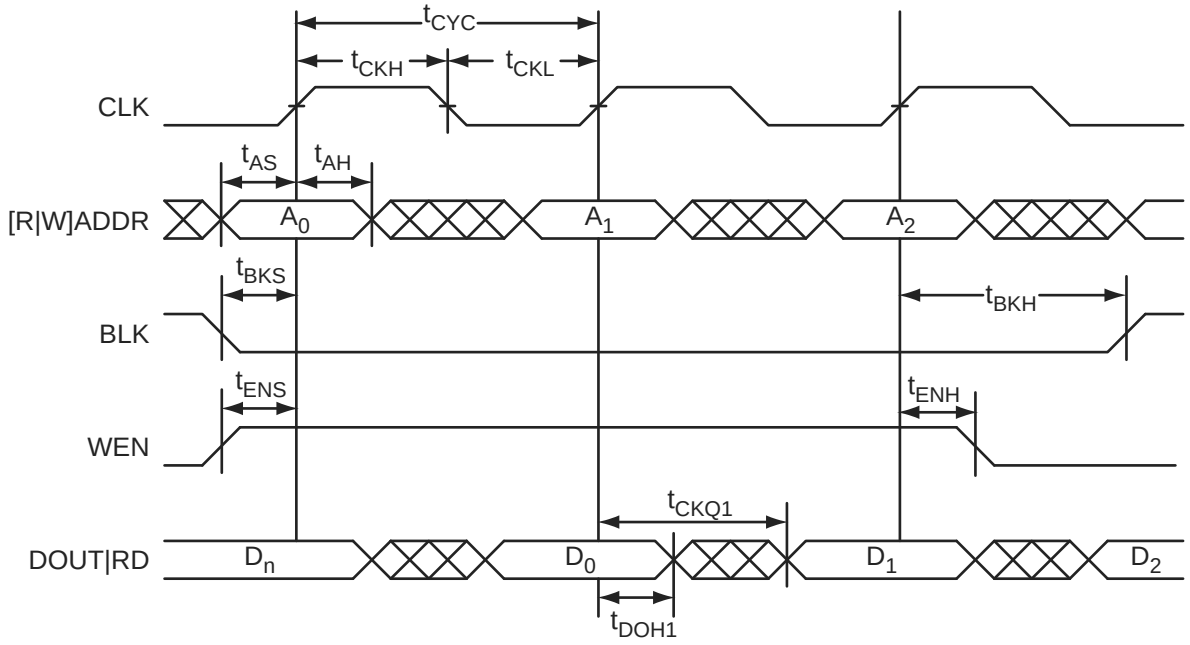


Figure 2-32 • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

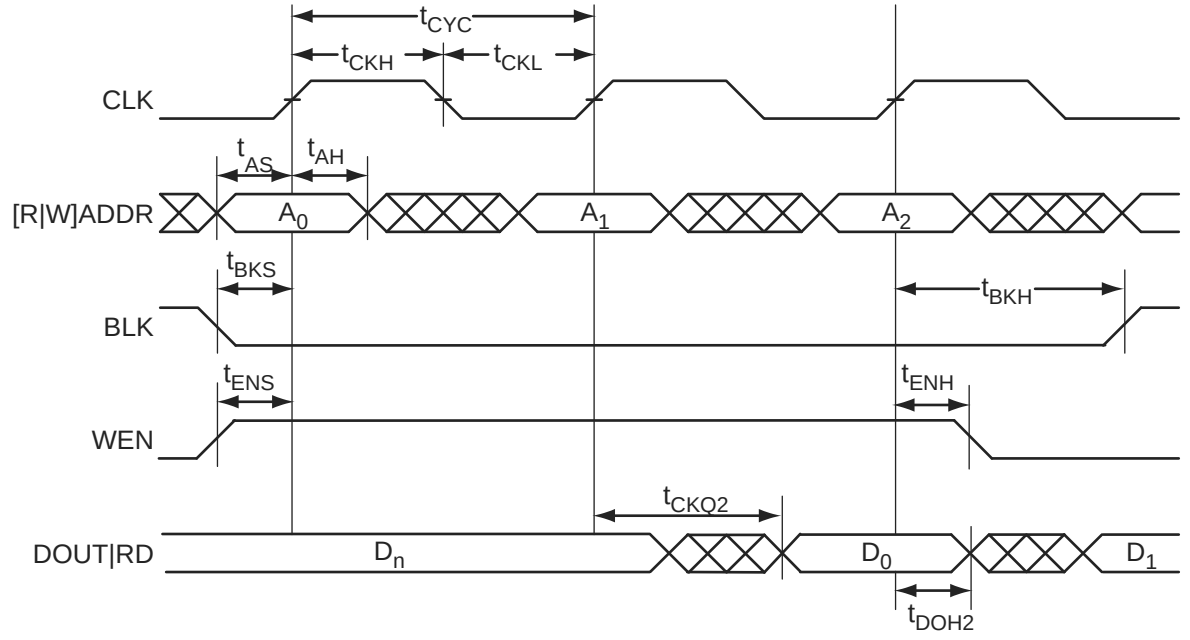


Figure 2-33 • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

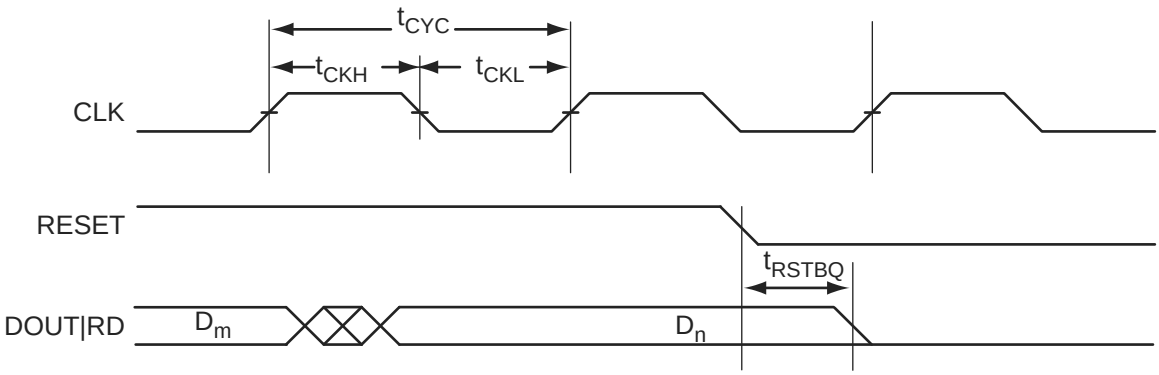


Figure 2-36 • **RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

Timing Waveforms

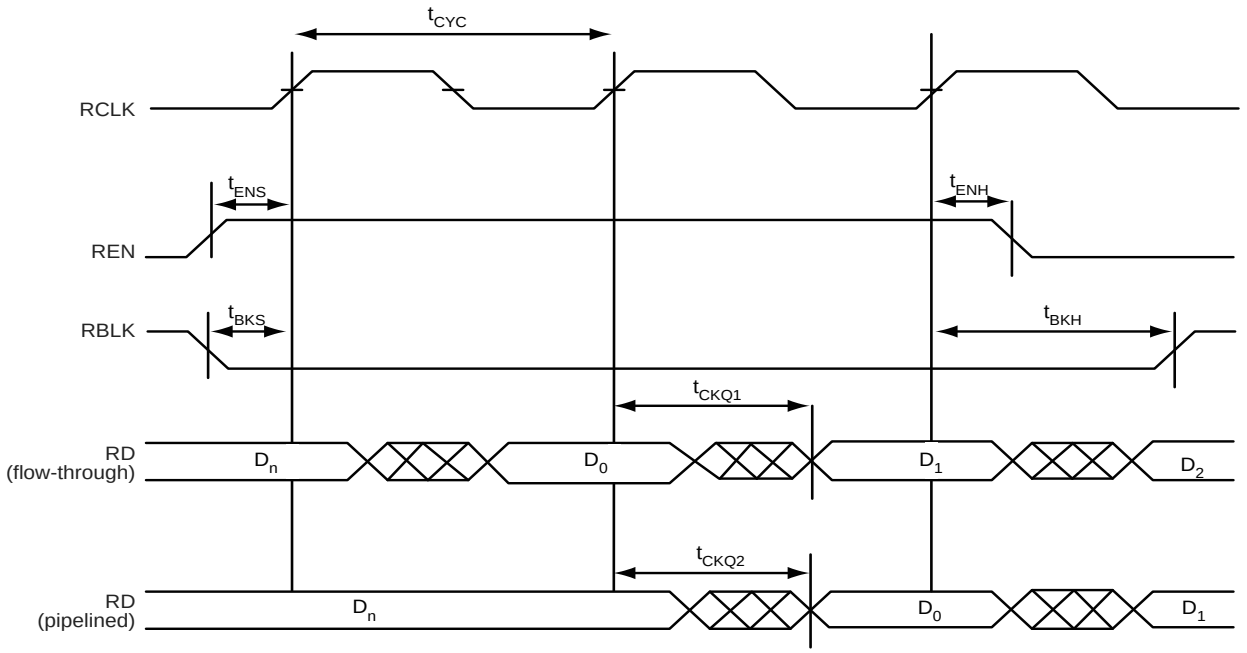


Figure 2-38 • **FIFO Read**

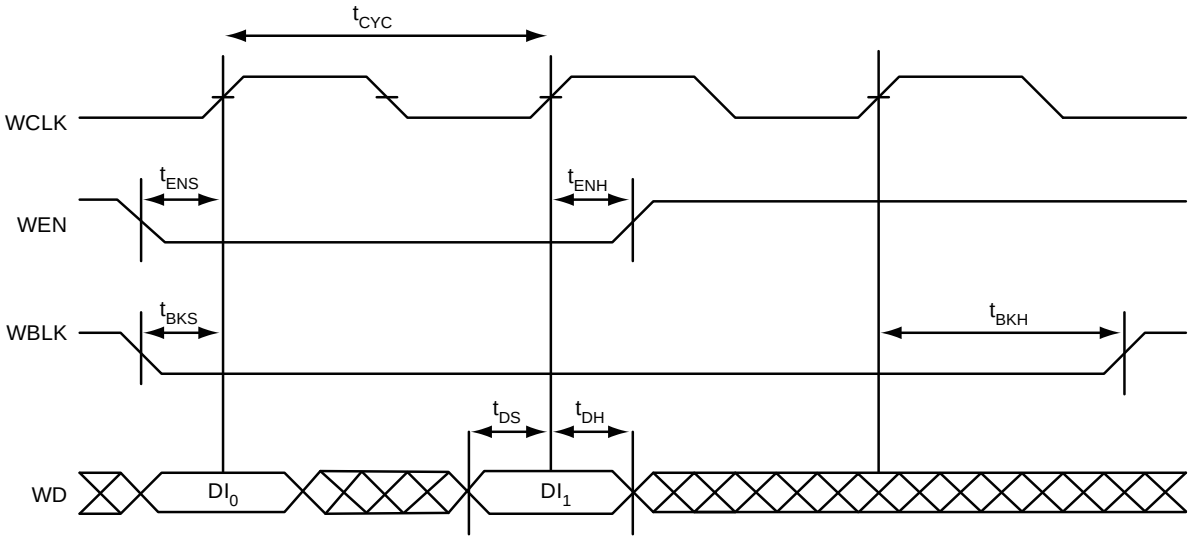


Figure 2-39 • **FIFO Write**

3 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices, and 1.2 V or 1.5 V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

- 1.5 V for IGLOO V5 devices
- 1.2 V or 1.5 V for IGLOO V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

- There is one VCCPLF pin on IGLOO devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.

CS196	
Pin Number	**AGL400 Function**
H10	GCC1/IO67PDB1
H11	GCB0/IO68NDB1
H12	GCA1/IO69PDB1
H13	IO70NDB1
H14	GCA2/IO70PDB1
J1	GFC2/IO142PDB3
J2	IO141PPB3
J3	IO143NPB3
J4	IO140PDB3
J5	IO140NDB3
J6	IO109RSB2
J7	VCC
J8	VCC
J9	IO84RSB2
J10	IO75PDB1
J11	GCB2/IO71PDB1
J12	IO71NDB1
J13	GDC1/IO77UDB1
J14	GDC0/IO77VDB1
K1	IO142NDB3
K2	GND
K3	IO141NPB3
K4	VCCIB3
K5	IO138PPB3
K6	IO125RSB2
K7	IO110RSB2
K8	IO98RSB2
K9	IO104RSB2
K10	IO75NDB1
K11	VCCIB1
K12	GDA1/IO79UPB1
K13	GND
K14	GDB1/IO78UDB1
L1	GEB1/IO136PDB3
L2	GEC1/IO137PDB3
L3	GEC0/IO137NDB3

CS196	
Pin Number	**AGL400 Function**
L4	IO138NPB3
L5	IO122RSB2
L6	IO128RSB2
L7	IO101RSB2
L8	IO88RSB2
L9	IO86RSB2
L10	IO94RSB2
L11	VPUMP
L12	VJTAG
L13	GDA0/IO79VPB1
L14	GDB0/IO78VDB1
M1	GEB0/IO136NDB3
M2	GEA1/IO135PPB3
M3	GNDQ
M4	VCCIB2
M5	IO120RSB2
M6	IO119RSB2
M7	IO112RSB2
M8	VCCIB2
M9	IO89RSB2
M10	GDB2/IO81RSB2
M11	VCCIB2
M12	VMV2
M12	VMV2
M13	TRST
M14	VCCIB1
N1	GEA0/IO135NPB3
N2	VMV3
N3	GEC2/IO132RSB2
N4	IO130RSB2
N5	GND
N6	IO117RSB2
N7	IO106RSB2
N8	IO100RSB2
N9	IO92RSB2
N10	GND

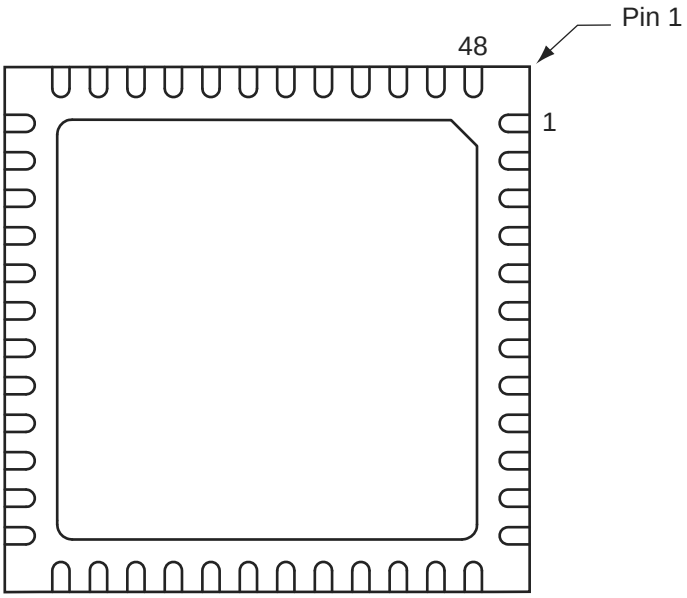
CS196	
Pin Number	**AGL400 Function**
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO134RSB2
P3	FF/GEB2/IO133RSB2
P4	IO123RSB2
P5	IO116RSB2
P6	IO114RSB2
P7	IO107RSB2
P8	IO103RSB2
P9	IO95RSB2
P10	IO91RSB2
P11	GDC2/IO82RSB2
P12	GDA2/IO80RSB2
P13	TMS
P14	GND

CS281	
Pin Number	AGL1000 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	VCOMPLF
J2	GFA0/IO207NDB3
J4	VCCPLF
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	VCCIB3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO96PPB1

CS281	
Pin Number	AGL1000 Function
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	VCCIB1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3

CS281	
Pin Number	AGL1000 Function
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	VCCIB2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	VCCIB2
N13	VPUMP
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2

QN48



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN132	
Pin Number	**AGL250 Function**
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG144	
Pin Number	**AGL1000 Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	**AGL1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	**AGL1000 Function**
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	**AGL1000 Function**
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG484	
Pin Number	**AGL400 Function**
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2

Revision / Version	Changes	Page
Revision 14 (Feb 2009) Product Brief v1.4	The "Advanced I/O" section was revised to include two bullets regarding wide range power supply voltage support.	I
	3.0 V wide range was added to the list of supported voltages in the "I/Os with Advanced I/O Standards" section. The "Wide Range I/O Support" section is new.	1-8
Revision 13 (Jan 2009) Packaging v1.8	The "CS121" pin table was revised to add a note regarding pins F1 and G1.	4-7
Revision 12 (Dec 2008) Product Brief v1.3	QN48 and QN68 were added to the AGL030 for the following tables: "IGLOO Devices" Product Family Table "IGLOO Ordering Information" "Temperature Grade Offerings"	N/A
	QN132 is fully supported by AGL125 so footnote 3 was removed.	
Packaging v1.7	The "QN48" pin diagram and pin table are new.	4-24
	The "QN68" pin table for AGL030 is new.	4-26
Revision 12 (Dec 2008)	The AGL600 Function for pin K15 in the "FG484" table was changed to VCCIB1.	4-78
Revision 11 (Oct 2008) Product Brief v1.2	This document was updated to include AGL400 device information. The following sections were updated: "IGLOO Devices" Product Family Table "IGLOO Ordering Information" "Temperature Grade Offerings" Figure 1-2 • IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)	N/A
DC and Switching Characteristics Advance v0.5	The tables in the "Quiescent Supply Current" section were updated with values for AGL400. In addition, the title was updated to include: (VCC = VJTAG = VPP = 0 V).	2-7
	The tables in the "Power Consumption of Various Internal Resources" section were updated with values for AGL400.	2-13
	Table 2-178 • AGL400 Global Resource is new.	2-109
Packaging v1.6	The "CS196" table for the AGL400 device is new.	4-14
	The "FG144" table for the AGL400 device is new.	4-47
	The "FG256" table for the AGL400 device is new.	4-54
	The "FG484" table for the AGL400 device is new.	4-64
Revision 10 (Aug 2008)	3.0 V LVCMOS wide range support data was added to Table 2-2 • Recommended Operating Conditions 1.	2-2
DC and Switching Characteristics Advance v0.4	3.3 V LVCMOS wide range support data was added to Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings to Table 2-27 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings.	2-24 to 2-26
	3.3 V LVCMOS wide range support data was added to Table 2-28 • Summary of Maximum and Minimum DC Input Levels.	2-27
	3.3 V LVCMOS wide range support text was added to Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range.	2-39