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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Obsolete  |
| Number of LABs/CLBs            | -   |
| Number of Logic Elements/Cells | 24576   |
| Total RAM Bits                 | 147456  |
| Number of I/O                  | 177   |
| Number of Gates                | 1000000   |
| Voltage - Supply               | 1.14V ~ 1.575V  |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 70°C (TA)   |
| Package / Case                 | 256-LBGA  |
| Supplier Device Package        | 256-FPBGA (17x17)   |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/microsemi/agl1000v2-fgg256t">https://www.e-xfl.com/product-detail/microsemi/agl1000v2-fgg256t</a> |

**Table 2-20 • Different Components Contributing to the Static Power Consumption in IGLOO Devices**  
**For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

| Parameter | Definition                                       | Device-Specific Static Power (mW)                            |        |        |        |        |        |        |        |
|-----------|--|--|--------|--------|--------|--------|--------|--------|--------|
|           |  | AGL1000  | AGL600 | AGL400 | AGL250 | AGL125 | AGL060 | AGL030 | AGL015 |
| PDC1      | Array static power in Active mode                | See Table 2-12 on page 2-9.                                  |        |        |        |        |        |        |        |
| PDC2      | Array static power in Static (Idle) mode         | See Table 2-11 on page 2-8.                                  |        |        |        |        |        |        |        |
| PDC3      | Array static power in Flash*Freeze mode          | See Table 2-9 on page 2-7.                                   |        |        |        |        |        |        |        |
| PDC4      | Static PLL contribution                          | 1.84   |        |        |        |        |        |        |        |
| PDC5      | Bank quiescent power ( $V_{CC1}$ -dependent)     | See Table 2-12 on page 2-9.                                  |        |        |        |        |        |        |        |
| PDC6      | I/O input pin static power (standard-dependent)  | See Table 2-13 on page 2-10 through Table 2-15 on page 2-11. |        |        |        |        |        |        |        |
| PDC7      | I/O output pin static power (standard-dependent) | See Table 2-16 on page 2-11 through Table 2-18 on page 2-12. |        |        |        |        |        |        |        |

*Note:* \*For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

**Combinatorial Cells Contribution— $P_{C-CELL}$** 

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**Routing Net Contribution— $P_{NET}$** 

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**I/O Input Buffer Contribution— $P_{INPUTS}$** 

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**I/O Output Buffer Contribution— $P_{OUTPUTS}$** 

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

$\beta_1$  is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

**RAM Contribution— $P_{MEMORY}$** 

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

$N_{BLOCKS}$  is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$  is the memory read clock frequency.

$\beta_2$  is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$  is the memory write clock frequency.

$\beta_3$  is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

**PLL Contribution— $P_{PLL}$** 

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

$F_{CLKOUT}$  is the output clock frequency.<sup>†</sup>

<sup>†</sup> If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ( $P_{AC13} * F_{CLKOUT}$  product) to the total PLL contribution.

**Table 2-75 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI} = 2.7$**   
**Applicable to Standard Plus Banks**

| Drive Strength    | Equivalent Software Default Drive Strength Option <sup>1</sup> | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 $\mu\text{A}$ | 2 mA   | Std.        | 1.55       | 6.69     | 0.26      | 1.32     | 1.10       | 6.69     | 5.73     | 3.41     | 3.72     | 12.48     | 11.52     | ns    |
| 100 $\mu\text{A}$ | 4 mA   | Std.        | 1.55       | 6.69     | 0.26      | 1.32     | 1.10       | 6.69     | 5.73     | 3.41     | 3.72     | 12.48     | 11.52     | ns    |
| 100 $\mu\text{A}$ | 6 mA   | Std.        | 1.55       | 5.58     | 0.26      | 1.32     | 1.10       | 5.58     | 5.01     | 3.77     | 4.35     | 11.36     | 10.79     | ns    |
| 100 $\mu\text{A}$ | 8 mA   | Std.        | 1.55       | 5.58     | 0.26      | 1.32     | 1.10       | 5.58     | 5.01     | 3.77     | 4.35     | 11.36     | 10.79     | ns    |
| 100 $\mu\text{A}$ | 12 mA  | Std.        | 1.55       | 4.82     | 0.26      | 1.32     | 1.10       | 4.82     | 4.44     | 4.02     | 4.76     | 10.61     | 10.23     | ns    |
| 100 $\mu\text{A}$ | 16 mA  | Std.        | 1.55       | 4.82     | 0.26      | 1.32     | 1.10       | 4.82     | 4.44     | 4.02     | 4.76     | 10.61     | 10.23     | ns    |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-76 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$ , Worst-Case  $V_{CCI} = 2.7$**   
**Applicable to Standard Plus Banks**

| Drive Strength    | Equivalent Software Default Drive Strength Option <sup>1</sup> | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|-------------------|--|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 100 $\mu\text{A}$ | 2 mA   | Std.        | 1.55       | 4.10     | 0.26      | 1.32     | 1.10       | 4.10     | 3.30     | 3.40     | 3.92     | 9.89      | 9.09      | ns    |
| 100 $\mu\text{A}$ | 4 mA   | Std.        | 1.55       | 4.10     | 0.26      | 1.32     | 1.10       | 4.10     | 3.30     | 3.40     | 3.92     | 9.89      | 9.09      | ns    |
| 100 $\mu\text{A}$ | 6 mA   | Std.        | 1.55       | 3.51     | 0.26      | 1.32     | 1.10       | 3.51     | 2.79     | 3.76     | 4.56     | 9.30      | 8.57      | ns    |
| 100 $\mu\text{A}$ | 8 mA   | Std.        | 1.55       | 3.51     | 0.26      | 1.32     | 1.10       | 3.51     | 2.79     | 3.76     | 4.56     | 9.30      | 8.57      | ns    |
| 100 $\mu\text{A}$ | 12 mA  | Std.        | 1.55       | 3.20     | 0.26      | 1.32     | 1.10       | 3.20     | 2.52     | 4.01     | 4.97     | 8.99      | 8.31      | ns    |
| 100 $\mu\text{A}$ | 16 mA  | Std.        | 1.55       | 3.20     | 0.26      | 1.32     | 1.10       | 3.20     | 2.52     | 4.01     | 4.97     | 8.99      | 8.31      | ns    |

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

**Table 2-107 • 1.8 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA           | Std.        | 1.55       | 6.32     | 0.26      | 1.11     | 1.10       | 6.43     | 5.81     | 2.47     | 2.16     | 12.22     | 11.60     | ns    |
| 4 mA           | Std.        | 1.55       | 5.27     | 0.26      | 1.11     | 1.10       | 5.35     | 5.01     | 2.78     | 2.92     | 11.14     | 10.79     | ns    |
| 6 mA           | Std.        | 1.55       | 4.56     | 0.26      | 1.11     | 1.10       | 4.64     | 4.44     | 3.00     | 3.30     | 10.42     | 10.22     | ns    |
| 8 mA           | Std.        | 1.55       | 4.56     | 0.26      | 1.11     | 1.10       | 4.64     | 4.44     | 3.00     | 3.30     | 10.42     | 10.22     | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-108 • 1.8 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-----------|-----------|-------|
| 2 mA           | Std.        | 1.55       | 3.22     | 0.26      | 1.11     | 1.10       | 3.26     | 3.18     | 2.47     | 2.20     | 9.05      | 8.97      | ns    |
| 4 mA           | Std.        | 1.55       | 2.72     | 0.26      | 1.11     | 1.10       | 2.75     | 2.50     | 2.78     | 3.01     | 8.54      | 8.29      | ns    |
| 6 mA           | Std.        | 1.55       | 2.43     | 0.26      | 1.11     | 1.10       | 2.47     | 2.16     | 2.99     | 3.39     | 8.25      | 7.94      | ns    |
| 8 mA           | Std.        | 1.55       | 2.43     | 0.26      | 1.11     | 1.10       | 2.47     | 2.16     | 2.99     | 3.39     | 8.25      | 7.94      | ns    |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-109 • 1.8 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA           | Std.        | 1.55       | 6.13     | 0.26      | 1.08     | 1.10       | 6.24     | 5.79     | 2.08     | 1.78     | ns    |
| 4 mA           | Std.        | 1.55       | 5.17     | 0.26      | 1.08     | 1.10       | 5.26     | 4.98     | 2.38     | 2.54     | ns    |

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-110 • 1.8 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|----------------|-------------|------------|----------|-----------|----------|------------|----------|----------|----------|----------|-------|
| 2 mA           | Std.        | 3.06       | 0.26     | 1.08      | 1.10     | 3.10       | 3.01     | 2.08     | 1.83     | 3.06     | ns    |
| 4 mA           | Std.        | 2.60       | 0.26     | 1.08      | 1.10     | 2.64       | 2.33     | 2.38     | 2.62     | 2.60     | ns    |

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

**Table 2-127 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

| 1.2 V LVCMOS   | VIL    |             | VIH         |        | VOL         | VOH         | IOL | IOH | IOSH                 | IOSL                 | IIL <sup>1</sup> | IIH <sup>2</sup> |
|----------------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V      | Min. V      | Max. V | Max. V      | Min. V      | mA  | mA  | Max. mA <sup>3</sup> | Max. mA <sup>3</sup> | μA <sup>4</sup>  | μA <sup>4</sup>  |
| 2 mA           | −0.3   | 0.35 * VCCI | 0.65 * VCCI | 1.26   | 0.25 * VCCI | 0.75 * VCCI | 2   | 2   | 20                   | 26                   | 10               | 10               |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-128 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

| 1.2 V LVCMOS   | VIL    |             | VIH         |        | VOL         | VOH         | IOL | IOH | IOSH                 | IOSL                 | IIL <sup>1</sup> | IIH <sup>2</sup> |
|----------------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V      | Min. V      | Max. V | Max. V      | Min. V      | mA  | mA  | Max. mA <sup>3</sup> | Max. mA <sup>3</sup> | μA <sup>4</sup>  | μA <sup>4</sup>  |
| 2 mA           | −0.3   | 0.35 * VCCI | 0.65 * VCCI | 1.26   | 0.25 * VCCI | 0.75 * VCCI | 2   | 2   | 20                   | 26                   | 10               | 10               |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

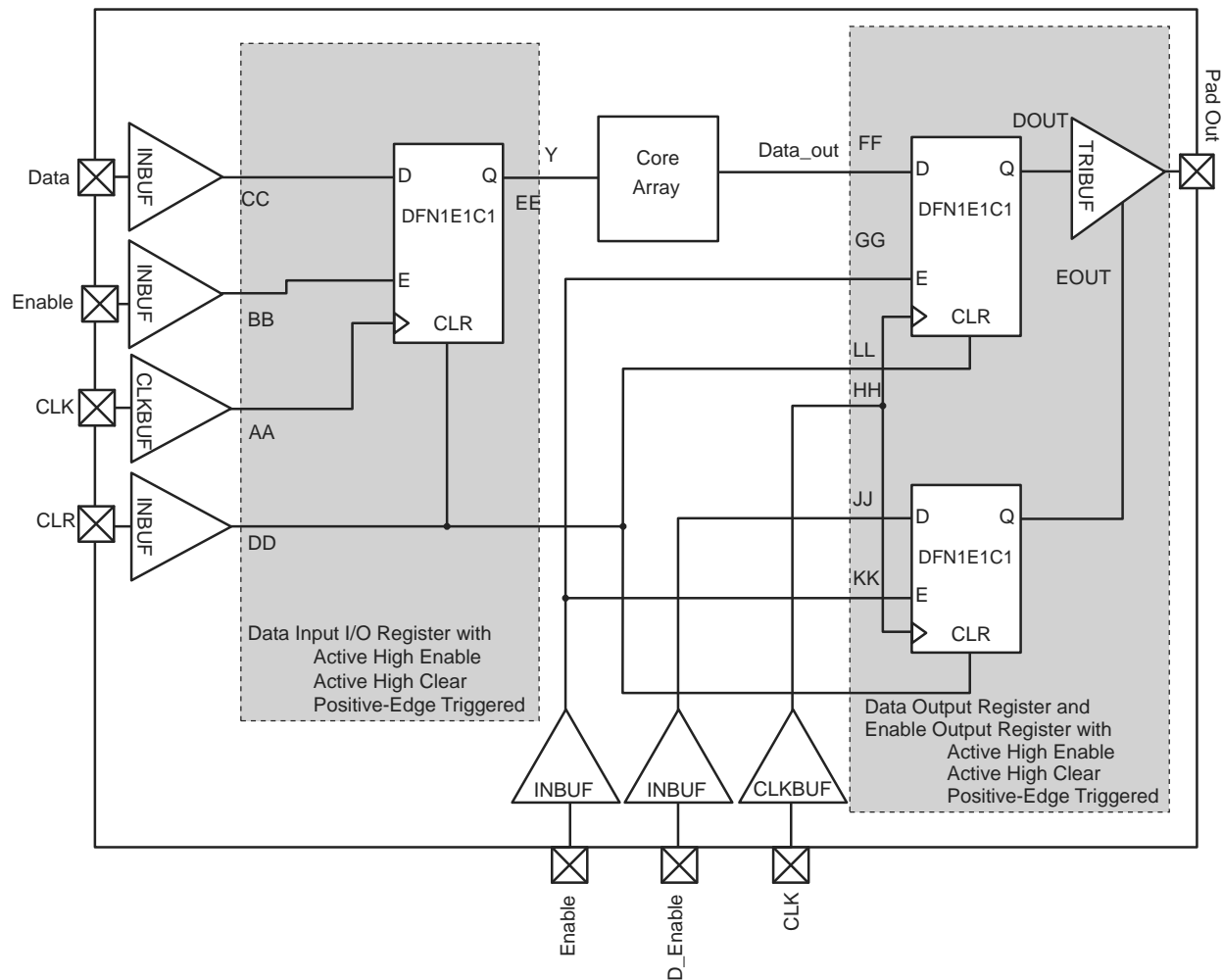
**Table 2-129 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard I/O Banks

| 1.2 V LVCMOS   | VIL    |             | VIH         |        | VOL         | VOH         | IOL | IOH | IOSH                 | IOSL                 | IIL <sup>1</sup> | IIH <sup>2</sup> |
|----------------|--------|-------------|-------------|--------|-------------|-------------|-----|-----|----------------------|----------------------|------------------|------------------|
| Drive Strength | Min. V | Max. V      | Min. V      | Max. V | Max. V      | Min. V      | mA  | mA  | Max. mA <sup>3</sup> | Max. mA <sup>3</sup> | μA <sup>4</sup>  | μA <sup>4</sup>  |
| 1 mA           | −0.3   | 0.35 * VCCI | 0.65 * VCCI | 3.6    | 0.25 * VCCI | 0.75 * VCCI | 1   | 1   | 20                   | 26                   | 10               | 10               |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**



**Figure 2-17 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

**Table 2-175 • AGL060 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

| Parameter     | Description                               | Std.              |                   | Units |
|---------------|---|-------------------|-------------------|-------|
|               |   | Min. <sup>1</sup> | Max. <sup>2</sup> |       |
| $t_{RCKL}$    | Input Low Delay for Global Clock          | 1.33              | 1.55              | ns    |
| $t_{RCKH}$    | Input High Delay for Global Clock         | 1.35              | 1.62              | ns    |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18              |                   | ns    |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock  | 1.15              |                   | ns    |
| $t_{RCKSW}$   | Maximum Skew for Global Clock             |                   | 0.27              | ns    |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-176 • AGL125 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

| Parameter     | Description                               | Std.              |                   | Units |
|---------------|---|-------------------|-------------------|-------|
|               |   | Min. <sup>1</sup> | Max. <sup>2</sup> |       |
| $t_{RCKL}$    | Input Low Delay for Global Clock          | 1.36              | 1.71              | ns    |
| $t_{RCKH}$    | Input High Delay for Global Clock         | 1.39              | 1.82              | ns    |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.18              |                   | ns    |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock  | 1.15              |                   | ns    |
| $t_{RCKSW}$   | Maximum Skew for Global Clock             |                   | 0.43              | ns    |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.



**Table 2-187 • AGL600 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$** 

| Parameter            | Description                               | Std.              |                   | Units |
|----------------------|---|-------------------|-------------------|-------|
|                      |   | Min. <sup>1</sup> | Max. <sup>2</sup> |       |
| $t_{\text{RCKL}}$    | Input Low Delay for Global Clock          | 2.22              | 2.67              | ns    |
| $t_{\text{RCKH}}$    | Input High Delay for Global Clock         | 2.32              | 2.93              | ns    |
| $t_{\text{RCKMPWH}}$ | Minimum Pulse Width High for Global Clock | 1.40              |                   | ns    |
| $t_{\text{RCKMPWL}}$ | Minimum Pulse Width Low for Global Clock  | 1.65              |                   | ns    |
| $t_{\text{RCKSW}}$   | Maximum Skew for Global Clock             |                   | 0.61              | ns    |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-188 • AGL1000 Global Resource****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$** 

| Parameter            | Description                               | Std.              |                   | Units |
|----------------------|---|-------------------|-------------------|-------|
|                      |   | Min. <sup>1</sup> | Max. <sup>2</sup> |       |
| $t_{\text{RCKL}}$    | Input Low Delay for Global Clock          | 2.31              | 2.76              | ns    |
| $t_{\text{RCKH}}$    | Input High Delay for Global Clock         | 2.42              | 3.03              | ns    |
| $t_{\text{RCKMPWH}}$ | Minimum Pulse Width High for Global Clock | 1.40              |                   | ns    |
| $t_{\text{RCKMPWL}}$ | Minimum Pulse Width Low for Global Clock  | 1.65              |                   | ns    |
| $t_{\text{RCKSW}}$   | Maximum Skew for Global Clock             |                   | 0.61              | ns    |

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**VJTAG****JTAG Supply Voltage**

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

**VPUMP****Programming Supply Voltage**

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01  $\mu$ F and 0.33  $\mu$ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User Pins

**I/O****User Input/Output**

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

**GL****Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

**FF****Flash\*Freeze Mode Activation Pin**

Flash\*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash\*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash\*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash\*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash\*Freeze mode. While in Flash\*Freeze mode, the Flash\*Freeze pin should be constantly asserted.

## JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500  $\Omega$  to 1 k $\Omega$  will satisfy the requirements. Refer to Table 3-2 for more information.

**Table 3-2 • Recommended Tie-Off Values for the TCK and TRST Pins**

| VJTAG          | Tie-Off Resistance <sup>1,2</sup> |
|----------------|-----------------------------------|
| VJTAG at 3.3 V | 200 $\Omega$ to 1 k $\Omega$      |
| VJTAG at 2.5 V | 200 $\Omega$ to 1 k $\Omega$      |
| VJTAG at 1.8 V | 500 $\Omega$ to 1 k $\Omega$      |
| VJTAG at 1.5 V | 500 $\Omega$ to 1 k $\Omega$      |

Notes:

1. The TCK pin can be pulled-up or pulled-down.
2. The TRST pin is pulled-down.
3. Equivalent parallel resistance if more than one device is on the JTAG chain

**Table 3-3 • TRST and TCK Pull-Down Recommendations**

| VJTAG          | Tie-Off Resistance*          |
|----------------|------------------------------|
| VJTAG at 3.3 V | 200 $\Omega$ to 1 k $\Omega$ |
| VJTAG at 2.5 V | 200 $\Omega$ to 1 k $\Omega$ |
| VJTAG at 1.8 V | 500 $\Omega$ to 1 k $\Omega$ |
| VJTAG at 1.5 V | 500 $\Omega$ to 1 k $\Omega$ |

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

### TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

### TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

### TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

### TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

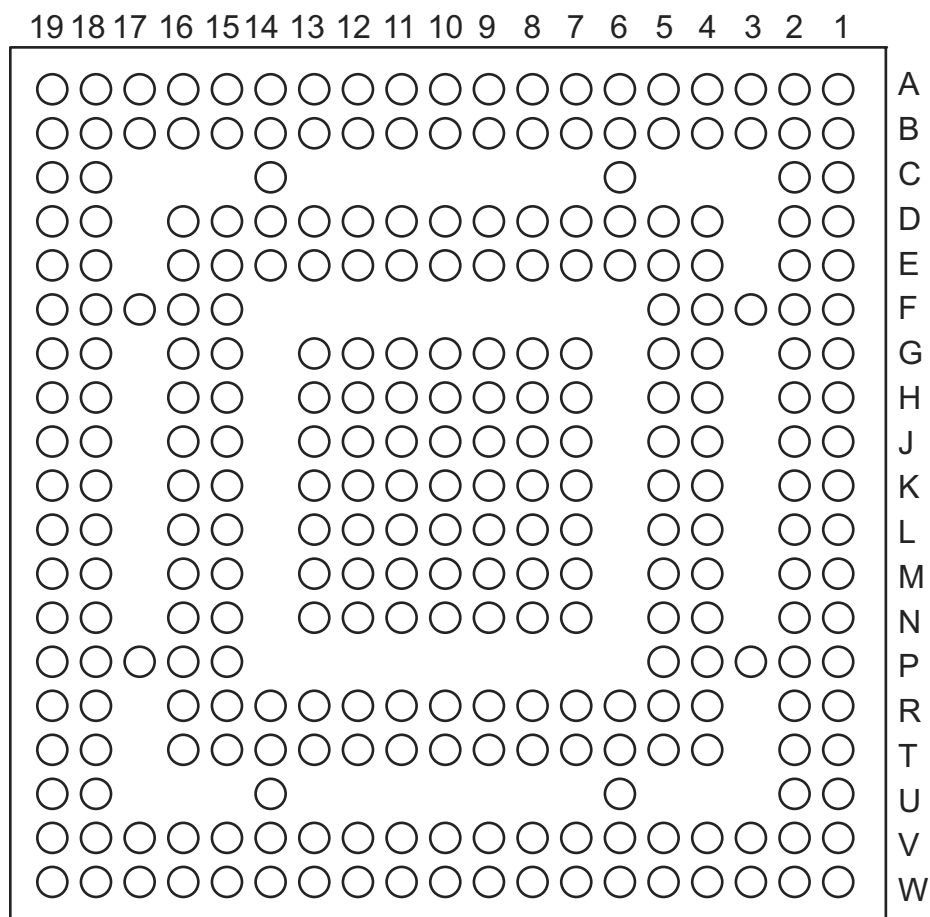
In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

| CS196      |                 |
|------------|-----------------|
| Pin Number | AGL400 Function |
| A1         | GND             |
| A2         | GAA0/IO00RSB0   |
| A3         | GAC0/IO04RSB0   |
| A4         | GAC1/IO05RSB0   |
| A5         | IO14RSB0        |
| A6         | IO18RSB0        |
| A7         | IO26RSB0        |
| A8         | IO29RSB0        |
| A9         | IO36RSB0        |
| A10        | GBC0/IO54RSB0   |
| A11        | GBB0/IO56RSB0   |
| A12        | GBB1/IO57RSB0   |
| A13        | GBA1/IO59RSB0   |
| A14        | GND             |
| B1         | VCCIB3          |
| B2         | VMV0            |
| B2         | VMV0            |
| B3         | GAA1/IO01RSB0   |
| B4         | GAB1/IO03RSB0   |
| B5         | GND             |
| B6         | IO17RSB0        |
| B7         | IO25RSB0        |
| B8         | IO34RSB0        |
| B9         | IO39RSB0        |
| B10        | GND             |
| B11        | GBC1/IO55RSB0   |
| B12        | GBA0/IO58RSB0   |
| B13        | GBA2/IO60PPB1   |
| B14        | GBB2/IO61PDB1   |
| C1         | GAC2/IO153UDB3  |
| C2         | GAB2/IO154UDB3  |
| C3         | GNDQ            |
| C4         | VCCIB0          |
| C5         | GAB0/IO02RSB0   |
| C6         | IO15RSB0        |
| C7         | VCCIB0          |

| CS196      |                 |
|------------|-----------------|
| Pin Number | AGL400 Function |
| C8         | IO31RSB0        |
| C9         | IO44RSB0        |
| C10        | IO49RSB0        |
| C11        | VCCIB0          |
| C12        | IO60NPB1        |
| C13        | GNDQ            |
| C14        | IO61NDB1        |
| D1         | IO153VDB3       |
| D2         | IO154VDB3       |
| D3         | GAA2/IO155UDB3  |
| D4         | IO150PPB3       |
| D5         | IO11RSB0        |
| D6         | IO20RSB0        |
| D7         | IO23RSB0        |
| D8         | IO28RSB0        |
| D9         | IO41RSB0        |
| D10        | IO47RSB0        |
| D11        | IO63PPB1        |
| D12        | VMV1            |
| D13        | IO62NDB1        |
| D14        | GBC2/IO62PDB1   |
| E1         | IO149PDB3       |
| E2         | GND             |
| E3         | IO155VDB3       |
| E4         | VCCIB3          |
| E5         | IO151USB3       |
| E6         | IO09RSB0        |
| E7         | IO12RSB0        |
| E8         | IO32RSB0        |
| E9         | IO46RSB0        |
| E10        | IO51RSB0        |
| E11        | VCCIB1          |
| E12        | IO63NPB1        |
| E13        | GND             |
| E14        | IO64PDB1        |
| F1         | IO149NDB3       |

| CS196      |                 |
|------------|-----------------|
| Pin Number | AGL400 Function |
| F2         | IO144NPB3       |
| F3         | IO148PDB3       |
| F4         | IO148NDB3       |
| F5         | IO150NPB3       |
| F6         | IO07RSB0        |
| F7         | VCC             |
| F8         | VCC             |
| F9         | IO43RSB0        |
| F10        | IO73PDB1        |
| F11        | IO73NDB1        |
| F12        | IO66NDB1        |
| F13        | IO66PDB1        |
| F14        | IO64NDB1        |
| G1         | GFB1/IO146PDB3  |
| G2         | GFA0/IO145NDB3  |
| G3         | GFA2/IO144PPB3  |
| G4         | VCOMPLF         |
| G5         | GFC0/IO147NDB3  |
| G6         | VCC             |
| G7         | GND             |
| G8         | GND             |
| G9         | VCC             |
| G10        | GCC0/IO67NDB1   |
| G11        | GCB1/IO68PDB1   |
| G12        | GCA0/IO69NDB1   |
| G13        | IO72NDB1        |
| G14        | GCC2/IO72PDB1   |
| H1         | GFB0/IO146NDB3  |
| H2         | GFA1/IO145PDB3  |
| H3         | VCCPLF          |
| H4         | GFB2/IO143PPB3  |
| H5         | GFC1/IO147PDB3  |
| H6         | VCC             |
| H7         | GND             |
| H8         | GND             |
| H9         | VCC             |

## CS281



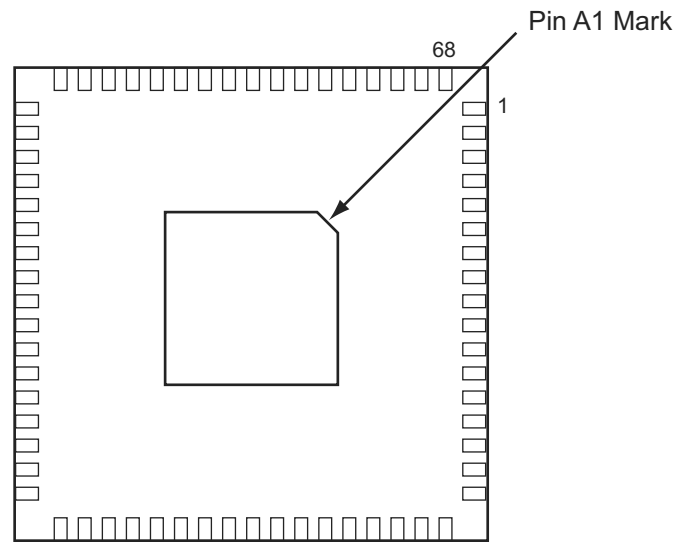
*Note: This is the bottom view of the package.*

### **Note**

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

## QN68

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*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

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**Note**

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| <b>QN132</b>      |                        |
|-------------------|------------------------|
| <b>Pin Number</b> | <b>AGL250 Function</b> |
| C17               | IO74RSB2               |
| C18               | VCCIB2                 |
| C19               | TCK                    |
| C20               | VMV2                   |
| C21               | VPUMP                  |
| C22               | VJTAG                  |
| C23               | VCCIB1                 |
| C24               | IO53NSB1               |
| C25               | IO51NPB1               |
| C26               | GCA1/IO50PPB1          |
| C27               | GCC0/IO48NDB1          |
| C28               | VCCIB1                 |
| C29               | IO42NDB1               |
| C30               | GNDQ                   |
| C31               | GBA1/IO40RSB0          |
| C32               | GBB0/IO37RSB0          |
| C33               | VCC                    |
| C34               | IO24RSB0               |
| C35               | IO19RSB0               |
| C36               | IO16RSB0               |
| C37               | IO10RSB0               |
| C38               | VCCIB0                 |
| C39               | GAB1/IO03RSB0          |
| C40               | VMV0                   |
| D1                | GND                    |
| D2                | GND                    |
| D3                | GND                    |
| D4                | GND                    |

| FG144      |                 |
|------------|-----------------|
| Pin Number | AGL125 Function |
| A1         | GNDQ            |
| A2         | VMV0            |
| A3         | GAB0/IO02RSB0   |
| A4         | GAB1/IO03RSB0   |
| A5         | IO11RSB0        |
| A6         | GND             |
| A7         | IO18RSB0        |
| A8         | VCC             |
| A9         | IO25RSB0        |
| A10        | GBA0/IO39RSB0   |
| A11        | GBA1/IO40RSB0   |
| A12        | GNDQ            |
| B1         | GAB2/IO69RSB1   |
| B2         | GND             |
| B3         | GAA0/IO00RSB0   |
| B4         | GAA1/IO01RSB0   |
| B5         | IO08RSB0        |
| B6         | IO14RSB0        |
| B7         | IO19RSB0        |
| B8         | IO22RSB0        |
| B9         | GBB0/IO37RSB0   |
| B10        | GBB1/IO38RSB0   |
| B11        | GND             |
| B12        | VMV0            |
| C1         | IO132RSB1       |
| C2         | GFA2/IO120RSB1  |
| C3         | GAC2/IO131RSB1  |
| C4         | VCC             |
| C5         | IO10RSB0        |
| C6         | IO12RSB0        |
| C7         | IO21RSB0        |
| C8         | IO24RSB0        |
| C9         | IO27RSB0        |
| C10        | GBA2/IO41RSB0   |
| C11        | IO42RSB0        |
| C12        | GBC2/IO45RSB0   |

| FG144      |                 |
|------------|-----------------|
| Pin Number | AGL125 Function |
| D1         | IO128RSB1       |
| D2         | IO129RSB1       |
| D3         | IO130RSB1       |
| D4         | GAA2/IO67RSB1   |
| D5         | GAC0/IO04RSB0   |
| D6         | GAC1/IO05RSB0   |
| D7         | GBC0/IO35RSB0   |
| D8         | GBC1/IO36RSB0   |
| D9         | GBB2/IO43RSB0   |
| D10        | IO28RSB0        |
| D11        | IO44RSB0        |
| D12        | GCB1/IO53RSB0   |
| E1         | VCC             |
| E2         | GFC0/IO125RSB1  |
| E3         | GFC1/IO126RSB1  |
| E4         | VCCIB1          |
| E5         | IO68RSB1        |
| E6         | VCCIB0          |
| E7         | VCCIB0          |
| E8         | GCC1/IO51RSB0   |
| E9         | VCCIB0          |
| E10        | VCC             |
| E11        | GCA0/IO56RSB0   |
| E12        | IO46RSB0        |
| F1         | GFB0/IO123RSB1  |
| F2         | VCOMPLF         |
| F3         | GFB1/IO124RSB1  |
| F4         | IO127RSB1       |
| F5         | GND             |
| F6         | GND             |
| F7         | GND             |
| F8         | GCC0/IO52RSB0   |
| F9         | GCB0/IO54RSB0   |
| F10        | GND             |
| F11        | GCA1/IO55RSB0   |
| F12        | GCA2/IO57RSB0   |

| FG144      |                 |
|------------|-----------------|
| Pin Number | AGL125 Function |
| G1         | GFA1/IO121RSB1  |
| G2         | GND             |
| G3         | VCCPLF          |
| G4         | GFA0/IO122RSB1  |
| G5         | GND             |
| G6         | GND             |
| G7         | GND             |
| G8         | GDC1/IO61RSB0   |
| G9         | IO48RSB0        |
| G10        | GCC2/IO59RSB0   |
| G11        | IO47RSB0        |
| G12        | GCB2/IO58RSB0   |
| H1         | VCC             |
| H2         | GFB2/IO119RSB1  |
| H3         | GFC2/IO118RSB1  |
| H4         | GEC1/IO112RSB1  |
| H5         | VCC             |
| H6         | IO50RSB0        |
| H7         | IO60RSB0        |
| H8         | GDB2/IO71RSB1   |
| H9         | GDC0/IO62RSB0   |
| H10        | VCCIB0          |
| H11        | IO49RSB0        |
| H12        | VCC             |
| J1         | GEB1/IO110RSB1  |
| J2         | IO115RSB1       |
| J3         | VCCIB1          |
| J4         | GEC0/IO111RSB1  |
| J5         | IO116RSB1       |
| J6         | IO117RSB1       |
| J7         | VCC             |
| J8         | TCK             |
| J9         | GDA2/IO70RSB1   |
| J10        | TDO             |
| J11        | GDA1/IO65RSB0   |
| J12        | GDB1/IO63RSB0   |



| <b>FG144</b>      |                        |
|-------------------|------------------------|
| <b>Pin Number</b> | <b>AGL600 Function</b> |
| K1                | GEB0/IO145NDB3         |
| K2                | GEA1/IO144PDB3         |
| K3                | GEA0/IO144NDB3         |
| K4                | GEA2/IO143RSB2         |
| K5                | IO119RSB2              |
| K6                | IO111RSB2              |
| K7                | GND                    |
| K8                | IO94RSB2               |
| K9                | GDC2/IO91RSB2          |
| K10               | GND                    |
| K11               | GDA0/IO88NDB1          |
| K12               | GDB0/IO87NDB1          |
| L1                | GND                    |
| L2                | VMV3                   |
| L3                | FF/GEB2/IO142RSB2      |
| L4                | IO136RSB2              |
| L5                | VCCIB2                 |
| L6                | IO115RSB2              |
| L7                | IO103RSB2              |
| L8                | IO97RSB2               |
| L9                | TMS                    |
| L10               | VJTAG                  |
| L11               | VMV2                   |
| L12               | TRST                   |
| M1                | GNDQ                   |
| M2                | GEC2/IO141RSB2         |
| M3                | IO138RSB2              |
| M4                | IO123RSB2              |
| M5                | IO126RSB2              |
| M6                | IO134RSB2              |
| M7                | IO108RSB2              |
| M8                | IO99RSB2               |
| M9                | TDI                    |
| M10               | VCCIB2                 |
| M11               | VPUMP                  |
| M12               | GNDQ                   |

| <b>FG484</b>      |                        |
|-------------------|------------------------|
| <b>Pin Number</b> | <b>AGL400 Function</b> |
| V15               | IO85RSB2               |
| V16               | GDB2/IO81RSB2          |
| V17               | TDI                    |
| V18               | NC                     |
| V19               | TDO                    |
| V20               | GND                    |
| V21               | NC                     |
| V22               | NC                     |
| W1                | NC                     |
| W2                | NC                     |
| W3                | NC                     |
| W4                | GND                    |
| W5                | IO126RSB2              |
| W6                | FF/GEB2/IO133RSB2      |
| W7                | IO124RSB2              |
| W8                | IO116RSB2              |
| W9                | IO113RSB2              |
| W10               | IO107RSB2              |
| W11               | IO105RSB2              |
| W12               | IO102RSB2              |
| W13               | IO97RSB2               |
| W14               | IO92RSB2               |
| W15               | GDC2/IO82RSB2          |
| W16               | IO86RSB2               |
| W17               | GDA2/IO80RSB2          |
| W18               | TMS                    |
| W19               | GND                    |
| W20               | NC                     |
| W21               | NC                     |
| W22               | NC                     |
| Y1                | VCCIB3                 |
| Y2                | NC                     |
| Y3                | NC                     |
| Y4                | NC                     |
| Y5                | GND                    |
| Y6                | NC                     |

| FG484      |                 |
|------------|-----------------|
| Pin Number | AGL600 Function |
| A1         | GND             |
| A2         | GND             |
| A3         | VCCIB0          |
| A4         | NC              |
| A5         | NC              |
| A6         | IO09RSB0        |
| A7         | IO15RSB0        |
| A8         | NC              |
| A9         | NC              |
| A10        | IO22RSB0        |
| A11        | IO23RSB0        |
| A12        | IO29RSB0        |
| A13        | IO35RSB0        |
| A14        | NC              |
| A15        | NC              |
| A16        | IO46RSB0        |
| A17        | IO48RSB0        |
| A18        | NC              |
| A19        | NC              |
| A20        | VCCIB0          |
| A21        | GND             |
| A22        | GND             |
| AA1        | GND             |
| AA2        | VCCIB3          |
| AA3        | NC              |
| AA4        | NC              |
| AA5        | NC              |
| AA6        | IO135RSB2       |
| AA7        | IO133RSB2       |
| AA8        | NC              |
| AA9        | NC              |
| AA10       | NC              |
| AA11       | NC              |
| AA12       | NC              |
| AA13       | NC              |
| AA14       | NC              |

| FG484      |                 |
|------------|-----------------|
| Pin Number | AGL600 Function |
| AA15       | NC              |
| AA16       | IO101RSB2       |
| AA17       | NC              |
| AA18       | NC              |
| AA19       | NC              |
| AA20       | NC              |
| AA21       | VCCIB1          |
| AA22       | GND             |
| AB1        | GND             |
| AB2        | GND             |
| AB3        | VCCIB2          |
| AB4        | NC              |
| AB5        | NC              |
| AB6        | IO130RSB2       |
| AB7        | IO128RSB2       |
| AB8        | IO122RSB2       |
| AB9        | IO116RSB2       |
| AB10       | NC              |
| AB11       | NC              |
| AB12       | IO113RSB2       |
| AB13       | IO112RSB2       |
| AB14       | NC              |
| AB15       | NC              |
| AB16       | IO100RSB2       |
| AB17       | IO95RSB2        |
| AB18       | NC              |
| AB19       | NC              |
| AB20       | VCCIB2          |
| AB21       | GND             |
| AB22       | GND             |
| B1         | GND             |
| B2         | VCCIB3          |
| B3         | NC              |
| B4         | NC              |
| B5         | NC              |
| B6         | IO08RSB0        |

| FG484      |                 |
|------------|-----------------|
| Pin Number | AGL600 Function |
| B7         | IO12RSB0        |
| B8         | NC              |
| B9         | NC              |
| B10        | IO17RSB0        |
| B11        | NC              |
| B12        | NC              |
| B13        | IO36RSB0        |
| B14        | NC              |
| B15        | NC              |
| B16        | IO47RSB0        |
| B17        | IO49RSB0        |
| B18        | NC              |
| B19        | NC              |
| B20        | NC              |
| B21        | VCCIB1          |
| B22        | GND             |
| C1         | VCCIB3          |
| C2         | NC              |
| C3         | NC              |
| C4         | NC              |
| C5         | GND             |
| C6         | NC              |
| C7         | NC              |
| C8         | VCC             |
| C9         | VCC             |
| C10        | NC              |
| C11        | NC              |
| C12        | NC              |
| C13        | NC              |
| C14        | VCC             |
| C15        | VCC             |
| C16        | NC              |
| C17        | NC              |
| C18        | GND             |
| C19        | NC              |
| C20        | NC              |

| <b>FG484</b>      |                        |
|-------------------|------------------------|
| <b>Pin Number</b> | <b>AGL600 Function</b> |
| G5                | IO171PDB3              |
| G6                | GAC2/IO172PDB3         |
| G7                | IO06RSB0               |
| G8                | GNDQ                   |
| G9                | IO10RSB0               |
| G10               | IO19RSB0               |
| G11               | IO26RSB0               |
| G12               | IO30RSB0               |
| G13               | IO40RSB0               |
| G14               | IO45RSB0               |
| G15               | GNDQ                   |
| G16               | IO50RSB0               |
| G17               | GBB2/IO61PPB1          |
| G18               | IO53RSB0               |
| G19               | IO63NDB1               |
| G20               | NC                     |
| G21               | NC                     |
| G22               | NC                     |
| H1                | NC                     |
| H2                | NC                     |
| H3                | VCC                    |
| H4                | IO166PDB3              |
| H5                | IO167NPB3              |
| H6                | IO172NDB3              |
| H7                | IO169NDB3              |
| H8                | VMV0                   |
| H9                | VCCIB0                 |
| H10               | VCCIB0                 |
| H11               | IO25RSB0               |
| H12               | IO31RSB0               |
| H13               | VCCIB0                 |
| H14               | VCCIB0                 |
| H15               | VMV1                   |
| H16               | GBC2/IO62PDB1          |
| H17               | IO67PPB1               |
| H18               | IO64PPB1               |

| <b>FG484</b>      |                         |
|-------------------|-------------------------|
| <b>Pin Number</b> | <b>AGL1000 Function</b> |
| R9                | VCCIB2                  |
| R10               | VCCIB2                  |
| R11               | IO147RSB2               |
| R12               | IO136RSB2               |
| R13               | VCCIB2                  |
| R14               | VCCIB2                  |
| R15               | VMV2                    |
| R16               | IO110NDB1               |
| R17               | GDB1/IO112PPB1          |
| R18               | GDC1/IO111PDB1          |
| R19               | IO107NDB1               |
| R20               | VCC                     |
| R21               | IO104NDB1               |
| R22               | IO105PDB1               |
| T1                | IO198PDB3               |
| T2                | IO198NDB3               |
| T3                | NC                      |
| T4                | IO194PPB3               |
| T5                | IO192PPB3               |
| T6                | GEC1/IO190PPB3          |
| T7                | IO192NPB3               |
| T8                | GNDQ                    |
| T9                | GEA2/IO187RSB2          |
| T10               | IO161RSB2               |
| T11               | IO155RSB2               |
| T12               | IO141RSB2               |
| T13               | IO129RSB2               |
| T14               | IO124RSB2               |
| T15               | GNDQ                    |
| T16               | IO110PDB1               |
| T17               | VJTAG                   |
| T18               | GDC0/IO111NDB1          |
| T19               | GDA1/IO113PDB1          |
| T20               | NC                      |
| T21               | IO108PDB1               |
| T22               | IO105NDB1               |