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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	71
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl125v2-vqg100t

I/Os Per Package¹

IGLOO Devices	AGL015 ²	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250				M1AGL600		M1AGL1000	
Package	I/O Type ³											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs
QN48	–	34	–	–	–	–	–	–	–	–	–	–
QN68	49	49	–	–	–	–	–	–	–	–	–	–
UC81	–	66	–	–	–	–	–	–	–	–	–	–
CS81	–	66	–	–	–	–	–	–	–	–	–	–
CS121	–	–	96	96	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–	–	–	–	–
QN132 ⁶	–	81	80	84	–	–	–	–	–	–	–	–
CS196	–	–	–	133	143 ⁵	35 ⁵	143	35	–	–	–	–
FG144	–	–	–	97	97	24	97	25	97	25	97	25
FG256 ⁷	–	–	–	–	–	–	178	38	177	43	177	44
CS281	–	–	–	–	–	–	–	–	215	53	215	53
FG484 ⁷	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

- When considering migrating your design to a lower- or higher-density device, refer to the IGLOO FPGA Fabric User Guide to ensure compliance with design and board migration requirements.
- AGL015 is not recommended for new designs.
- When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.
- Each used differential I/O pair reduces the number of single-ended I/Os available by two.
- The M1AGL250 device does not support QN132 or CS196 packages.
- Package not available.
- FG256 and FG484 are footprint-compatible packages.

Table 1 • IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23
Nominal Area (mm ²)	16	25	36	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

Note: * Package not available.

field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC[®] family of third-generation-architecture flash FPGAs.

[†] The AGL015 and AGL030 do not support PLL or SRAM.

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$)
For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.500	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$)
For IGLOO V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.967	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.874	0.885	0.894	0.899	0.902
1.26	0.794	0.803	0.814	0.821	0.827	0.830

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (V_{CC} , V_{CCI} , and V_{JTAG}), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • Power Supply State per Mode

Modes/power supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0 V

Table 2-9 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	4	8	13	20	27	30	44	μA
	1.5 V	6	6	10	18	34	51	72	127	μA

Note: * I_{DD} includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min.V	Max. V	Min. V	Max.V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS ⁴	2 mA	2 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	2 mA	High	−0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI − 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI $\geq$ VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

Timing Characteristics***Applies to 1.5 V DC Core Voltage***

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

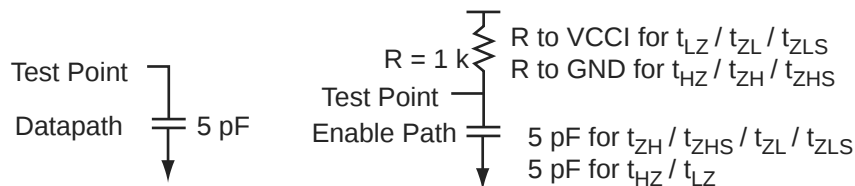
Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-53 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Figure 2-11 • AC Loading****Table 2-130 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-131 • 1.2 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-132 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-133 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-134 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-141 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced and Standard Plus I/Os

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										10	10

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-12.

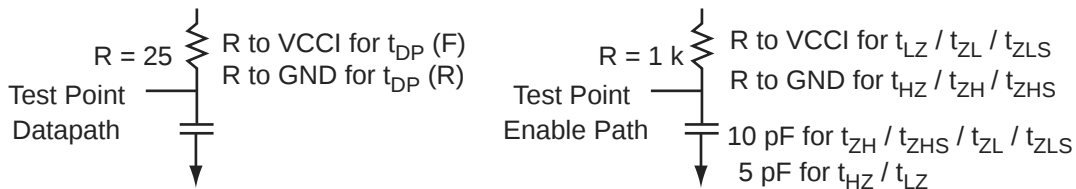


Figure 2-12 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-142.

Table 2-142 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	0.285 * VCCI for t _{DP(R)} 0.615 * VCCI for t _{DP(F)}	10

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-143 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-144 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

Table 2-189 • IGLOO CCC/PLL Specification
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		360 ³		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL ^{4, 5}			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
Acquisition Time				
LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁶				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.469		15.65	ns
Delay Range in Block: Fixed Delay ^{1, 2}		3.5		ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Jitter Data ⁷			
	SSO $\geq 4^8$	SSO $\geq 8^8$	SSO $\geq 16^8$	
0.75 MHz to 50 MHz	0.60%	0.80%	1.20%	
50 MHz to 160 MHz	4.00%	6.00%	12.00%	

Notes:

1. This delay is a function of voltage and temperature. See Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help associated with the core for more information.
4. The AGL030 device does not support a PLL.
5. Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
6. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
7. Measurements done with LVTTTL 3.3 V, 8 mA I/O drive strength, and high slew Rate. $V_{CC}/V_{CCPLL} = 1.14\text{ V}$, VQ/PQ/TQ type of packages, 20 pF load.
8. Simultaneously Switching Outputs (SSOs) are outputs that are synchronous to a single clock domain and have clock-to-out times that are within $\pm 200\text{ ps}$ of each other. Switching I/Os are placed outside of the PLL bank. Refer to the "Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout" section in the IGLOO FPGA Fabric User Guide.

JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 3-2 for more information.

Table 3-2 • Recommended Tie-Off Values for the TCK and TRST Pins

VJTAG	Tie-Off Resistance ^{1,2}
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Notes:

1. The TCK pin can be pulled-up or pulled-down.
2. The TRST pin is pulled-down.
3. Equivalent parallel resistance if more than one device is on the JTAG chain

Table 3-3 • TRST and TCK Pull-Down Recommendations

VJTAG	Tie-Off Resistance*
VJTAG at 3.3 V	200 Ω to 1 k Ω
VJTAG at 2.5 V	200 Ω to 1 k Ω
VJTAG at 1.8 V	500 Ω to 1 k Ω
VJTAG at 1.5 V	500 Ω to 1 k Ω

Note: Equivalent parallel resistance if more than one device is on the JTAG chain

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

CS81	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

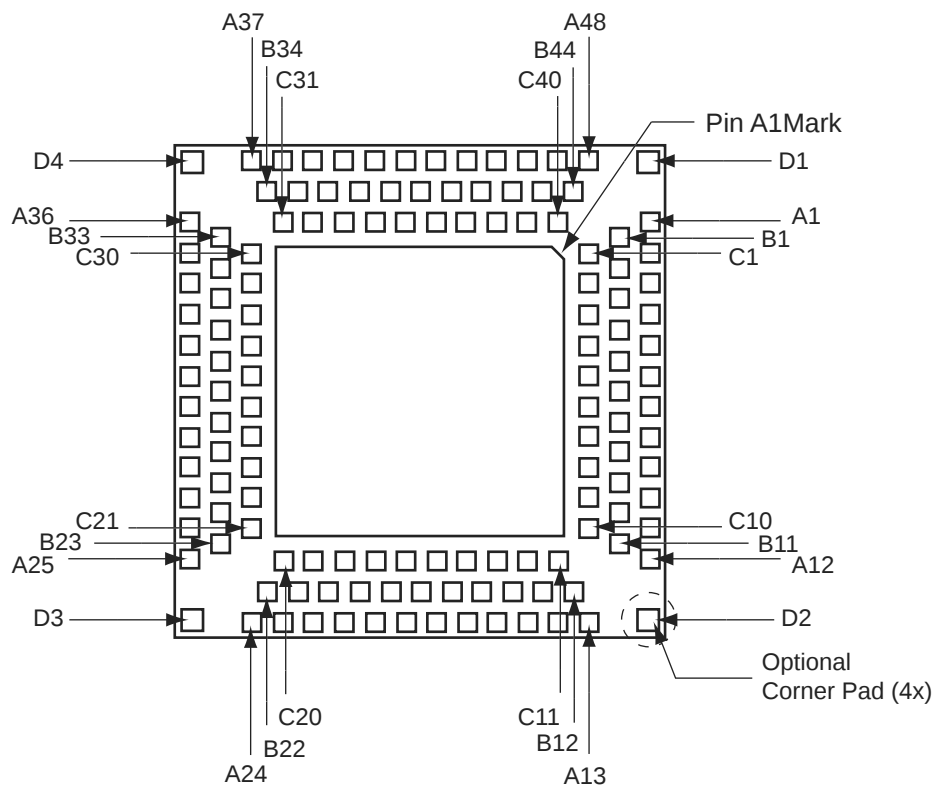
CS81	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

CS81	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS281	
Pin Number	AGL1000 Function
R15	IO122RSB2
R16	GDA1/IO113PPB1
R18	GDB0/IO112NPB1
R19	GDC0/IO111NPB1
T1	IO197PPB3
T2	GEC0/IO190NPB3
T4	GEB0/IO189NPB3
T5	IO181RSB2
T6	IO172RSB2
T7	IO171RSB2
T8	IO156RSB2
T9	IO159RSB2
T10	GND
T11	IO139RSB2
T12	IO138RSB2
T13	IO129RSB2
T14	IO123RSB2
T15	GDC2/IO116RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO112PPB1
U1	IO193PDB3
U2	GEA1/IO188PPB3
U6	IO167RSB2
U14	IO128RSB2
U18	TRST
U19	GDA0/IO113NPB1
V1	IO193NDB3
V2	VCCIB3
V3	GEC2/IO185RSB2
V4	IO182RSB2
V5	IO175RSB2
V6	GND
V7	IO161RSB2
V8	IO143RSB2
V9	IO146RSB2

CS281	
Pin Number	AGL1000 Function
V10	IO145RSB2
V11	IO144RSB2
V12	IO134RSB2
V13	IO133RSB2
V14	GND
V15	IO119RSB2
V16	GDA2/IO114RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO186RSB2
W3	IO183RSB2
W4	IO176RSB2
W5	IO170RSB2
W6	IO162RSB2
W7	IO157RSB2
W8	IO152RSB2
W9	IO149RSB2
W10	VCCIB2
W11	IO140RSB2
W12	IO135RSB2
W13	IO130RSB2
W14	IO125RSB2
W15	IO120RSB2
W16	IO118RSB2
W17	GDB2/IO115RSB2
W18	TCK
W19	GND

QN132



Notes:

1. This is the bottom view of the package.
2. The die attach paddle center of the package is tied to ground (GND).

Note

QN132 package is discontinued and is not available for IGLOO devices. For more information on package drawings, see PD3068: *Package Mechanical Drawings*.

QN132		QN132		QN132	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
A1	GAB2/IO117UPB3	A37	GBB1/IO38RSB0	B25	GND
A2	IO117VPB3	A38	GBC0/IO35RSB0	B26	IO54PDB1
A3	VCCIB3	A39	VCCIB0	B27	GCB2/IO52PDB1
A4	GFC1/IO110PDB3	A40	IO28RSB0	B28	GND
A5	GFB0/IO109NPB3	A41	IO22RSB0	B29	GCB0/IO49NDB1
A6	VCCPLF	A42	IO18RSB0	B30	GCC1/IO48PDB1
A7	GFA1/IO108PPB3	A43	IO14RSB0	B31	GND
A8	GFC2/IO105PPB3	A44	IO11RSB0	B32	GBB2/IO42PDB1
A9	IO103NDB3	A45	IO07RSB0	B33	VMV1
A10	VCC	A46	VCC	B34	GBA0/IO39RSB0
A11	GEA1/IO98PPB3	A47	GAC1/IO05RSB0	B35	GBC1/IO36RSB0
A12	GEA0/IO98NPB3	A48	GAB0/IO02RSB0	B36	GND
A13	GEC2/IO95RSB2	B1	IO118VDB3	B37	IO26RSB0
A14	IO91RSB2	B2	GAC2/IO116UDB3	B38	IO21RSB0
A15	VCC	B3	GND	B39	GND
A16	IO90RSB2	B4	GFC0/IO110NDB3	B40	IO13RSB0
A17	IO87RSB2	B5	VCOMPLF	B41	IO08RSB0
A18	IO85RSB2	B6	GND	B42	GND
A19	IO82RSB2	B7	GFB2/IO106PSB3	B43	GAC0/IO04RSB0
A20	IO76RSB2	B8	IO103PDB3	B44	GNDQ
A21	IO70RSB2	B9	GND	C1	GAA2/IO118UDB3
A22	VCC	B10	GEB0/IO99NDB3	C2	IO116VDB3
A23	GDB2/IO62RSB2	B11	VMV3	C3	VCC
A24	TDI	B12	FF/GEB2/IO96RSB2	C4	GFB1/IO109PPB3
A25	TRST	B13	IO92RSB2	C5	GFA0/IO108NPB3
A26	GDC1/IO58UDB1	B14	GND	C6	GFA2/IO107PSB3
A27	VCC	B15	IO89RSB2	C7	IO105NPB3
A28	IO54NDB1	B16	IO86RSB2	C8	VCCIB3
A29	IO52NDB1	B17	GND	C9	GEB1/IO99PDB3
A30	GCA2/IO51PPB1	B18	IO78RSB2	C10	GNDQ
A31	GCA0/IO50NPB1	B19	IO72RSB2	C11	GEA2/IO97RSB2
A32	GCB1/IO49PDB1	B20	GND	C12	IO94RSB2
A33	IO47NSB1	B21	GNDQ	C13	VCCIB2
A34	VCC	B22	TMS	C14	IO88RSB2
A35	IO41NPB1	B23	TDO	C15	IO84RSB2
A36	GBA2/IO41PPB1	B24	GDC0/IO58VDB1	C16	IO80RSB2

FG144	
Pin Number	AGL125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	AGL125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	AGL125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG144	
Pin Number	AGL250 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	VCC
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

FG144	
Pin Number	AGL250 Function
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	VCC
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	VCCIB3
E5	IO118VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO48PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	VCOMPLF
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

FG144	
Pin Number	AGL250 Function
G1	GFA1/IO108PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	VCC
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	VCC
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	VCCIB1
H11	IO54PSB1
H12	VCC
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	VCCIB3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	VCC
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

FG484	
Pin Number	AGL600 Function
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

FG484	
Pin Number	AGL600 Function
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0

FG484	
Pin Number	AGL600 Function
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	AGL600 Function
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

FG484	
Pin Number	AGL1000 Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1

FG484	
Pin Number	AGL1000 Function
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2

Revision / Version	Changes	Page
Advance v0.4 (September 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.3 (August 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added.	3-2