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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	84
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl125v5-qng132i

Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

Table 2-31 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 [2]	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 [2]	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

Table 2-47 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-48 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		V_{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-64 • **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard Plus I/O Banks**

3.3 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	**Equivalent Software Default Drive Strength Option[1]**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**µA**	**µA**	**Max. mA[4]**	**Max. mA[4]**	**µA[5]**	**µA[5]**
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	12 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10
100 µA	16 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	103	109	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-69 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	4 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	6 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	8 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	12 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns
100 µA	16 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-70 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	4 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	6 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	8 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	12 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
100 µA	16 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

Table 2-71 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	4 mA	Std.	0.97	5.64	0.18	1.17	0.66	5.65	4.98	2.45	2.42	ns
100 µA	6 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns
100 µA	8 mA	Std.	0.97	4.63	0.18	1.17	0.66	4.64	4.26	2.80	3.02	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-72 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
100 µA	2 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	4 mA	0.97	3.16	0.18	1.17	0.66	3.17	2.53	2.45	2.56	0.97	ns
100 µA	6 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns
100 µA	8 mA	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	0.97	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

Table 2-92 • **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
4 mA	Std.	1.55	2.91	0.26	1.19	1.10	2.95	2.66	2.50	2.72	8.74	8.45	ns
6 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
8 mA	Std.	1.55	2.51	0.26	1.19	1.10	2.54	2.18	2.75	3.21	8.33	7.97	ns
12 mA	Std.	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-93 • **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
4 mA	Std.	1.55	4.85	0.26	1.15	1.10	4.93	4.55	2.13	2.24	ns
6 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns
8 mA	Std.	1.55	4.09	0.26	1.15	1.10	4.16	3.95	2.38	2.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-94 • **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
4 mA	Std.	1.55	2.76	0.26	1.15	1.10	2.80	2.52	2.13	2.32	ns
6 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns
8 mA	Std.	1.55	2.39	0.26	1.15	1.10	2.42	2.05	2.38	2.80	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-113* • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSH**	**IOSL**	**IIL**[1]	**IIH**[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**[3]	**Max. mA**[3]	**μA**[4]	**μA**[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

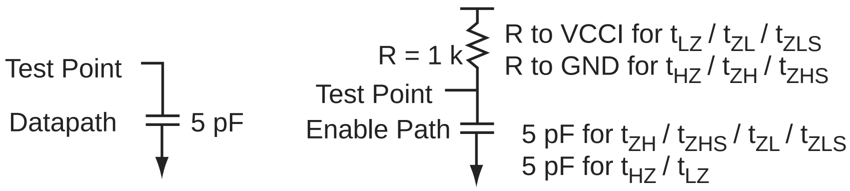

***Figure 2-10* • AC Loading**

***Table 2-114* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**C_{LOAD} (pF)**
0	1.5	0.75	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

Table 2-127 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.2 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSH**	**IOSL**	**IIL[1]**	**IIH[2]**
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-128 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.2 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**I_{OL}**	**IOH**	**IOSH**	**IOSL**	**IIL[1]**	**IIH[2]**
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2	20	26	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-129 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.2 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSH**	**IOSL**	**IIL[1]**	**IIH[2]**
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**μA[4]**	**μA[4]**
1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	1	1	20	26	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-138* • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard Plus I/O Banks**

1.2 V LVCMOS Wide Range		**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSL**	**IOSH**	**IIL[2]**	**IIH[3]**
Drive Strength	**Equivalent Software Default Drive Strength Option[1]**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[4]**	**Max. mA[4]**	**μA[5]**	**μA[5]**
100 µA	2mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

***Table 2-139* • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard I/O Banks**

1.2 V LVCMOS Wide Range		**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSL**	**IOSH**	**IIL[2]**	**IIH[3]**
Drive Strength	**Equivalent Software Default Drive Strength Option[1]**	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[4]**	**Max. mA[4]**	**μA[5]**	**μA[5]**
100 µA	1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

***Table 2-140* • 1.2 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**C_{LOAD} (pF)**
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-75 for worst-case timing.

Table 2-175 • **AGL060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-176 • **AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-183 • **AGL060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.04	2.33	ns
t_{RCKH}	Input High Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.40	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-184 • **AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

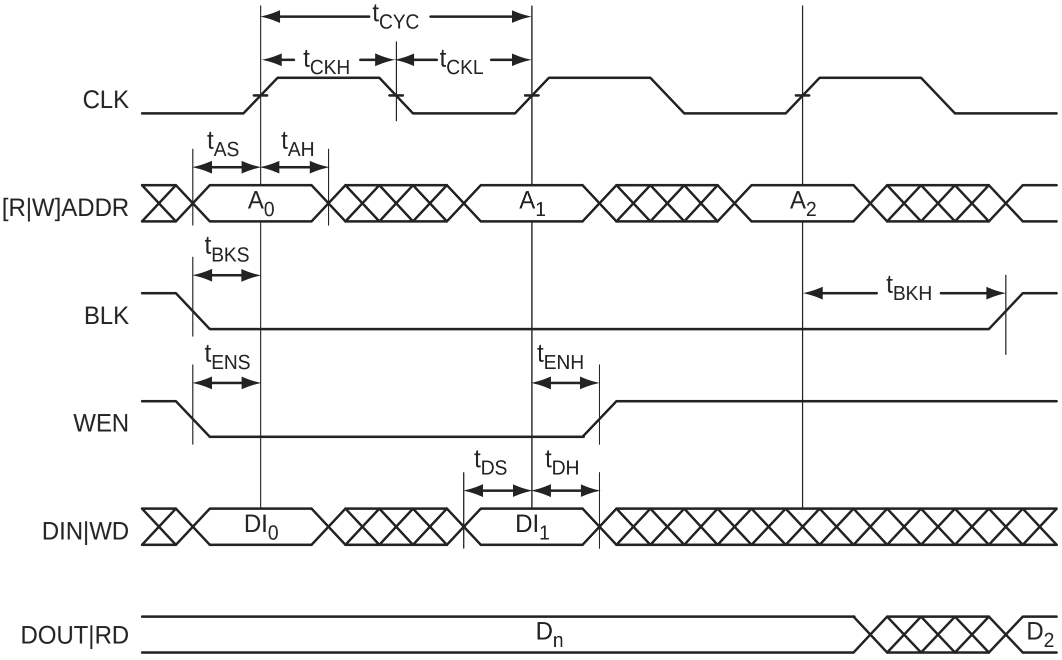

***Figure 2-34* • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

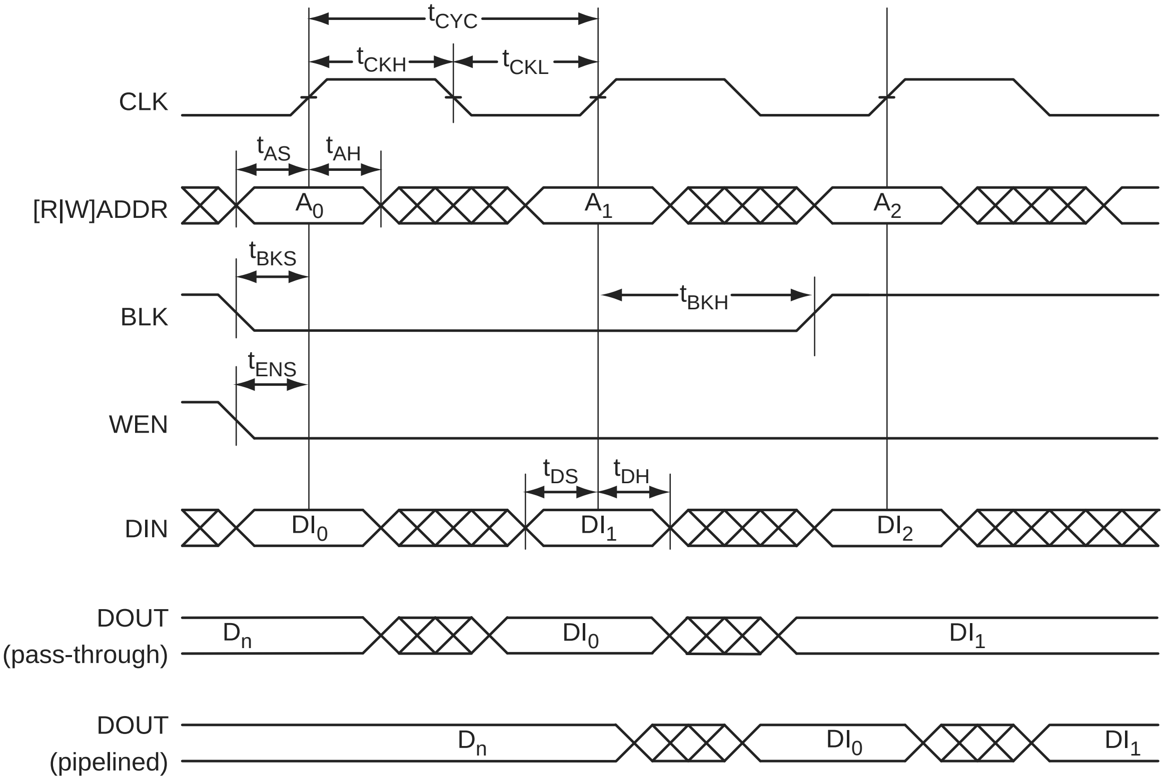

***Figure 2-35* • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

Embedded FlashROM Characteristics

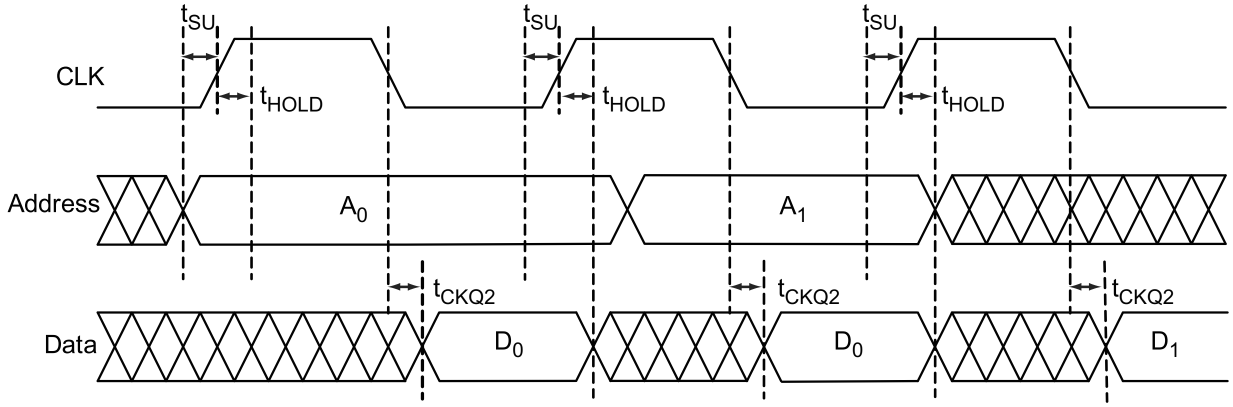

***Figure 2-45* •** **Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-197* • Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

***Table 2-198* • Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

QN68	
Pin Number	**AGL015 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	**AGL015 Function**
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

FG144	
Pin Number	**AGL1000 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

FG144	
Pin Number	**AGL1000 Function**
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

FG144	
Pin Number	**AGL1000 Function**
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

FG484	
Pin Number	**AGL400 Function**
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	**AGL400 Function**
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	FF/GEB2/IO133RSB2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC

FG484	
Pin Number	**AGL1000 Function**
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3

Revision	Changes	Page
Revision 23 (December 2012)	The "IGLOO Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43173).	III
	The note in Table 2-189 · IGLOO CCC/PLL Specification and Table 2-190 · IGLOO CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42564). Additionally, note regarding SSOs was added.	2-115, 2-116
	Live at Power-Up (LAPU) has been replaced with ’Instant On’.	NA
Revision 22 (September 2012)	The "Security" section was modified to clarify that Microsemi does not support read-back of programmed data.	1-2
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40271).	N/A
Revision 21 (May 2012)	Under AGL125, in the Package Pin list, CS121 was incorrectly added to the datasheet in revision 19 and has been removed (SAR 38217).	I to IV
	Corrected the inadvertent error for Max Values for LVPECL VIH and revised the same to ’3.6’ in Table 2-151 · Minimum and Maximum DC Input and Output Levels (SAR 37685).	2-82
	Figure 2-38 • FIFO Read and Figure 2-39 • FIFO Write have been added (SAR 34841).	2-127
	The following sentence was removed from the VMVx description in the "Pin Descriptions" section: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with “Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks” (SAR 38317). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1