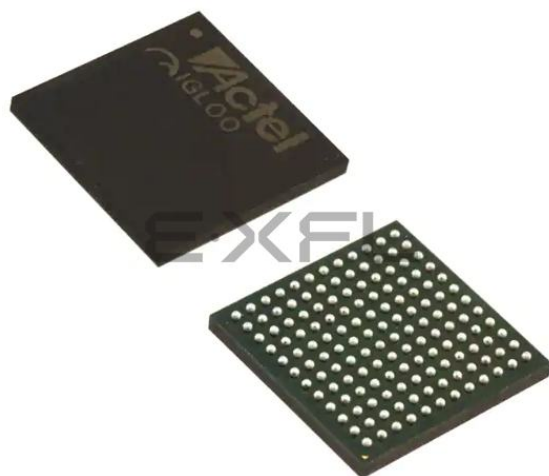




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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl250v2-fgg144t

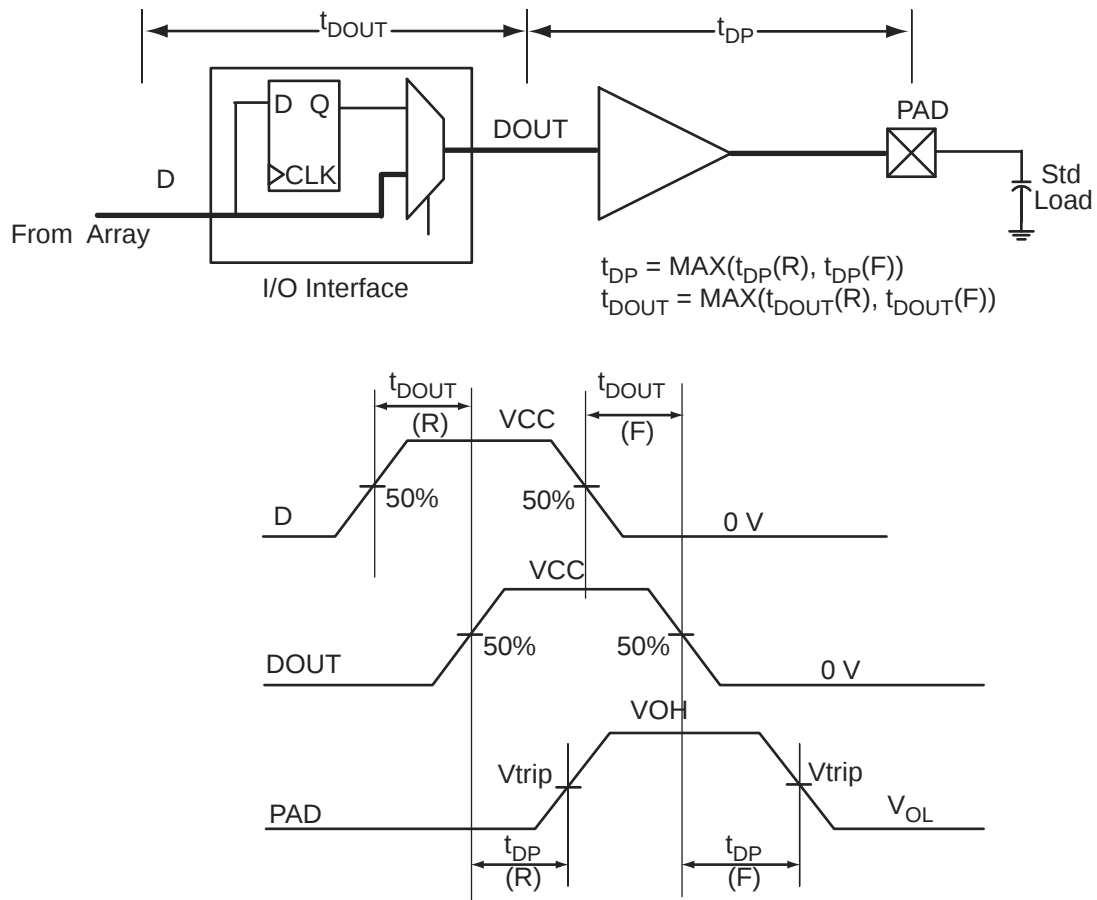


Figure 2-5 • Output Buffer Model and Delays (example)

Detailed I/O DC Characteristics

Table 2-37 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C _{IN}	Input capacitance	V _{IN} = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on the clock pin	V _{IN} = 0, f = 1.0 MHz		8	pF

Table 2-38 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS ⁴	2 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μA	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$
4. Applicable to IGLOO V2 Devices operating at VCCI ≥ VCC

Applies to 1.2 V Core Voltage**Table 2-89 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • 2.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-91 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-100 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-101 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-102 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-103 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Input Register

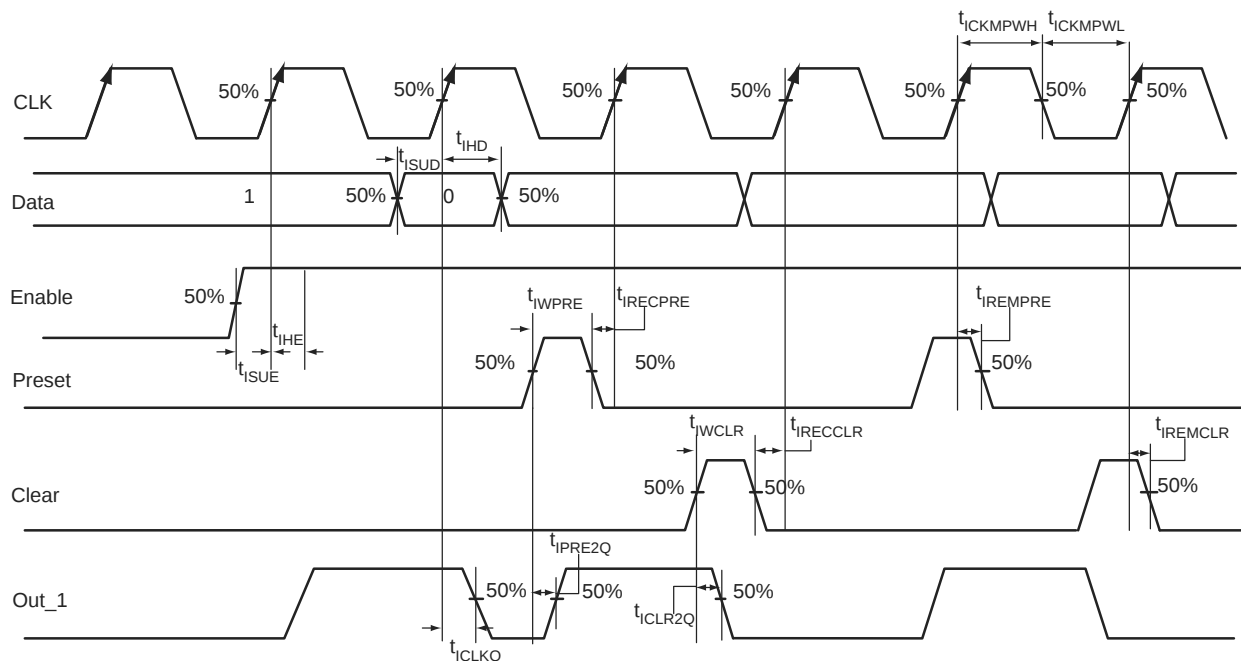


Figure 2-18 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-157 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

DDR Module Specifications

Input DDR Module

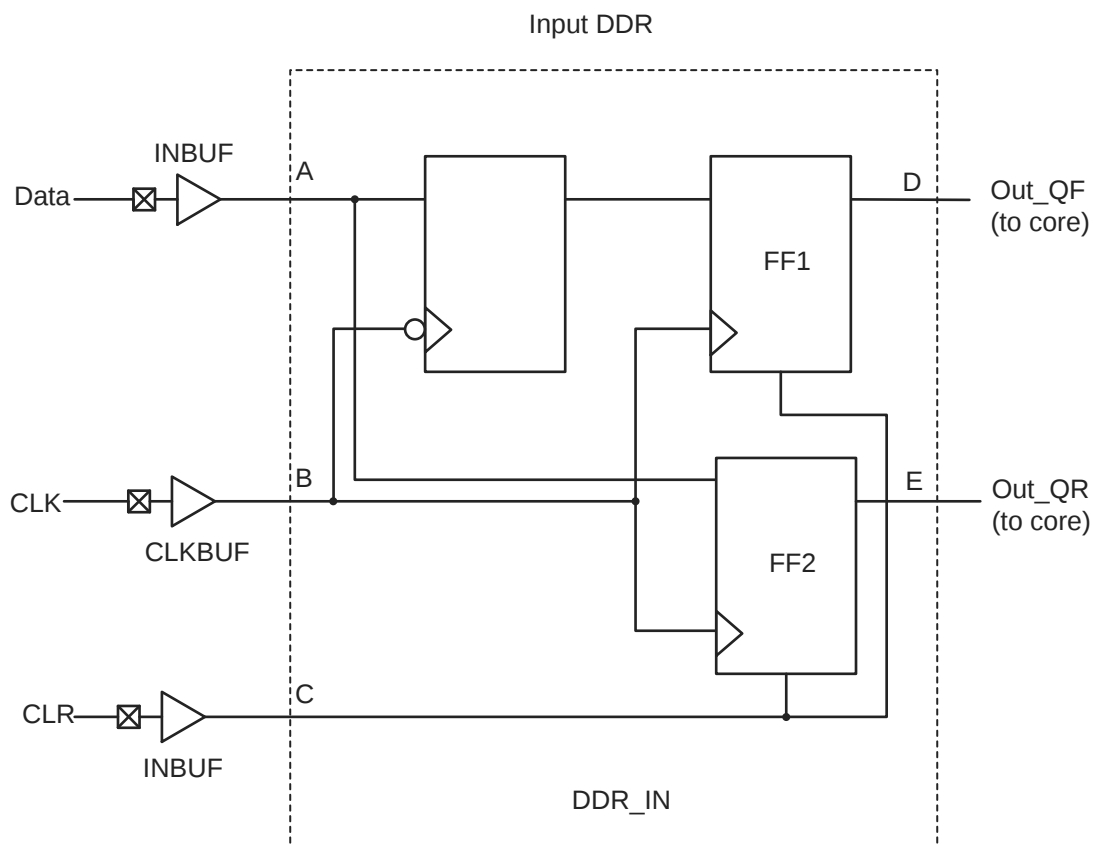


Figure 2-21 • Input DDR Timing Model

Table 2-163 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDRICKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRICKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

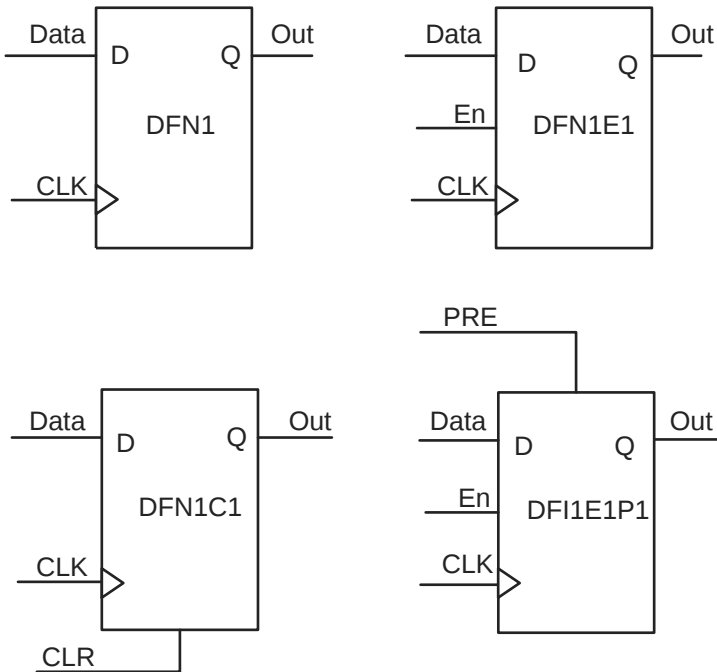


Figure 2-27 • Sample of Sequential Cells

Table 2-177 • AGL250 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-178 • AGL400 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.45	1.79	ns
t_{RCKH}	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-183 • AGL060 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.04	2.33	ns
t_{RCKH}	Input High Delay for Global Clock	2.10	2.51	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.40		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.40	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-184 • AGL125 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.40		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO a devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO FPGA Fabric User Guide* for more information on I/O states during Flash*Freeze mode.

Table 3-1 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)

IGLOO Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
CS281	W2
QN48	14
QN68	18
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

CS281	
Pin Number	AGL600 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO07RSB0
A5	IO10RSB0
A6	IO14RSB0
A7	IO18RSB0
A8	IO21RSB0
A9	IO22RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO40RSB0
A13	IO37RSB0
A14	IO48RSB0
A15	IO51RSB0
A16	IO53RSB0
A17	GBC1/IO55RSB0
A18	GBA0/IO58RSB0
A19	GND
B1	GAA2/IO174PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO06RSB0
B6	GND
B7	IO15RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO24RSB0
B11	IO36RSB0
B12	IO35RSB0
B13	IO44RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO54RSB0
B17	GBA1/IO59RSB0

CS281	
Pin Number	AGL600 Function
B18	VCCIB1
B19	IO61NDB1
C1	GAB2/IO173PPB3
C2	IO174NPB3
C6	IO12RSB0
C14	IO50RSB0
C18	IO60NPB1
C19	GBB2/IO61PDB1
D1	IO170PPB3
D2	IO172NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO09RSB0
D7	IO16RSB0
D8	IO19RSB0
D9	IO26RSB0
D10	GND
D11	IO34RSB0
D12	IO45RSB0
D13	IO49RSB0
D14	IO47RSB0
D15	GBB0/IO56RSB0
D16	GBA2/IO60PPB1
D18	GBC2/IO62PPB1
D19	IO66NPB1
E1	IO169NPB3
E2	IO171PPB3
E4	IO171NPB3
E5	IO08RSB0
E6	IO11RSB0
E7	IO13RSB0
E8	IO17RSB0
E9	IO25RSB0
E10	IO30RSB0
E11	IO41RSB0
E12	IO42RSB0

CS281	
Pin Number	AGL600 Function
E13	IO46RSB0
E14	GBB1/IO57RSB0
E15	IO62NPB1
E16	IO63PPB1
E18	IO64PPB1
E19	IO65NPB1
F1	IO168NPB3
F2	GND
F3	IO169PPB3
F4	IO170NPB3
F5	IO173NPB3
F15	IO63NPB1
F16	IO65PPB1
F17	IO64NPB1
F18	GND
F19	IO68PPB1
G1	IO167NPB3
G2	IO165NDB3
G4	IO168PPB3
G5	IO167PPB3
G7	GAC2/IO172PPB3
G8	VCCIB0
G9	IO28RSB0
G10	IO32RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO66PPB1
G15	IO67NDB1
G16	IO67PDB1
G18	GCC0/IO69NPB1
G19	GCB1/IO70PPB1
H1	GFB0/IO163NPB3
H2	IO165PDB3
H4	GFC1/IO164PPB3
H5	GFB1/IO163PPB3
H7	VCCIB3

FG256	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL400 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL400 Function
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

FG256	
Pin Number	AGL1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	AGL400 Function
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

FG484	
Pin Number	AGL400 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO67PPB1
K17	IO64NPB1
K18	IO73PDB1
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC

FG484	
Pin Number	AGL600 Function
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

FG484	
Pin Number	AGL600 Function
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

FG484	
Pin Number	AGL1000 Function
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

Revision / Version	Changes	Page
Advance v0.4 (September 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.3 (August 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added.	3-2