Microsemi Corporation - AGL250V2-VQG100T Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	68
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl250v2-vqg100t

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

I/Os Per Package[1]

IGLOO Devices	AGL015[2]	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250				M1AGL600		M1AGL1000	
	I/O Type[3]											
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs	Single-Ended I/O [4]	Differential I/O Pairs
QN48	–	34	–	–	–	–	–	–	–	–	–	–
QN68	49	49	–	–	–	–	–	–	–	–	–	–
UC81	–	66	–	–	–	–	–	–	–	–	–	–
CS81	–	66	–	–	–	–	–	–	–	–	–	–
CS121	–	–	96	96	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–	–	–	–	–
QN132[6]	–	81	80	84	–	–	–	–	–	–	–	–
CS196	–	–	–	133	143 [5]	35 [5]	143	35	–	–	–	–
FG144	–	–	–	97	97	24	97	25	97	25	97	25
FG256[7]	–	–	–	–	–	–	178	38	177	43	177	44
CS281	–	–	–	–	–	–	–	–	215	53	215	53
FG484[7]	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the* IGLOO FPGA Fabric User Guide *to ensure compliance with design and board migration requirements.*
2. *AGL015 is not recommended for new designs.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
5. *The M1AGL250 device does not support QN132 or CS196 packages.*
6. *Package not available.*
7. *FG256 and FG484 are footprint-compatible packages.*

Table 1 • IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23
Nominal Area (mm^2)	16	25	36	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

*Note: * Package not available.*

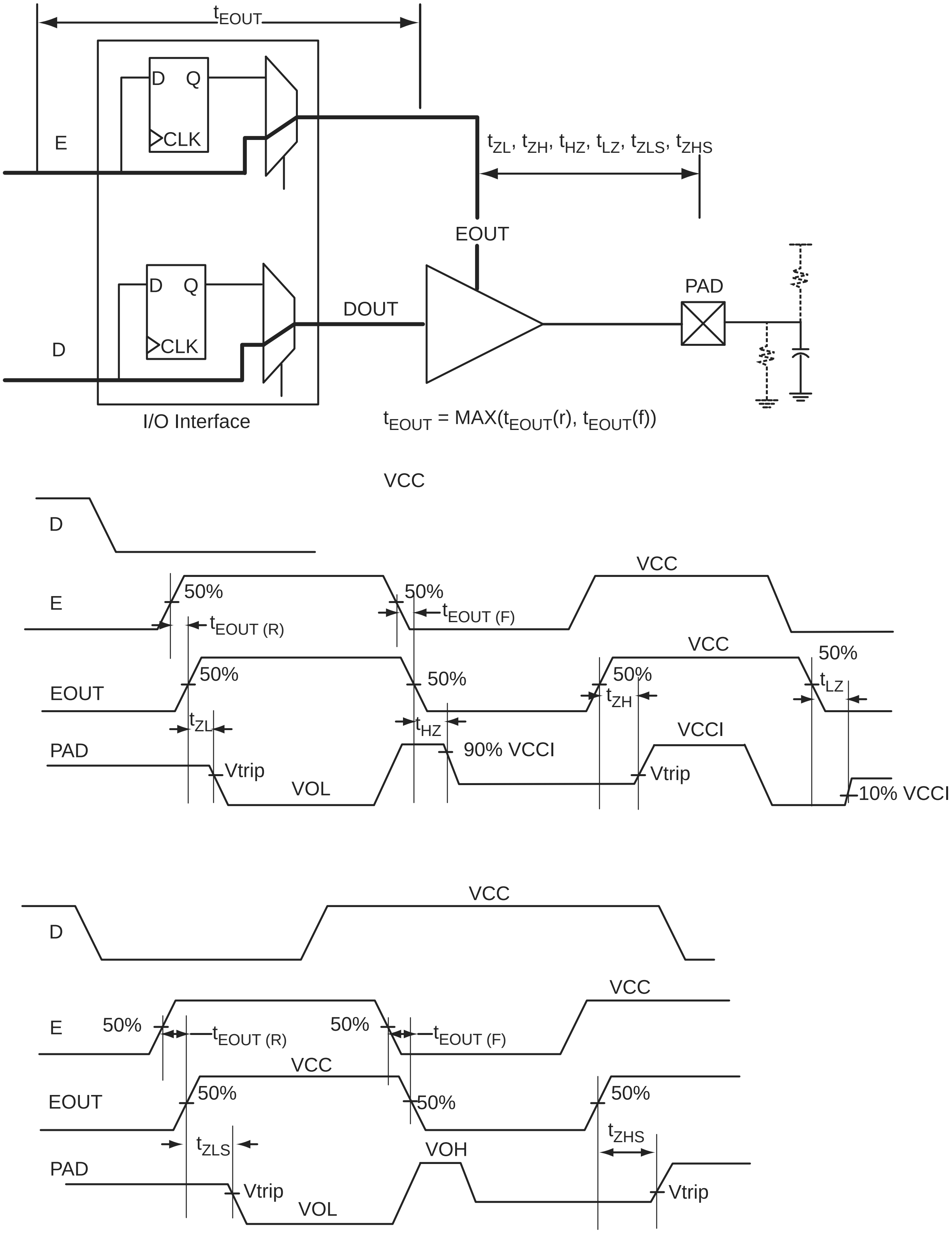


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Table 2-42 • **I/O Short Currents IOSH/IOSL Applicable to Advanced I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *$T_J = 100°C$

Table 2-54 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-55 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-56 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-75 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 µA	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 µA	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 µA	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 µA	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 µA	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-76 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 µA	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 µA	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 µA	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 µA	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 µA	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

Output DDR Module

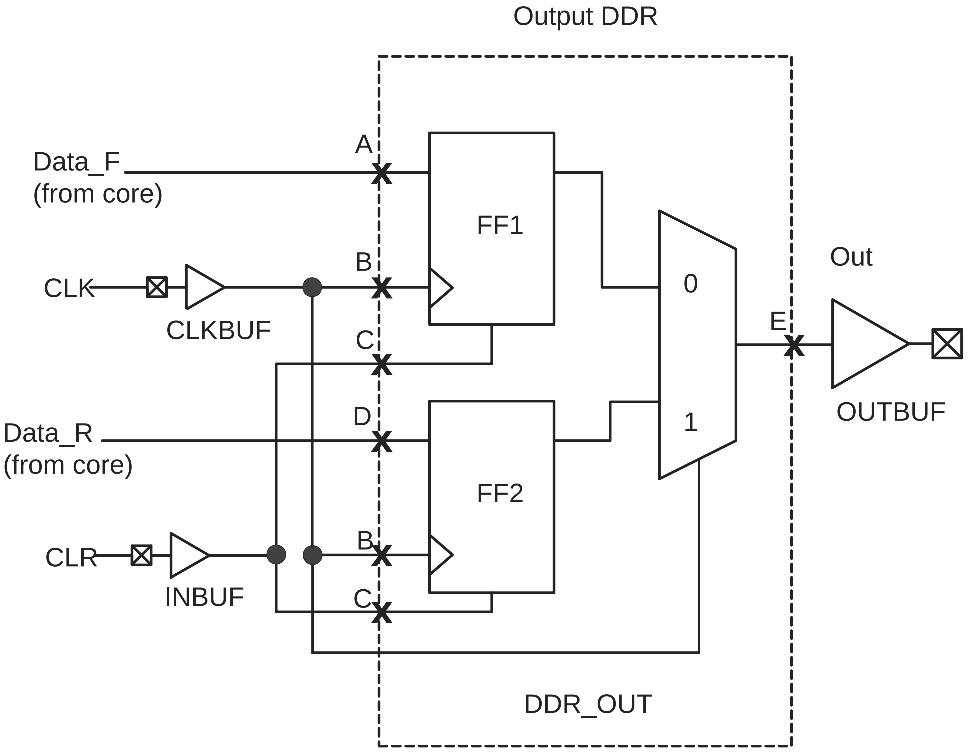


Figure 2-23 • **Output DDR Timing Model**

***Table 2-166* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-169* • Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y =!A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y =!(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	1.33	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

***Table 2-170* • Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.34	ns
AND2	Y = A · B	t_{PD}	1.43	ns
NAND2	Y = !(A · B)	t_{PD}	1.59	ns
OR2	Y = A + B	t_{PD}	2.30	ns
NOR2	Y = !(A + B)	t_{PD}	2.07	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.46	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	2.46	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.12	ns
MUX2	Y = A !S + B S	t_{PD}	2.83	ns
AND3	Y = A · B · C	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

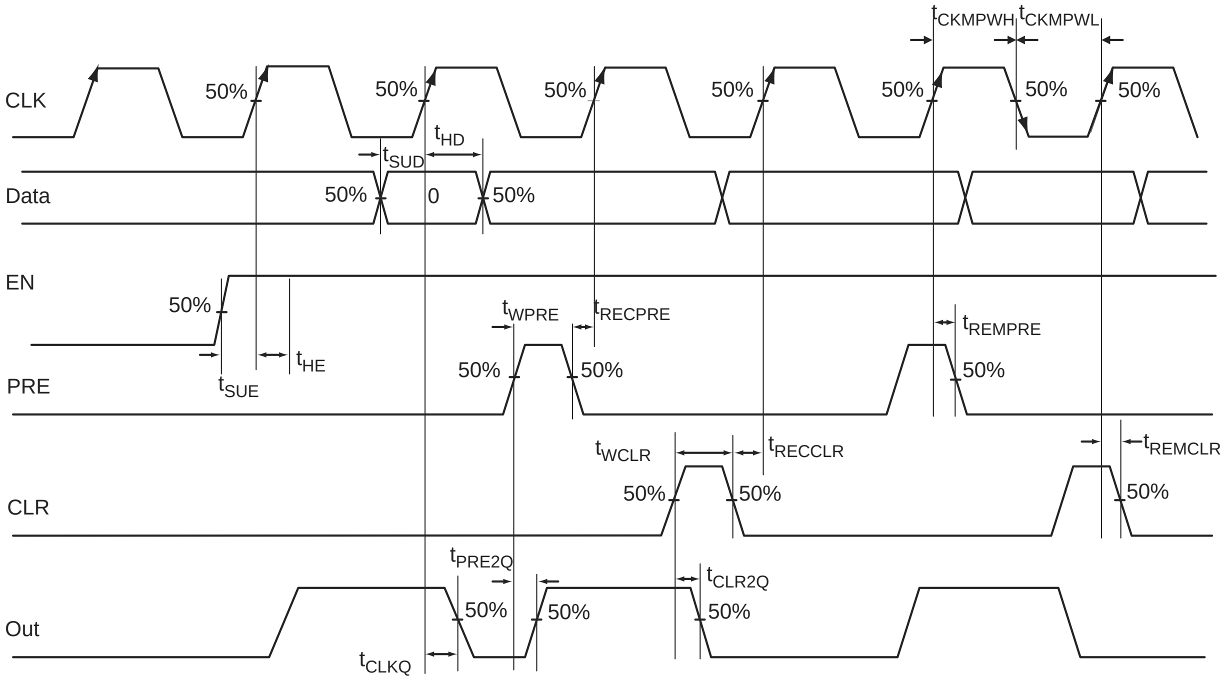


Figure 2-28 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-171 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-177 • **AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	**Description**	**Std.**		**Units**
		Min.[1]	**Max.**[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input High Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-178 • **AGL400 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	**Description**	**Std.**		**Units**
		Min. [1]	**Max.** [2]	
t_{RCKL}	Input Low Delay for Global Clock	1.45	1.79	ns
t_{RCKH}	Input High Delay for Global Clock	1.48	1.91	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-7 for derating values.*

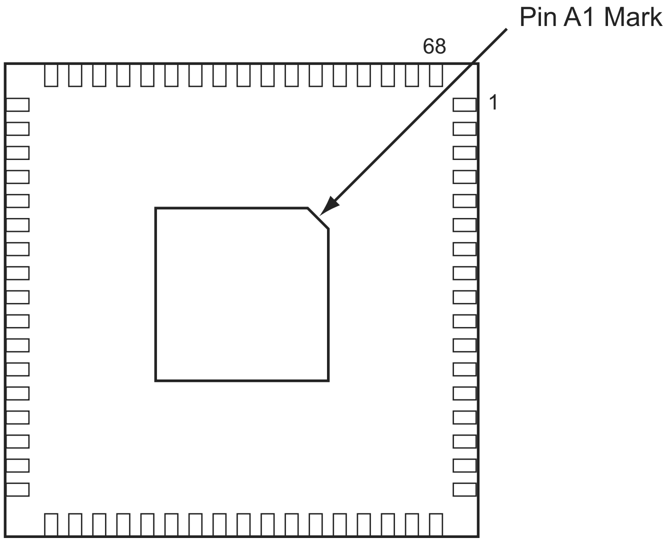
Table 2-192 • RAM512X18
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN, WEN setup time	0.73	ns
t_{ENH}	REN, WEN hold time	0.08	ns
t_{DS}	Input data (WD) setup time	0.71	ns
t_{DH}	Input data (WD) hold time	0.36	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	4.21	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	1.71	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge	0.35	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge	0.42	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	2.06	ns
	RESET Low to data out Low on RD (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET removal	0.61	ns
$t_{RECRSTB}$	RESET recovery	3.21	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

QN68



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

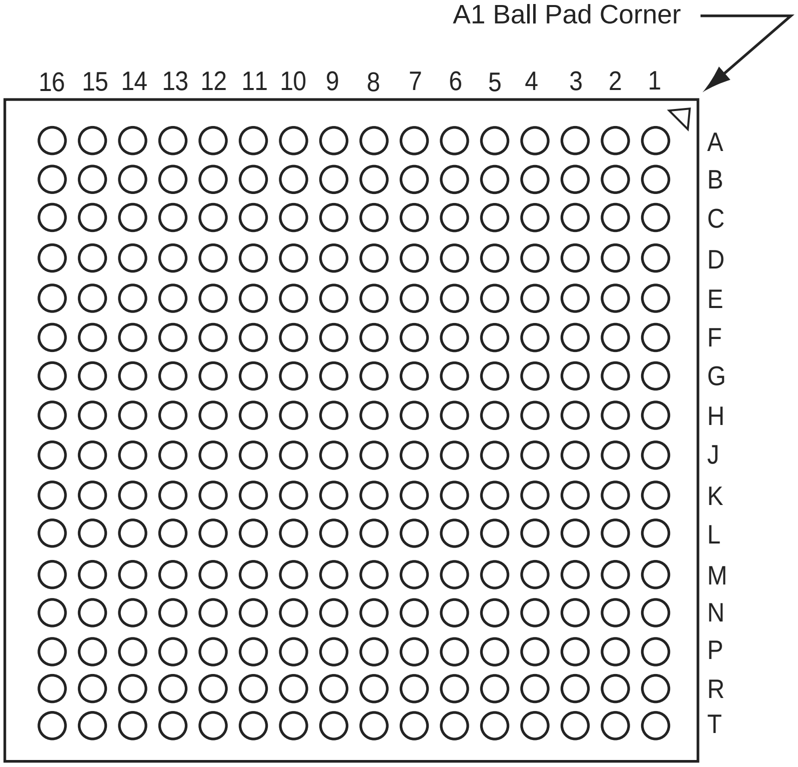
For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN68	
Pin Number	**AGL015 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	**AGL015 Function**
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

FG144	
Pin Number	**AGL1000 Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG256	
Pin Number	**AGL400 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

FG484	
Pin Number	**AGL400 Function**
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	**AGL600 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	VCOMPLF
L8	GFC0/IO164NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3

FG484	
Pin Number	**AGL600 Function**
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1

FG484	
Pin Number	**AGL600 Function**
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2

Revision / Version	Changes	Page
DC & Switching, cont'd.	Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.	2-39
Revision 9 (Jul 2008) Product Brief v1.1 DC and Switching Characteristics Advance v0.3	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Revision 8 (Jun 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
DC and Switching Characteristics Advance v0.2	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather then simulation values. AGL015 global clock delays have been added.	N/A
	Table 2-1 • Absolute Maximum Ratings was updated to combine the VCCI and VMV parameters in one row. The word "output" from the parameter description for VCCI and VMV, and table note 3 was added.	2-1
	Table 2-2 • Recommended Operating Conditions 1 was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the VCCI parameter row, and table note 9 was added.	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-3
	VMV was removed from Table 2-4 • Overshoot and Undershoot Limits 1. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels is new.	2-5
	EQ 2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode*, Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*, and Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode were updated to remove VMV and include PDC6 and PDC7. VCCI and VJTAG were removed from the statement about IDD in the table note for Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode.	2-7
	Note 2 of Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode1 was updated to include VCCPLL. Note 4 was updated to include PDC6 and PDC7.	2-9