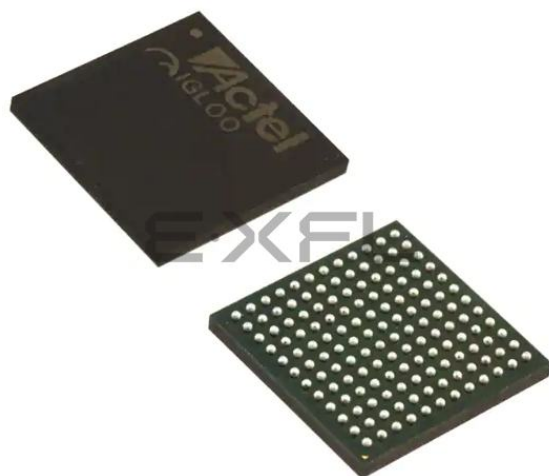




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	9216
Total RAM Bits	55296
Number of I/O	97
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl400v2-fg144

IGLOO Device Family Overview

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IGLOO DC and Switching Characteristics

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field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the ProASIC[®] family of third-generation-architecture flash FPGAs.

[†] The AGL015 and AGL030 do not support PLL or SRAM.

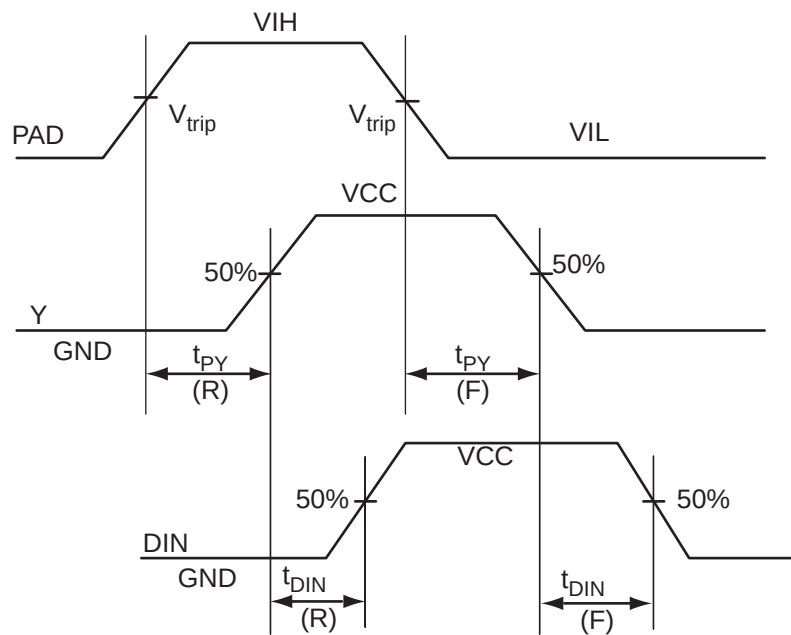
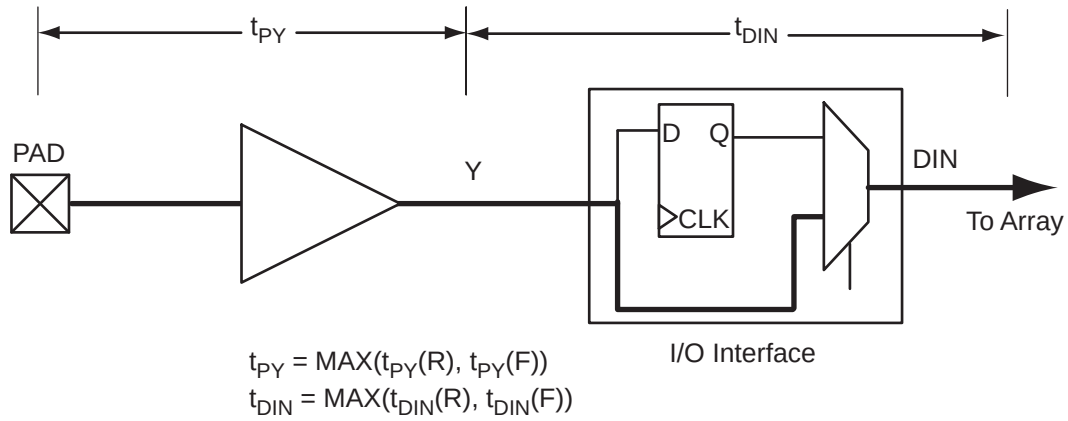


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Applies to 1.2 V DC Core Voltage

Table 2-73 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 μA	4 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 μA	6 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 μA	8 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 μA	12 mA	Std.	1.55	5.55	0.26	1.32	1.10	5.55	4.96	4.50	5.18	11.34	10.75	ns
100 μA	16 mA	Std.	1.55	5.32	0.26	1.32	1.10	5.32	4.82	4.56	5.29	11.10	10.61	ns
100 μA	24 mA	Std.	1.55	5.19	0.26	1.32	1.10	5.19	4.85	4.63	5.74	10.98	10.63	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-74 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 μA	4 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 μA	6 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 μA	8 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 μA	12 mA	Std.	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
100 μA	16 mA	Std.	1.55	3.67	0.26	1.32	1.10	3.67	2.85	4.57	5.55	9.46	8.64	ns
100 μA	24 mA	Std.	1.55	3.70	0.26	1.32	1.10	3.70	2.79	4.65	6.01	9.49	8.58	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.
3. Software default selection highlighted in gray.

Applies to 1.2 V Core Voltage
Table 2-89 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • 2.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-91 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage

 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-115 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-116 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-117 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-118 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-123 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.43	0.26	1.27	1.10	6.54	5.95	2.82	2.83	12.32	11.74	ns
4 mA	Std.	1.55	5.59	0.26	1.27	1.10	5.68	5.27	3.07	3.27	11.47	11.05	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.**Table 2-124 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.02	0.26	1.27	1.10	3.07	2.81	2.82	2.92	8.85	8.59	ns
4 mA	Std.	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-125 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.40	2.46	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.**Table 2-126 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.92	0.26	1.22	1.10	2.96	2.60	2.40	2.56	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-7 on page 2-7](#) for derating values.

Table 2-135 • 1.2 V LVC MOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	8.57	0.26	1.53	1.10	8.23	7.38	2.51	2.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-136 • 1.2 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 1.14\text{ V}$

Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	3.59	0.26	1.53	1.10	3.47	3.06	2.51	2.49	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V LVC MOS Wide Range

Table 2-137 • Minimum and Maximum DC Input and Output Levels for LVC MOS 1.2 V Wide Range

Applicable to Advanced I/O Banks

1.2 V LVC MOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Equivalent Software Default Drive Strength Option ¹	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ⁴	Max. mA ⁴	μA^5	μA^5
100 μA	2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

- The minimum drive strength for the default LVC MOS 1.2 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.
- IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
- IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
- Currents are measured at 100°C junction temperature and maximum voltage.
- Currents are measured at 85°C junction temperature.
- Software default selection highlighted in gray.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

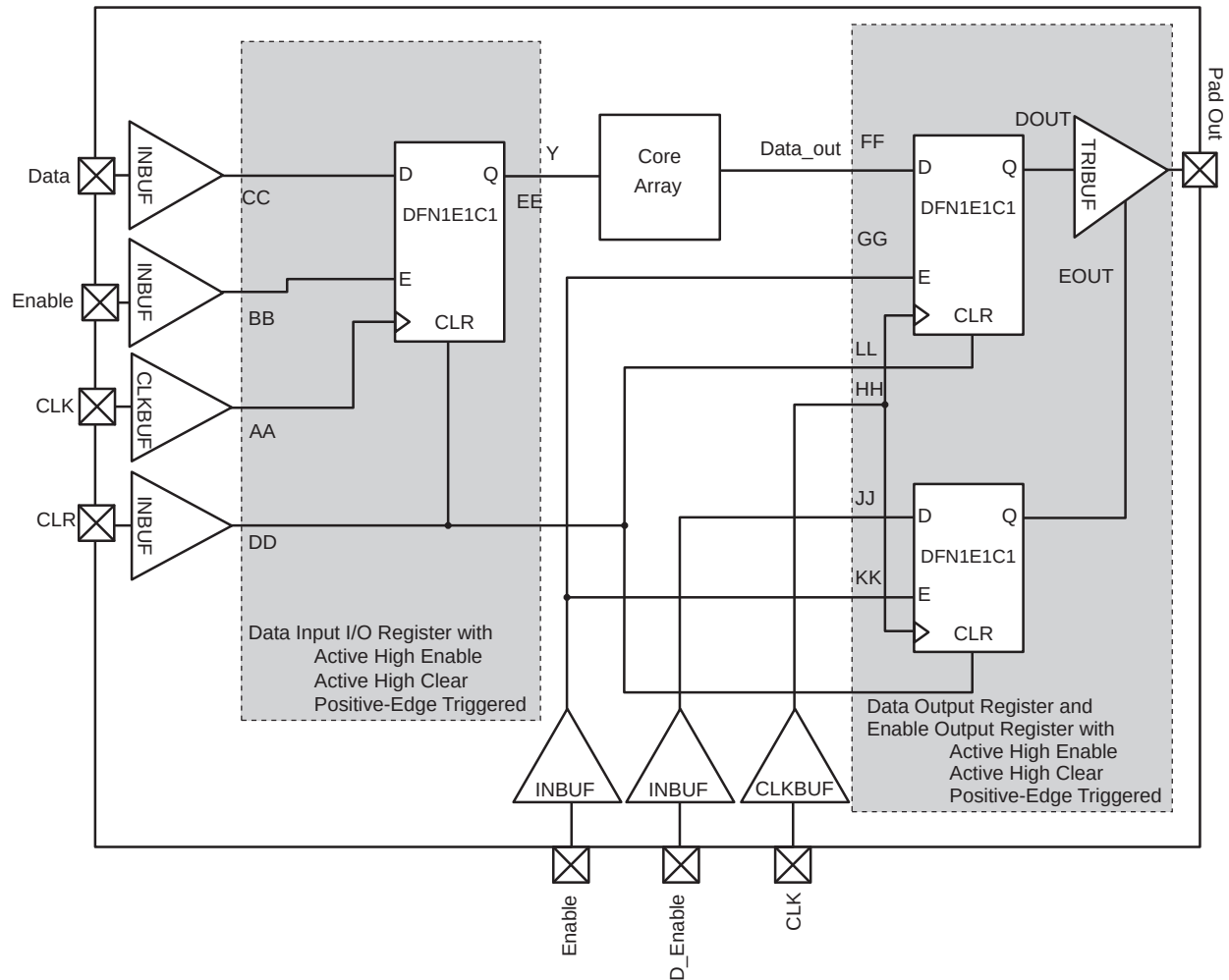


Figure 2-17 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-156 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERCCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-17 on page 2-86 for more information.

Table 2-175 • AGL060 Global Resource

 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

Table 2-176 • AGL125 Global Resource

 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input High Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

1.2 V DC Core Voltage

Table 2-193 • RAM4K9

 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}^1	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.30	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-7](#) for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-199 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
t_{TRSTREM}	ResetB Removal Time	0.58	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-200 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
t_{TRSTREM}	ResetB Removal Time	1.18	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

CS281		CS281		CS281	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
H8	VCC	K15	IO73NPB1	N4	IO150PPB3
H9	VCCIB0	K16	GND	N5	IO148NPB3
H10	VCC	K18	IO74NPB1	N7	GEA2/IO143RSB2
H11	VCCIB0	K19	VCCIB1	N8	VCCIB2
H12	VCC	L1	GFB2/IO160PDB3	N9	IO117RSB2
H13	VCCIB1	L2	IO160NDB3	N10	IO115RSB2
H15	IO68NPB1	L4	GFC2/IO159PPB3	N11	IO114RSB2
H16	GCB0/IO70NPB1	L5	IO153PPB3	N12	VCCIB2
H18	GCA1/IO71PPB1	L7	IO153NPB3	N13	VPUMP
H19	GCA2/IO72PPB1	L8	VCCIB3	N15	IO82PPB1
J1	VCOMPLF	L9	GND	N16	IO85PPB1
J2	GFA0/IO162NDB3	L10	GND	N18	IO82NPB1
J4	VCCPLF	L11	GND	N19	IO81PPB1
J5	GFC0/IO164NPB3	L12	VCCIB1	P1	IO151PDB3
J7	GFA2/IO161PDB3	L13	IO76PPB1	P2	GND
J8	VCCIB3	L15	IO76NPB1	P3	IO151NDB3
J9	GND	L16	IO77PPB1	P4	IO149PPB3
J10	GND	L18	IO78NPB1	P5	GEA0/IO144NPB3
J11	GND	L19	IO77NPB1	P15	IO83NDB1
J12	VCCIB1	M1	IO158PDB3	P16	IO83PDB1
J13	GCC1/IO69PPB1	M2	IO158NDB3	P17	GDC1/IO86PPB1
J15	GCA0/IO71NPB1	M4	IO154NPB3	P18	GND
J16	GCB2/IO73PPB1	M5	IO152PPB3	P19	IO85NPB1
J18	IO72NPB1	M7	VCCIB3	R1	IO150NPB3
J19	IO75PSB1	M8	VCC	R2	IO149NPB3
K1	VCCIB3	M9	VCCIB2	R4	GEC1/IO146PPB3
K2	GFA1/IO162PDB3	M10	VCC	R5	GEB1/IO145PPB3
K4	GND	M11	VCCIB2	R6	IO138RSB2
K5	IO159NPB3	M12	VCC	R7	IO127RSB2
K7	IO161NDB3	M13	VCCIB1	R8	IO123RSB2
K8	VCC	M15	IO79NPB1	R9	IO118RSB2
K9	GND	M16	IO81NPB1	R10	IO111RSB2
K10	GND	M18	IO79PPB1	R11	IO106RSB2
K11	GND	M19	IO78PPB1	R12	IO103RSB2
K12	VCC	N1	IO154PPB3	R13	IO97RSB2
K13	GCC2/IO74PPB1	N2	IO152NPB3	R14	IO95RSB2

CS281		CS281	
Pin Number	AGL600 Function	Pin Number	AGL600 Function
R15	IO94RSB2	V10	IO112RSB2
R16	GDA1/IO88PPB1	V11	IO110RSB2
R18	GDB0/IO87NPB1	V12	IO108RSB2
R19	GDC0/IO86NPB1	V13	IO102RSB2
T1	IO148PPB3	V14	GND
T2	GEC0/IO146NPB3	V15	IO93RSB2
T4	GEB0/IO145NPB3	V16	GDA2/IO89RSB2
T5	IO132RSB2	V17	TDI
T6	IO136RSB2	V18	VCCIB2
T7	IO130RSB2	V19	TDO
T8	IO126RSB2	W1	GND
T9	IO120RSB2	W2	FF/GEB2/IO142RSB2
T10	GND	W3	IO139RSB2
T11	IO113RSB2	W4	IO137RSB2
T12	IO104RSB2	W5	IO134RSB2
T13	IO101RSB2	W6	IO133RSB2
T14	IO98RSB2	W7	IO128RSB2
T15	GDC2/IO91RSB2	W8	IO124RSB2
T16	TMS	W9	IO119RSB2
T18	VJTAG	W10	VCCIB2
T19	GDB1/IO87PPB1	W11	IO109RSB2
U1	IO147PDB3	W12	IO107RSB2
U2	GEA1/IO144PPB3	W13	IO105RSB2
U6	IO131RSB2	W14	IO100RSB2
U14	IO99RSB2	W15	IO96RSB2
U18	TRST	W16	IO92RSB2
U19	GDA0/IO88NPB1	W17	GDB2/IO90RSB2
V1	IO147NDB3	W18	TCK
V2	VCCIB3	W19	GND
V3	GEC2/IO141RSB2		
V4	IO140RSB2		
V5	IO135RSB2		
V6	GND		
V7	IO125RSB2		
V8	IO122RSB2		
V9	IO116RSB2		

QN132	
Pin Number	AGL030 Function
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	VCCIB0
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC
C35	VCCIB0
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

FG144	
Pin Number	AGL125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	AGL125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	AGL125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG144	
Pin Number	AGL250 Function
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	AGL1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

Revision / Version	Changes	Page
Advance v0.4 (September 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.3 (August 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.2	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A , ambient temperature, and table notes 4–6 were added.	3-2