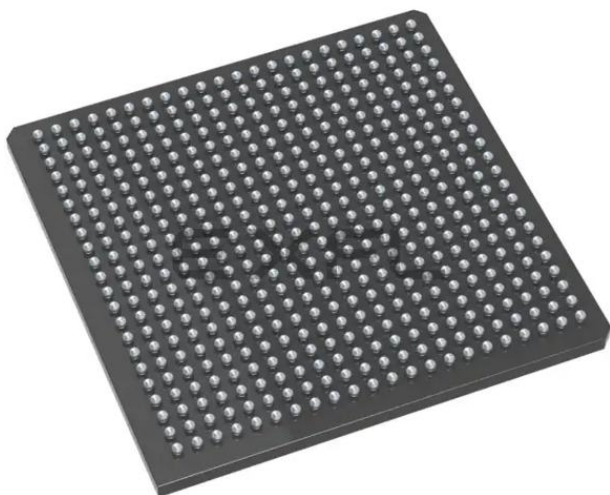




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	9216
Total RAM Bits	55296
Number of I/O	194
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl400v5-fg484

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note: $IDD = N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode¹

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
ICCA Current²										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	μA
	1.5 V	14	16	20	28	44	66	82	137	μA
ICCI or IJTAG Current³										
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} \times ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VPUMP, and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.27
3.3 V LVCMOS Wide Range ³	3.3	–	16.27
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.61
1.5 V LVCMOS (JESD8-11)	1.5	–	0.96
1.2 V LVCMOS ⁴	1.2	–	0.58
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.58
3.3 V PCI	3.3	–	17.67
3.3 V PCI-X	3.3	–	17.67
Differential			
LVDS	2.5	2.26	23.39
LVPECL	3.3	5.72	59.05

Notes:

1. P_{DC6} is the static power (where applicable) measured on VCCI.
2. P_{AC9} is the total dynamic power measured on VCCI.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable for IGLOO V2 devices only

Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks

	VCCI (V)	Static Power PDC6 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.41
3.3 V LVCMOS Wide Range ³	3.3	–	16.41
2.5 V LVCMOS	2.5	–	4.75
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.00
1.2 V LVCMOS ⁴	1.2	–	0.61
1.2 V LVCMOS Wide Range ⁴	1.2	–	0.61
3.3 V PCI	3.3	–	17.78
3.3 V PCI-X	3.3	–	17.78

Notes:

1. P_{DC6} is the static power (where applicable) measured on VCCI.
2. P_{AC9} is the total dynamic power measured on VCCI.
3. Applicable for IGLOO V2 devices only.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-23 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-24 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

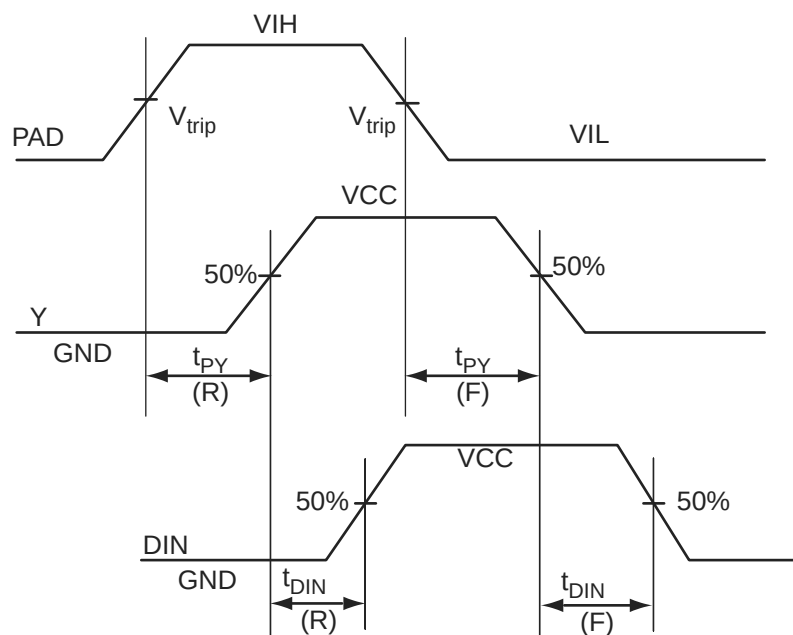
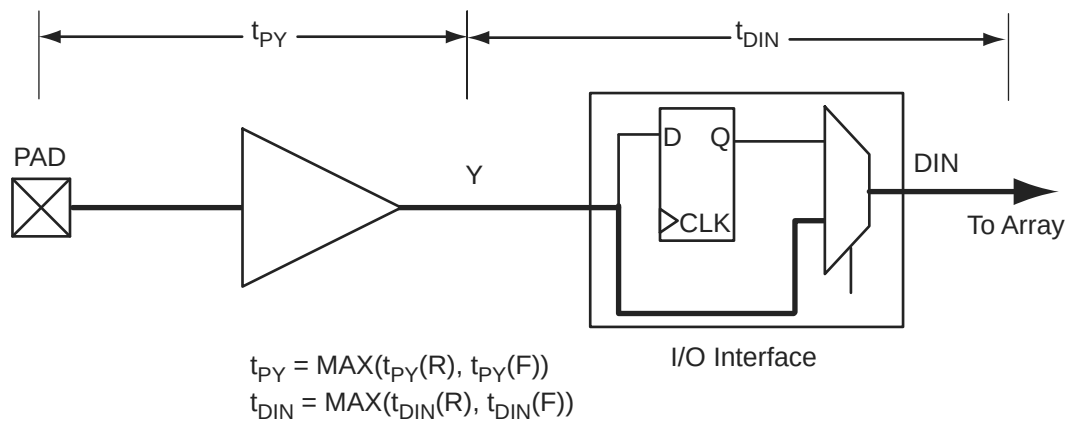


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Table 2-33 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case
Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8	High	5	–	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26	ns
3.3 V LVCMOS Wide Range ²	100 μA	8	High	5	–	0.97	2.62	0.18	1.17	0.66	2.63	2.02	2.79	3.17	ns
2.5 V LVCMOS	8 mA	8	High	5	–	0.97	1.88	0.18	1.04	0.66	1.92	1.63	1.95	2.15	ns
1.8 V LVCMOS	4 mA	4	High	5	–	0.97	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	ns
1.5 V LVCMOS	2 mA	2	High	5	–	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

Table 2-47 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-48 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

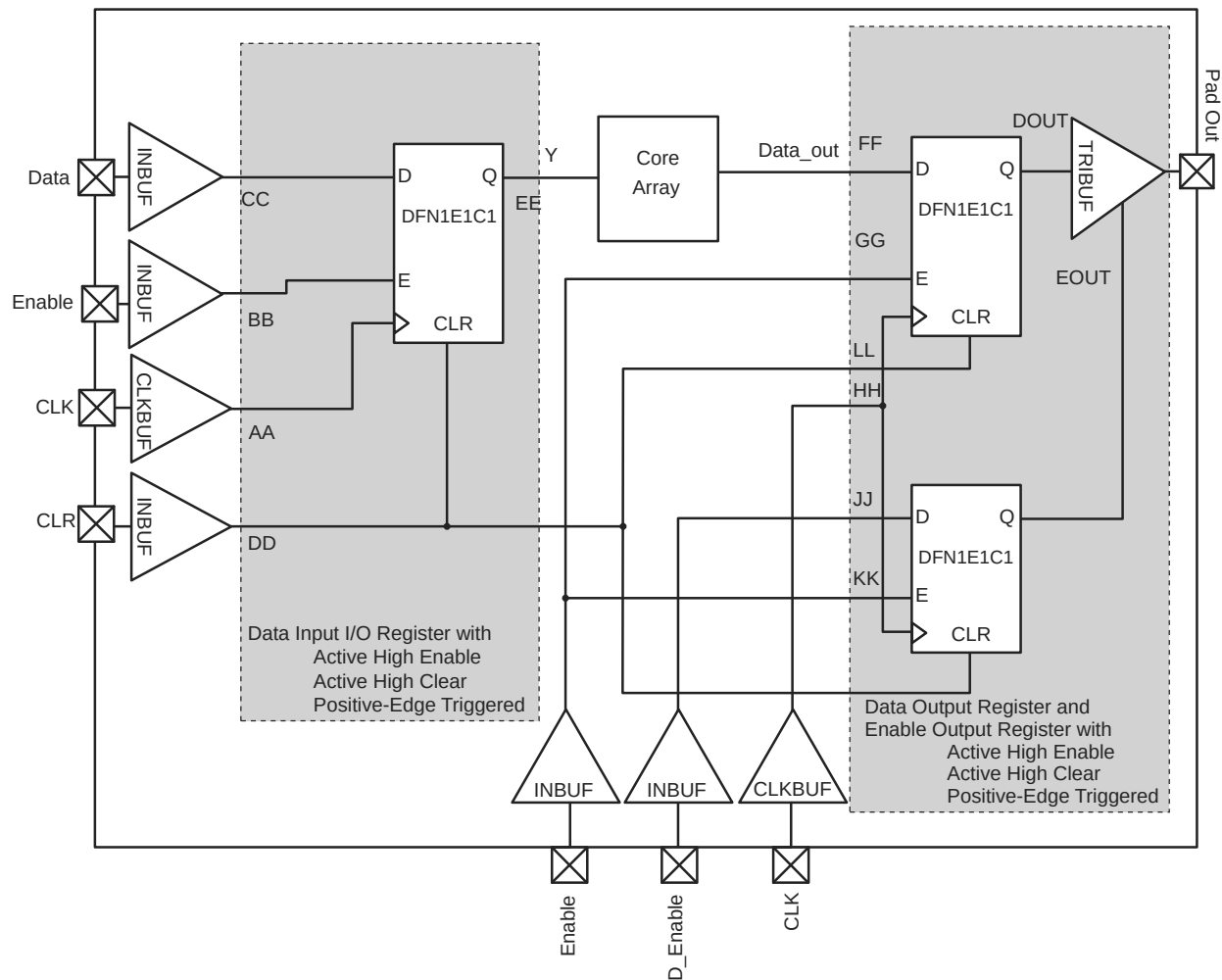


Figure 2-17 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

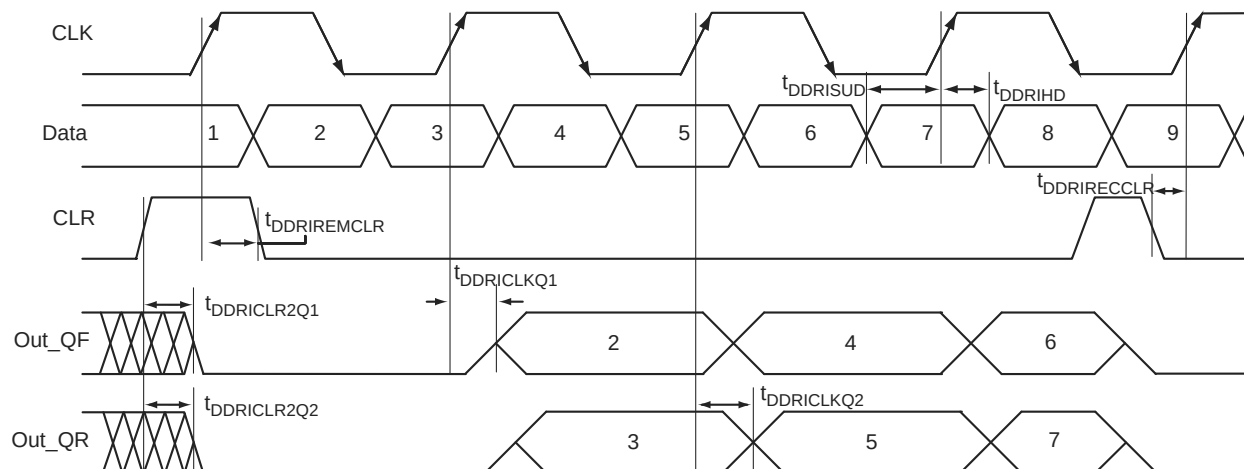


Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRIHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRIHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRIEMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRIVCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-179 • AGL600 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input High Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-180 • AGL1000 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.55	1.89	ns
t_{RCKH}	Input High Delay for Global Clock	1.60	2.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-195 • FIFO

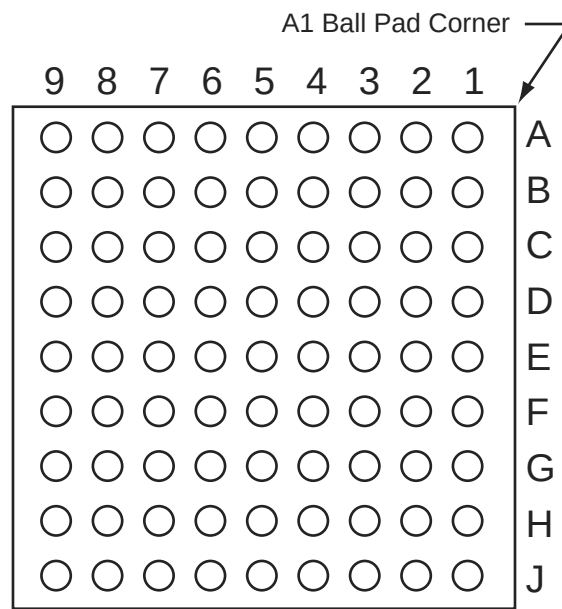
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.99	ns
t_{ENH}	REN, WEN Hold Time	0.16	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.76	ns
t_{DH}	Input Data (WD) Hold Time	0.25	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.33	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.80	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK High to Full Flag Valid	3.35	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	2.02	ns
	RESET Low to Data Out Low on RD (pipelined)	2.02	ns
t_{REMRSTB}	RESET Removal	0.61	ns
t_{RECRSTB}	RESET Recovery	3.21	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

4 – Package Pin Assignments

UC81

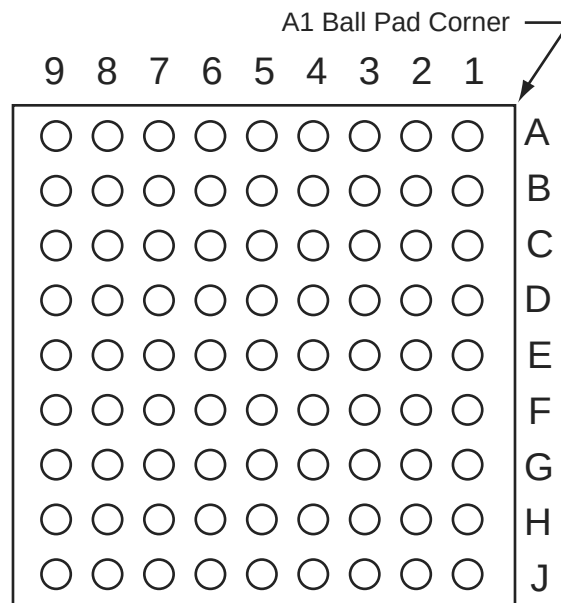


Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS81



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS196	
Pin Number	AGL125 Function
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	VCC
J8	VCC
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	VCCIB1
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	VCCIB0
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1

CS196	
Pin Number	AGL125 Function
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	VPUMP
L12	VJTAG
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	VCCIB1
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	VCCIB1
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	VCCIB1
M12	VMV1
M13	TRST
M14	VCCIB0
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI

CS196	
Pin Number	AGL125 Function
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

CS196	
Pin Number	AGL250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO10RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	IO19RSB0
A9	IO23RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO12RSB0
B7	IO16RSB0
B8	IO22RSB0
B9	IO24RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41PPB1
B14	GBB2/IO42PDB1
C1	GAC2/IO116UDB3
C2	GAB2/IO117UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO11RSB0
C7	VCCIB0
C8	IO20RSB0

CS196	
Pin Number	AGL250 Function
C9	IO30RSB0
C10	IO33RSB0
C11	VCCIB0
C12	IO41NPB1
C13	GNDQ
C14	IO42NDB1
D1	IO116VDB3
D2	IO117VDB3
D3	GAA2/IO118UDB3
D4	IO113PPB3
D5	IO08RSB0
D6	IO14RSB0
D7	IO15RSB0
D8	IO18RSB0
D9	IO25RSB0
D10	IO32RSB0
D11	IO44PPB1
D12	VMV1
D13	IO43NDB1
D14	GBC2/IO43PDB1
E1	IO112PDB3
E2	GND
E3	IO118VDB3
E4	VCCIB3
E5	IO114USB3
E6	IO07RSB0
E7	IO09RSB0
E8	IO21RSB0
E9	IO31RSB0
E10	IO34RSB0
E11	VCCIB1
E12	IO44NPB1
E13	GND
E14	IO45PDB1
F1	IO112NDB3
F2	IO107NPB3

CS196	
Pin Number	AGL250 Function
F3	IO111PDB3
F4	IO111NDB3
F5	IO113NPB3
F6	IO06RSB0
F7	VCC
F8	VCC
F9	IO28RSB0
F10	IO54PDB1
F11	IO54NDB1
F12	IO47NDB1
F13	IO47PDB1
F14	IO45NDB1
G1	GFB1/IO109PDB3
G2	GFA0/IO108NDB3
G3	GFA2/IO107PPB3
G4	VCOMPLF
G5	GFC0/IO110NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO48NDB1
G11	GCB1/IO49PDB1
G12	GCA0/IO50NDB1
G13	IO53NDB1
G14	GCC2/IO53PDB1
H1	GFB0/IO109NDB3
H2	GFA1/IO108PDB3
H3	VCCPLF
H4	GFB2/IO106PPB3
H5	GFC1/IO110PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO48PDB1

CS281	
Pin Number	AGL1000 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	VCOMPLF
J2	GFA0/IO207NDB3
J4	VCCPLF
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	VCCIB3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO96PPB1

CS281	
Pin Number	AGL1000 Function
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	VCCIB1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3

CS281	
Pin Number	AGL1000 Function
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	VCCIB2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	VCCIB2
N13	VPUMP
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2

FG144	
Pin Number	AGL1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484	
Pin Number	AGL1000 Function
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0

FG484	
Pin Number	AGL1000 Function
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3

FG484	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3

FG484	
Pin Number	AGL1000 Function
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2