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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	9216
Total RAM Bits	55296
Number of I/O	97
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl400v5-fgg144

Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 – I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Figure 1-5 • I/O States During Programming Window

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

**Table 2-22 • Different Components Contributing to the Static Power Consumption in IGLOO Device
For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-12 on page 2-9.							
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-8.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7.							
PDC4	Static PLL contribution	0.90							
PDC5	Bank quiescent power (VCCI-Dependent)	See Table 2-12 on page 2-9.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 on page 2-10 through Table 2-15 on page 2-11.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-16 on page 2-11 through Table 2-18 on page 2-12.							

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

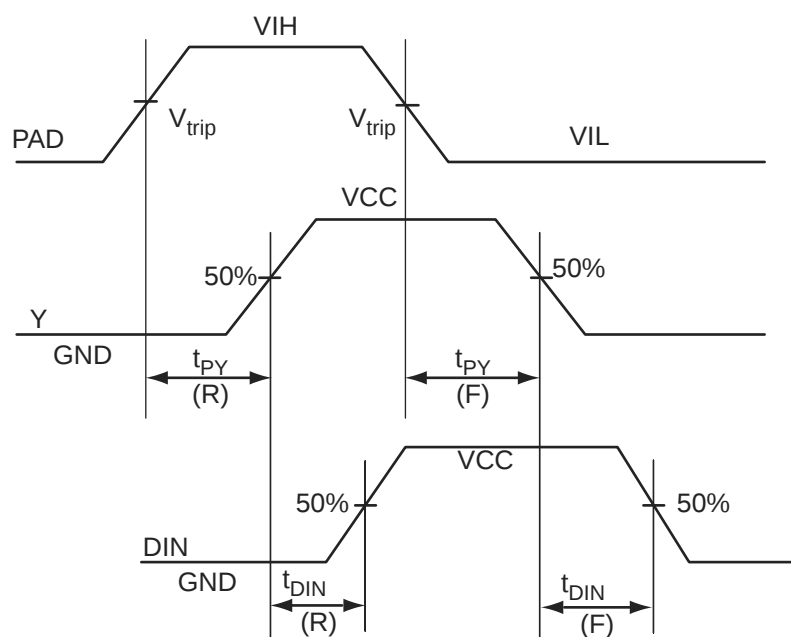
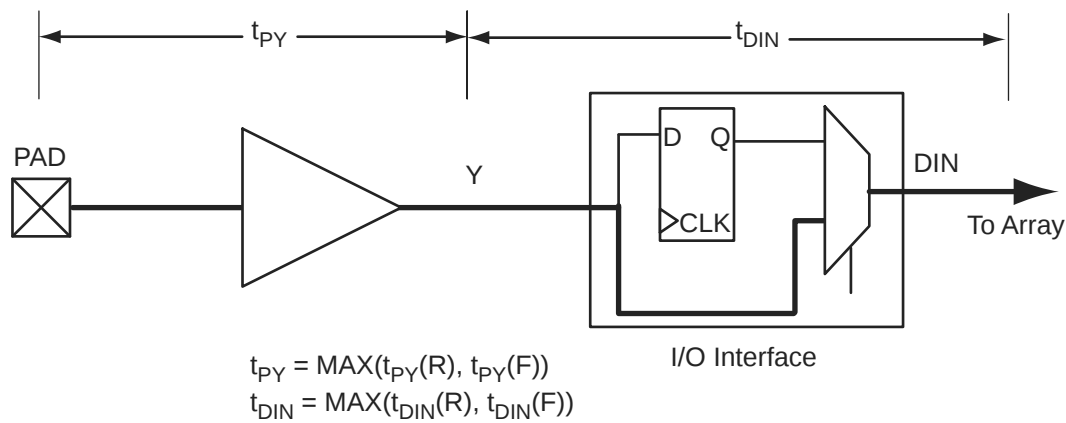


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Table 2-35 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{BOUT} (ns)	t_{BP} (ns)	t_{BIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	–	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5 V LVCMOS	12 mA	12	High	5	–	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8 V LVCMOS	8 mA	8	High	5	–	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5 V LVCMOS	4 mA	4	High	5	–	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2 V LVCMOS	2 mA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2 V LVCMOS Wide Range ³	100 μA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ²	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ²	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Notes:

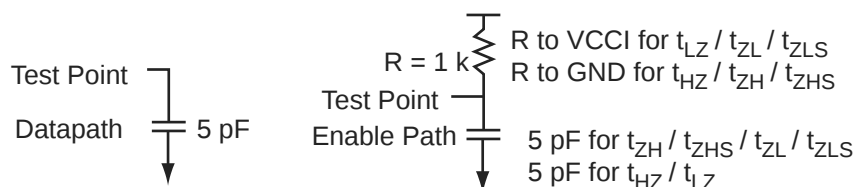
1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
5. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-97 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-9 • AC Loading****Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-99 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

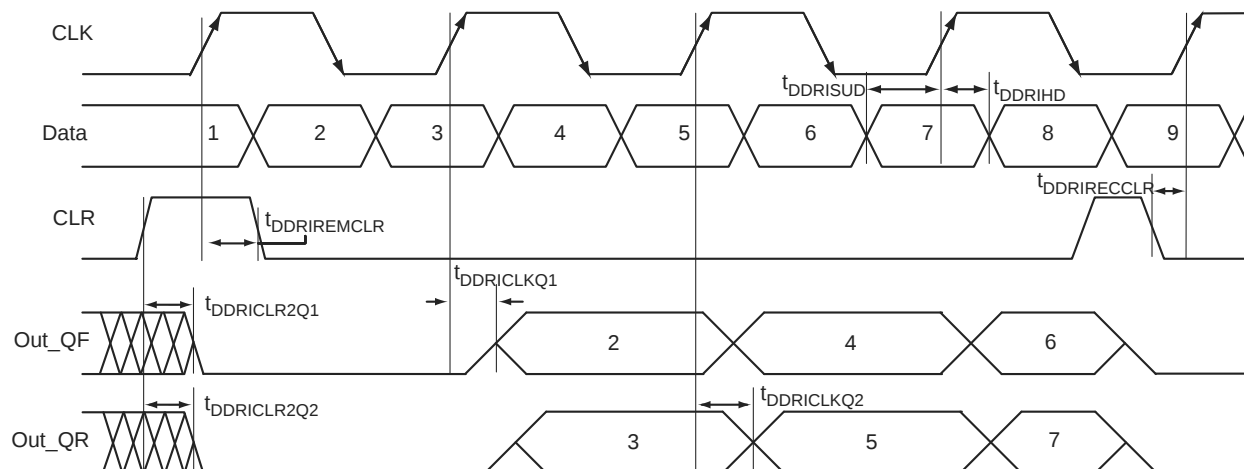


Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-165 • Input DDR Propagation Delays****Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.76	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.94	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.93	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.84	ns
t_{DDRILD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRILD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
t_{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

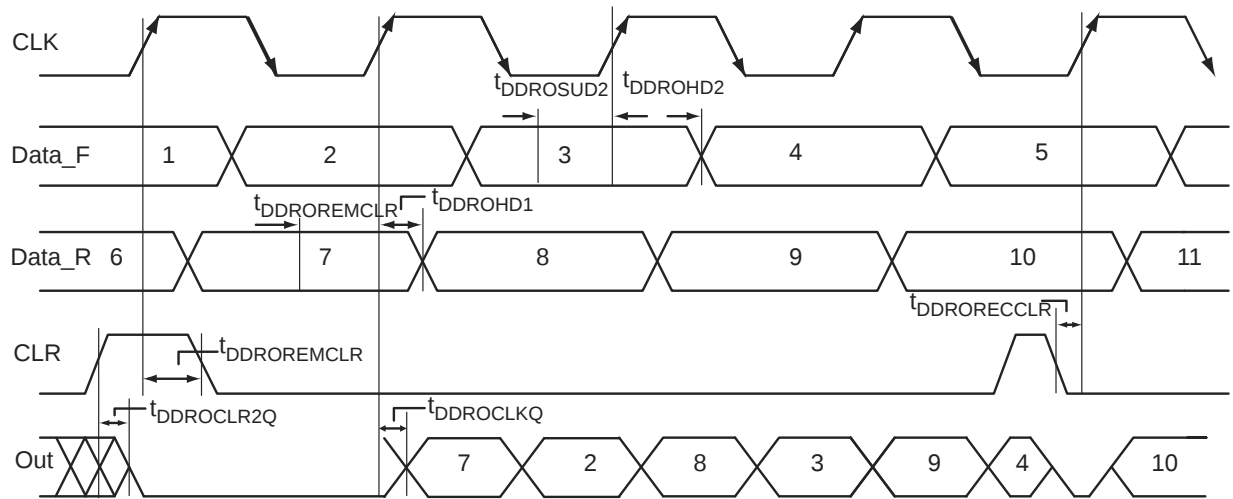


Figure 2-24 • Output DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-167 • Output DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	1.07	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.67	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.67	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-196 • FIFO****Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.13	ns
t_{ENH}	REN, WEN Hold Time	0.31	ns
t_{BKS}	BLK Setup Time	0.47	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	1.56	ns
t_{DH}	Input Data (WD) Hold Time	0.49	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	6.80	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	3.62	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK High to Full Flag Valid	6.85	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	4.09	ns
	RESET Low to Data Out Low on RD (pipelined)	4.09	ns
t_{REMRSTB}	RESET Removal	1.23	ns
t_{RECRSTB}	RESET Recovery	6.58	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-199 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
t_{TRSTREM}	ResetB Removal Time	0.58	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

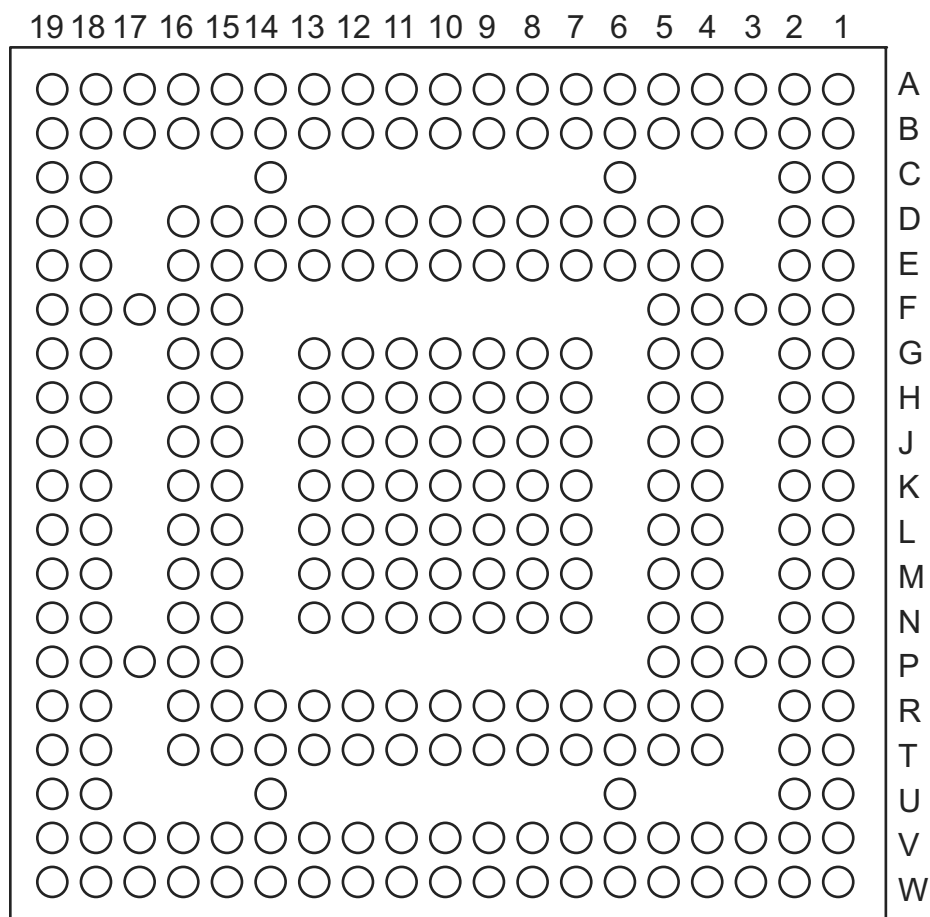
Table 2-200 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
t_{TRSTREM}	ResetB Removal Time	1.18	ns
t_{TRSTREC}	ResetB Recovery Time	0.00	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

CS281



Note: This is the bottom view of the package.

Note

For more information on package drawings, see PD3068: *Package Mechanical Drawings*.

CS281	
Pin Number	AGL1000 Function
R15	IO122RSB2
R16	GDA1/IO113PPB1
R18	GDB0/IO112NPB1
R19	GDC0/IO111NPB1
T1	IO197PPB3
T2	GEC0/IO190NPB3
T4	GEB0/IO189NPB3
T5	IO181RSB2
T6	IO172RSB2
T7	IO171RSB2
T8	IO156RSB2
T9	IO159RSB2
T10	GND
T11	IO139RSB2
T12	IO138RSB2
T13	IO129RSB2
T14	IO123RSB2
T15	GDC2/IO116RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO112PPB1
U1	IO193PDB3
U2	GEA1/IO188PPB3
U6	IO167RSB2
U14	IO128RSB2
U18	TRST
U19	GDA0/IO113NPB1
V1	IO193NDB3
V2	VCCIB3
V3	GEC2/IO185RSB2
V4	IO182RSB2
V5	IO175RSB2
V6	GND
V7	IO161RSB2
V8	IO143RSB2
V9	IO146RSB2

CS281	
Pin Number	AGL1000 Function
V10	IO145RSB2
V11	IO144RSB2
V12	IO134RSB2
V13	IO133RSB2
V14	GND
V15	IO119RSB2
V16	GDA2/IO114RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO186RSB2
W3	IO183RSB2
W4	IO176RSB2
W5	IO170RSB2
W6	IO162RSB2
W7	IO157RSB2
W8	IO152RSB2
W9	IO149RSB2
W10	VCCIB2
W11	IO140RSB2
W12	IO135RSB2
W13	IO130RSB2
W14	IO125RSB2
W15	IO120RSB2
W16	IO118RSB2
W17	GDB2/IO115RSB2
W18	TCK
W19	GND

QN132	
Pin Number	AGL250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG144	
Pin Number	AGL400 Function
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	AGL600 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	VCC
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	VCC
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

FG144	
Pin Number	AGL600 Function
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	VCC
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	VCCIB3
E5	IO174NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO69PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	VCOMPLF
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1

FG144	
Pin Number	AGL600 Function
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	VCC
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	VCC
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	VCCIB1
H11	IO84PSB1
H12	VCC
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	VCCIB3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	VCC
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1

FG256	
Pin Number	AGL600 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL600 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL600 Function
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3

FG484	
Pin Number	AGL400 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO67PPB1
K17	IO64NPB1
K18	IO73PDB1
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC

FG484	
Pin Number	AGL1000 Function
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	VCC
K10	GND

Revision / Version	Changes	Page
Revision 18 (Nov 2009)	The version changed to v2.0 for IGLOO datasheet chapters, indicating the datasheet contains information based on final characterization. Please review the datasheet carefully as most tables were updated with new data.	N/A
Revision 17 (Sep 2009) Product Brief v1.6	The "Reprogrammable Flash Technology" section was modified to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	"IGLOO Ordering Information" was revised to note that halogen-free packages are available with RoHS-compliant packaging.	III
	Table 1-1 • I/O Standards Supported is new.	1-7
	The definitions of hot-swap and cold-sparing were added to the "I/Os with Advanced I/O Standards" section.	1-7
Revision 16 (Apr 2009) Product Brief v1.5	M1AGL400 is no longer offered and was removed from the "IGLOO Devices" product table, "IGLOO Ordering Information", and "Temperature Grade Offerings".	I, III, IV
	The –F speed grade is no longer offered for IGLOO devices. The speed grade column and note regarding –F speed grade were removed from "IGLOO Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
	This datasheet now has fully characterized data and has moved from being Advance to a Production version. The version number changed from Advance v0.5 to v2.0. Please review the datasheet carefully as most tables were updated with new data.	N/A
DC and Switching Characteristics Advance v0.6	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-5 • Package Thermal Resistivities was updated.	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$) were updated.	2-7
	In Table 2-191 • RAM4K9 and Table 2-193 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-122 and 2-124
	In Table 2-192 • RAM512X18 and Table 2-194 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-123 and 2-125
Revision 15 (Feb 2009) Packaging v1.9	The "QN132" pin table for the AGL060 device is new.	4-31