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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	97
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl600v2-fg144t

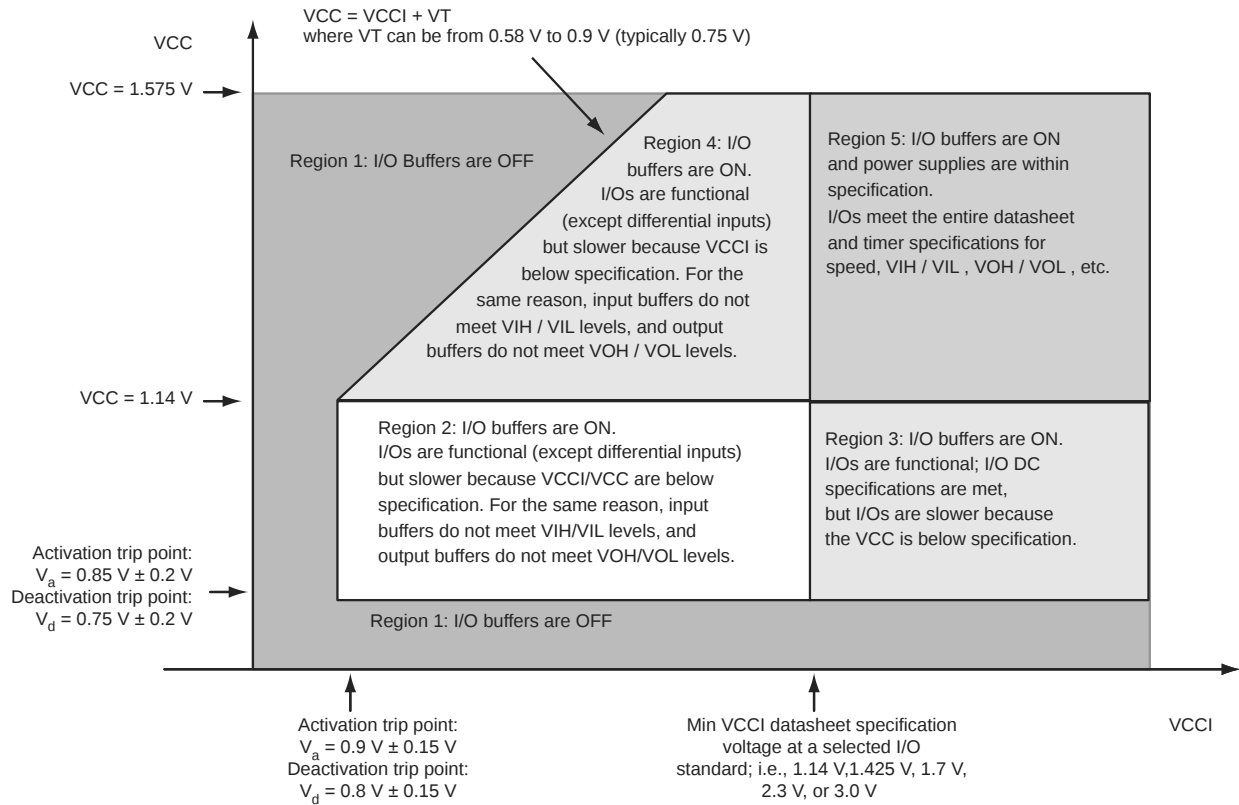


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution— P_{PLL}

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.[†]

[†] If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.

Table 2-39 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS ⁴	2 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$
4. Applicable to IGLOO V2 Devices operating at $VCCI \geq VCC$

Table 2-75 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 μA	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 μA	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 μA	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 μA	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 μA	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-76 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 μA	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 μA	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 μA	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 μA	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 μA	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-115 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-116 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-117 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-118 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

DDR Module Specifications

Input DDR Module

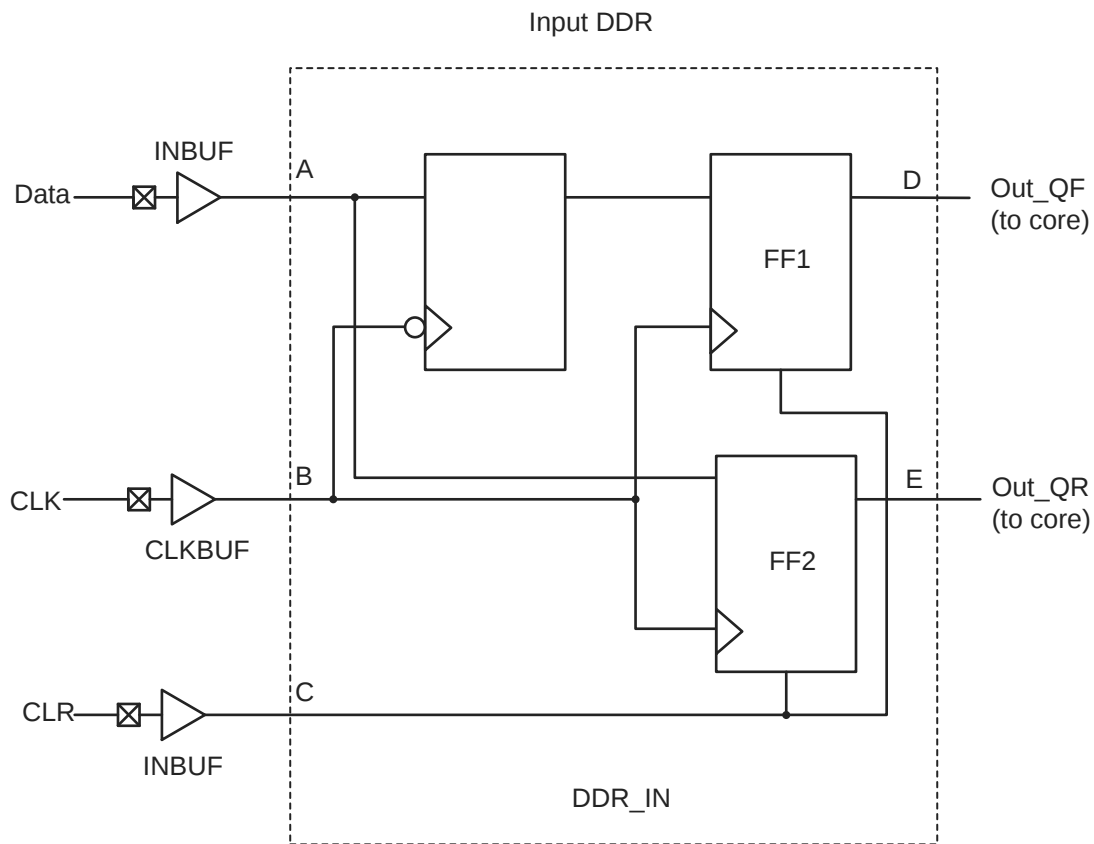


Figure 2-21 • Input DDR Timing Model

Table 2-163 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDRICKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRICKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup Time of DDR input	A, B
t_{DDRIRD}	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

Table 2-185 • AGL250 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-186 • AGL400 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.18	2.64	ns
t_{RCKH}	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

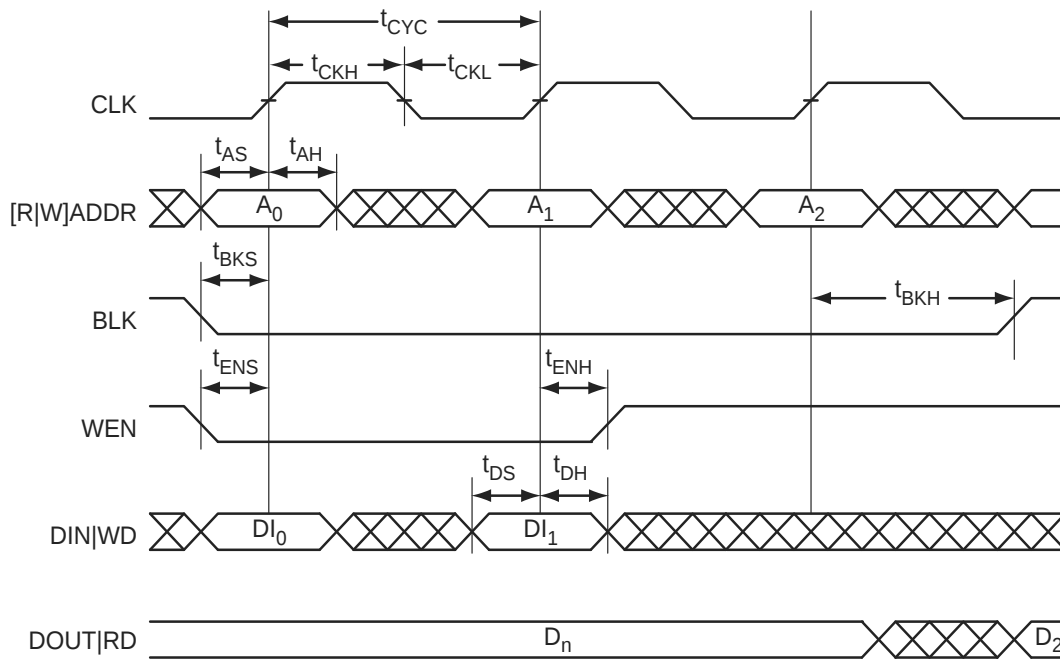


Figure 2-34 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

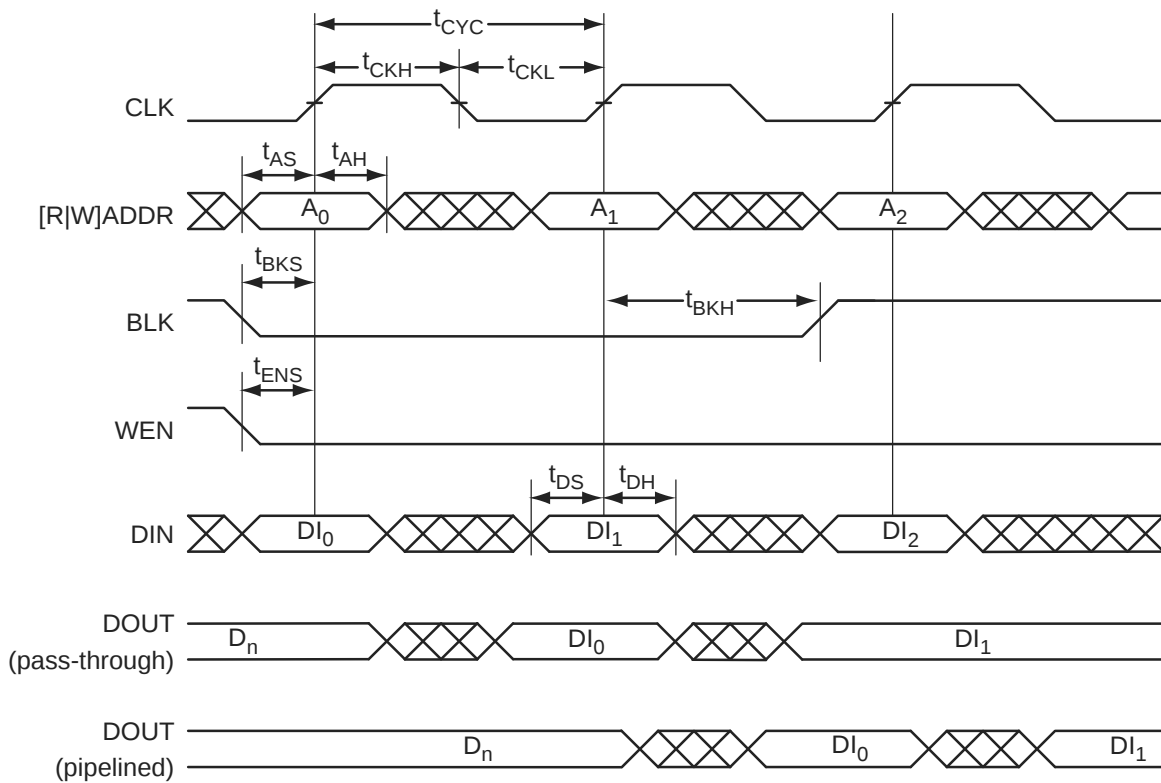


Figure 2-35 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.

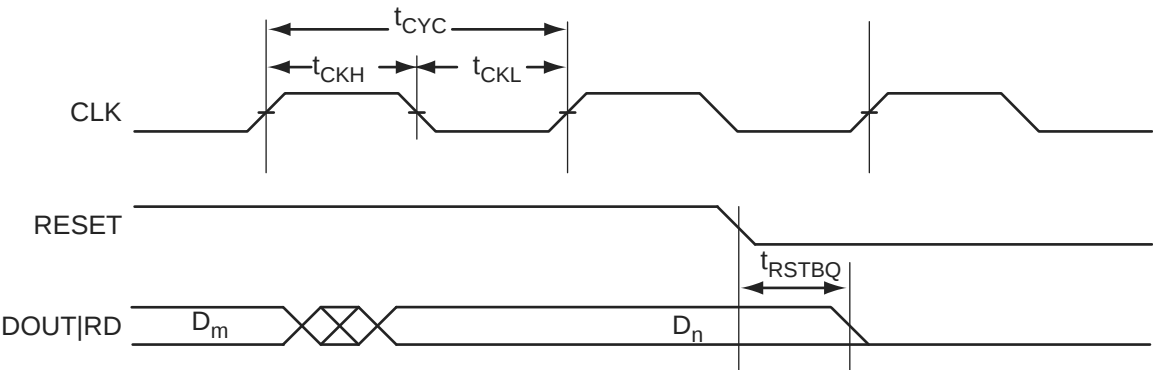


Figure 2-36 • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.

Timing Waveforms

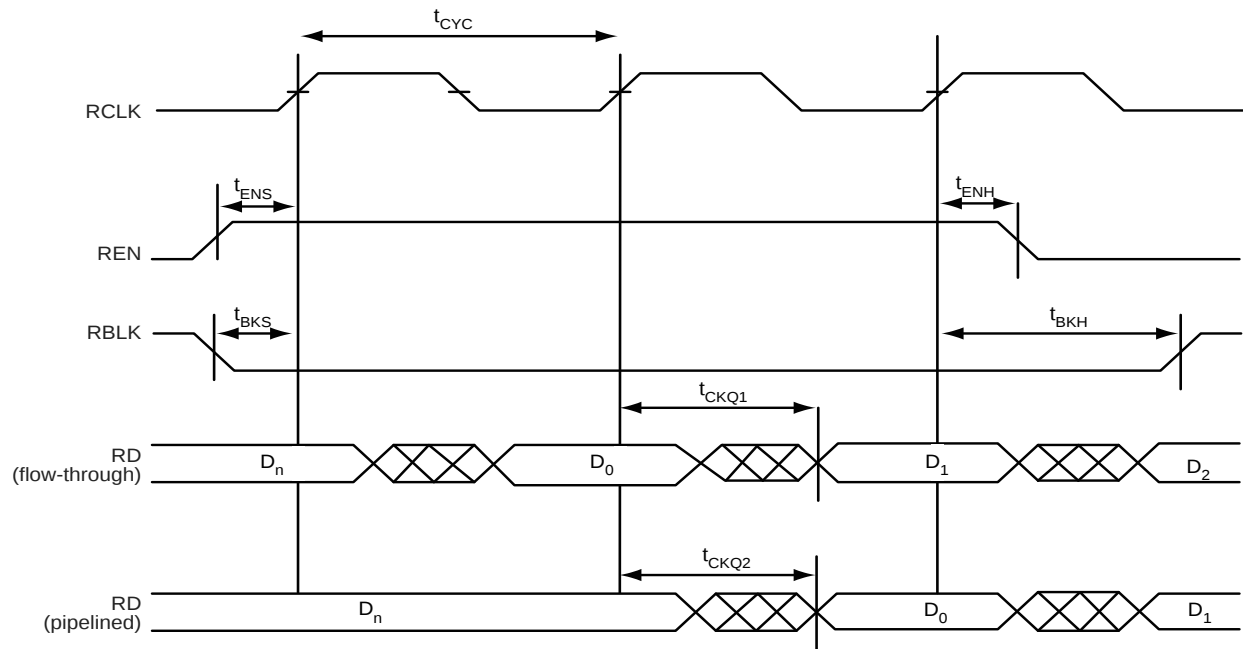


Figure 2-38 • FIFO Read

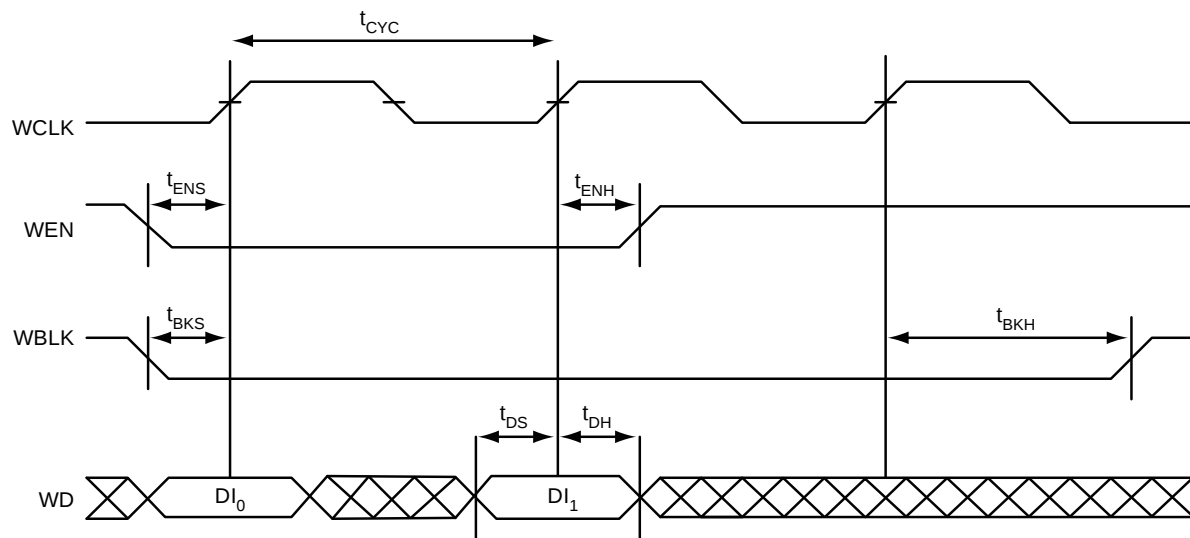


Figure 2-39 • FIFO Write

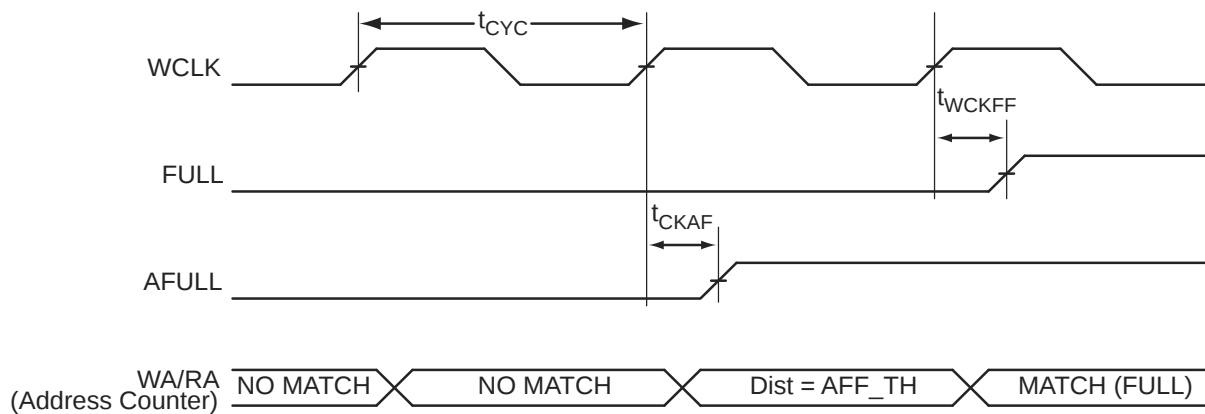


Figure 2-42 • FIFO FULL Flag and AFULL Flag Assertion

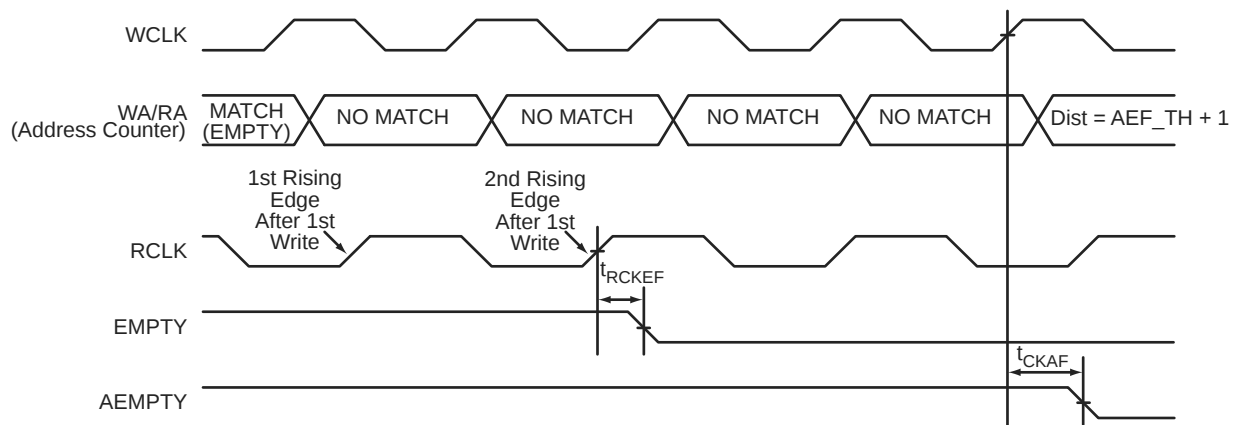


Figure 2-43 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

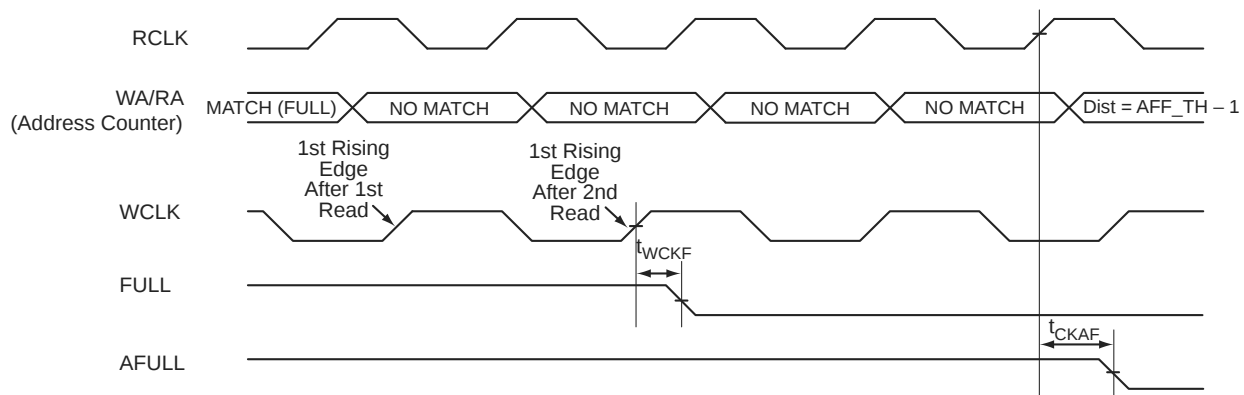


Figure 2-44 • FIFO FULL Flag and AFULL Flag Deassertion

CS281	
Pin Number	AGL1000 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO13RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO20RSB0
A8	IO24RSB0
A9	IO29RSB0
A10	VCCIB0
A11	IO39RSB0
A12	IO45RSB0
A13	IO48RSB0
A14	IO58RSB0
A15	IO61RSB0
A16	IO62RSB0
A17	GBC1/IO73RSB0
A18	GBA0/IO76RSB0
A19	GND
B1	GAA2/IO225PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO12RSB0
B6	GND
B7	IO21RSB0
B8	IO26RSB0
B9	IO34RSB0
B10	IO35RSB0
B11	IO36RSB0
B12	IO46RSB0
B13	IO52RSB0
B14	GND
B15	IO59RSB0
B16	GBC0/IO72RSB0
B17	GBA1/IO77RSB0

CS281	
Pin Number	AGL1000 Function
B18	VCCIB1
B19	IO79NDB1
C1	GAB2/IO224PPB3
C2	IO225NPB3
C6	IO18RSB0
C14	IO63RSB0
C18	IO78NPB1
C19	GBB2/IO79PDB1
D1	IO219PPB3
D2	IO223NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO15RSB0
D7	IO19RSB0
D8	IO27RSB0
D9	IO32RSB0
D10	GND
D11	IO38RSB0
D12	IO44RSB0
D13	IO47RSB0
D14	IO60RSB0
D15	GBB0/IO74RSB0
D16	GBA2/IO78PPB1
D18	GBC2/IO80PPB1
D19	IO88NPB1
E1	IO217NPB3
E2	IO221PPB3
E4	IO221NPB3
E5	IO10RSB0
E6	IO14RSB0
E7	IO25RSB0
E8	IO28RSB0
E9	IO31RSB0
E10	IO33RSB0
E11	IO42RSB0
E12	IO49RSB0

CS281	
Pin Number	AGL1000 Function
E13	IO53RSB0
E14	GBB1/IO75RSB0
E15	IO80NPB1
E16	IO85PPB1
E18	IO83PPB1
E19	IO84NPB1
F1	IO214NPB3
F2	GND
F3	IO217PPB3
F4	IO219NPB3
F5	IO224NPB3
F15	IO85NPB1
F16	IO84PPB1
F17	IO83NPB1
F18	GND
F19	IO90PPB1
G1	IO212NPB3
G2	IO211NDB3
G4	IO214PPB3
G5	IO212PPB3
G7	GAC2/IO223PPB3
G8	VCCIB0
G9	IO30RSB0
G10	IO37RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO88PPB1
G15	IO89NDB1
G16	IO89PDB1
G18	GCC0/IO91NPB1
G19	GCB1/IO92PPB1
H1	GFB0/IO208NPB3
H2	IO211PDB3
H4	GFC1/IO209PPB3
H5	GFB1/IO208PPB3
H7	VCCIB3

QN132	
Pin Number	AGL060 Function
C16	IO60RSB1
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG484	
Pin Number	AGL400 Function
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO15RSB0
A7	IO18RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO35RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO50RSB0
A17	IO51RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	NC
AA7	NC
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

FG484	
Pin Number	AGL400 Function
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

FG484	
Pin Number	AGL400 Function
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	AGL600 Function
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

FG484	
Pin Number	AGL1000 Function
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0

FG484	
Pin Number	AGL1000 Function
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	VCC
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3