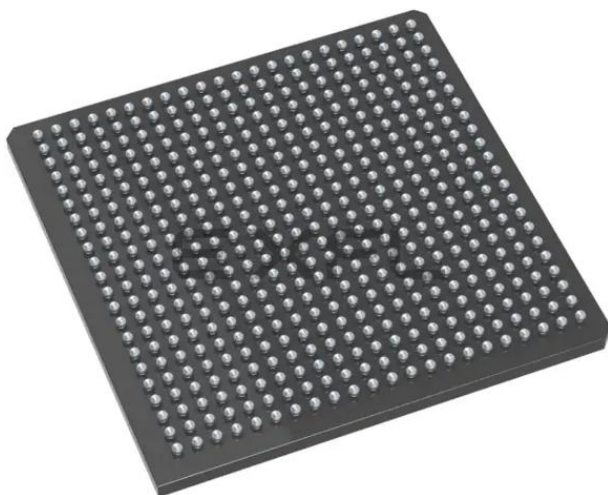




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	235
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/agl600v2-fg484i

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microsemi Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24 on page 2-19. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide*.

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Table 2-40 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{OH_{spec}}$

Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK PULL-UP)}$ ¹ (Ω)		$R_{(WEAK PULL-DOWN)}$ ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V Wide Range I/Os	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULLDOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULLDOWN-MIN)}$

Timing Characteristics***Applies to 1.5 V DC Core Voltage*****Table 2-83 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.***Table 2-84 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-85 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-111 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Notes:

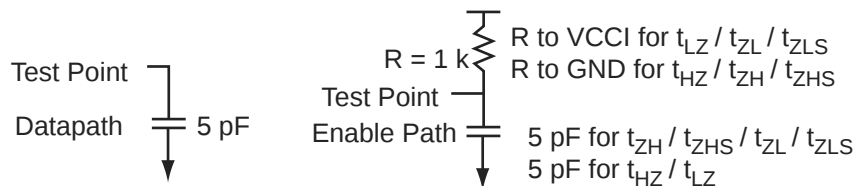
1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-112 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-11 • AC Loading****Table 2-130 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.2	0.6	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics

1.2 V DC Core Voltage

Table 2-131 • 1.2 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	8.37	0.26	1.60	1.10	8.04	7.17	3.94	3.52	13.82	12.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-132 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-133 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	7.59	0.26	1.59	1.10	7.29	6.54	3.30	3.35	13.08	12.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-134 • 1.2 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14. The input and output buffer delays are available in the LVDS section in Table 2-149 on page 2-81 and Table 2-150 on page 2-81.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

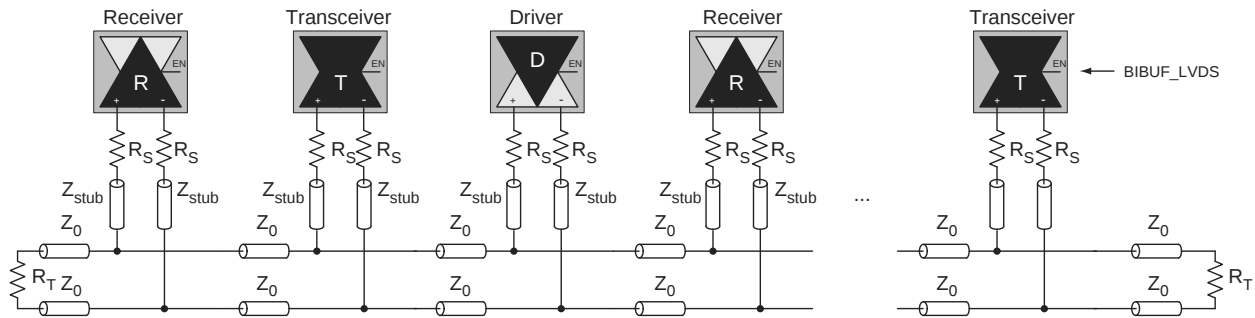


Figure 2-14 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

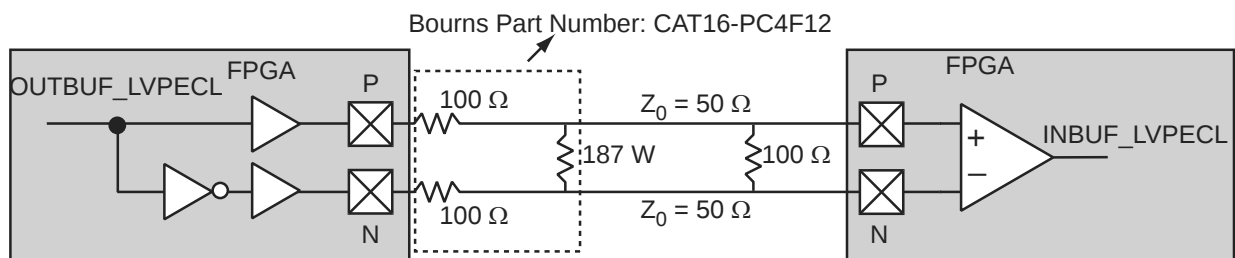


Figure 2-15 • LVPECL Circuit Diagram and Board-Level Implementation

DDR Module Specifications

Input DDR Module

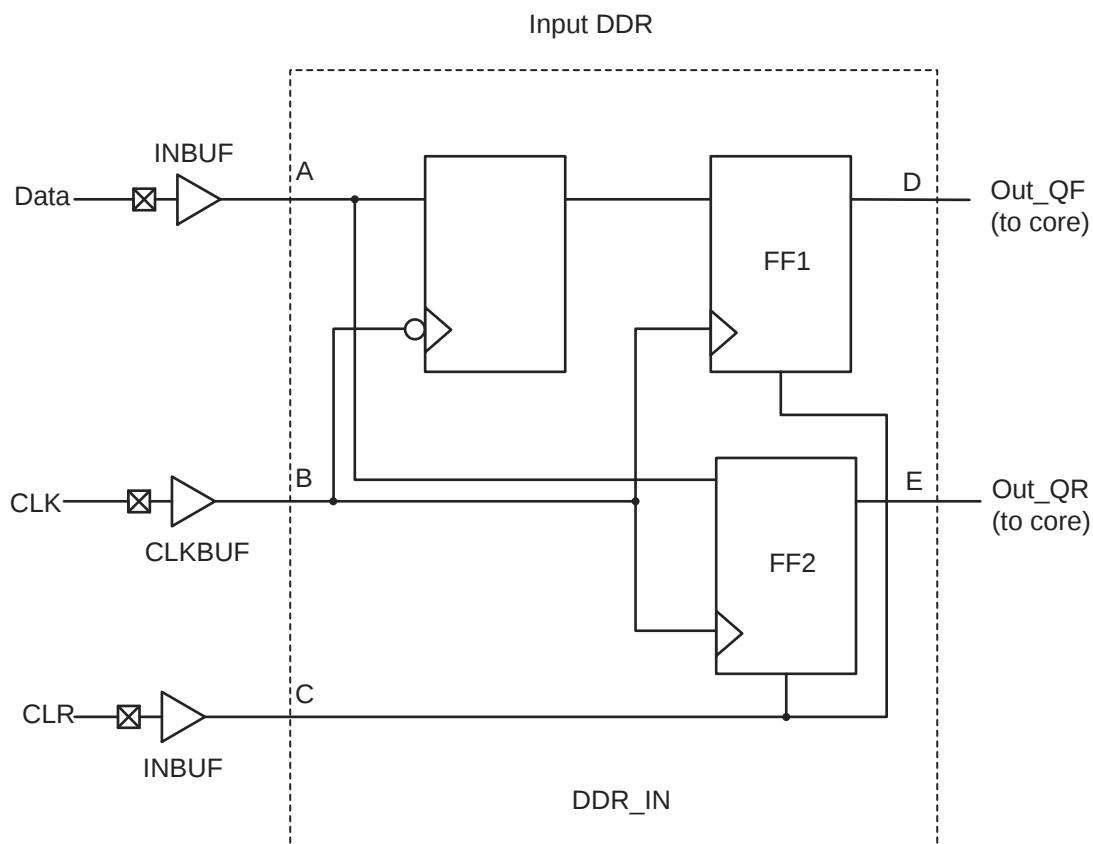


Figure 2-21 • Input DDR Timing Model

Table 2-163 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDRICKQ1}	Clock-to-Out Out_QR	B, D
t_{DDRICKQ2}	Clock-to-Out Out_QF	B, E
t_{DDRISUD}	Data Setup Time of DDR input	A, B
t_{DDRIRD}	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B

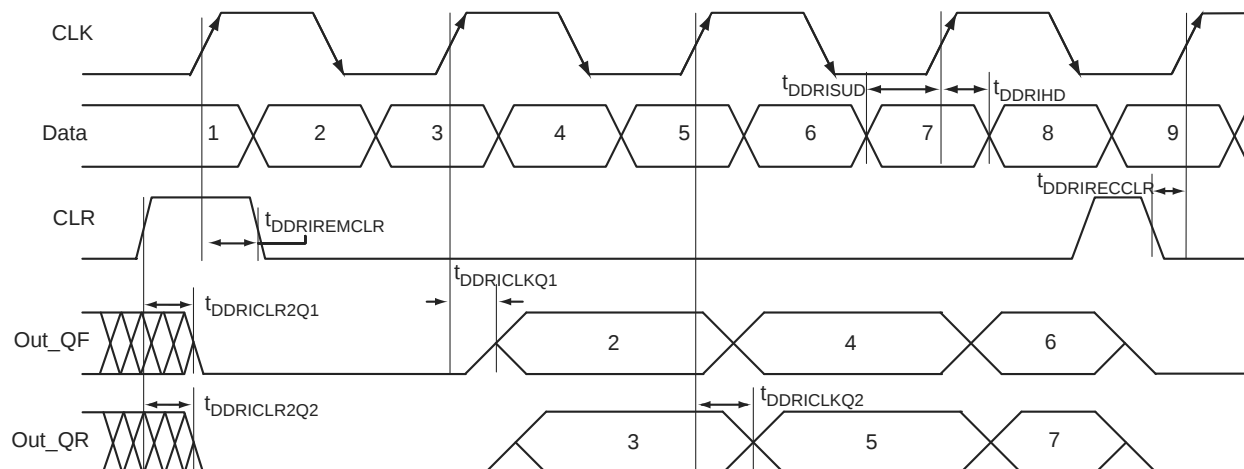


Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-179 • AGL600 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input High Delay for Global Clock	1.52	1.94	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-180 • AGL1000 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.55	1.89	ns
t_{RCKH}	Input High Delay for Global Clock	1.60	2.02	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	1.18		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Embedded SRAM and FIFO Characteristics

SRAM

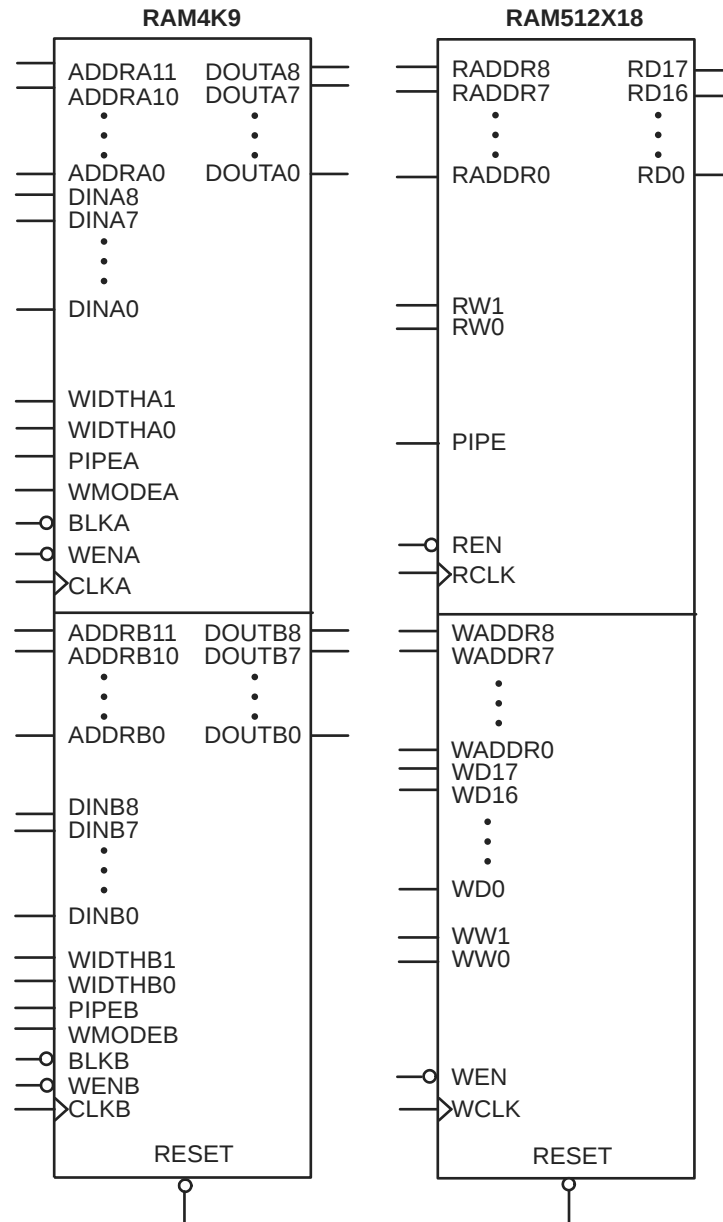


Figure 2-31 • RAM Models

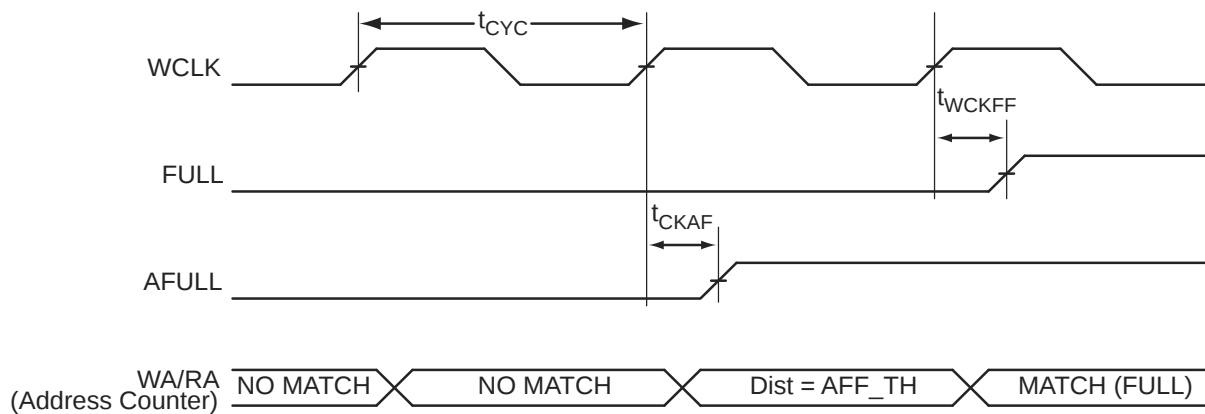


Figure 2-42 • FIFO FULL Flag and AFULL Flag Assertion

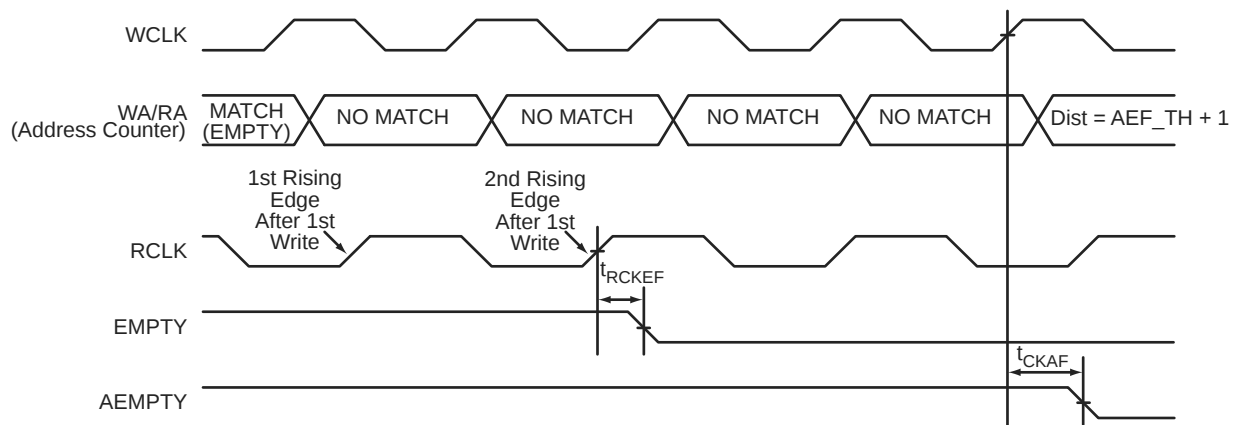


Figure 2-43 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

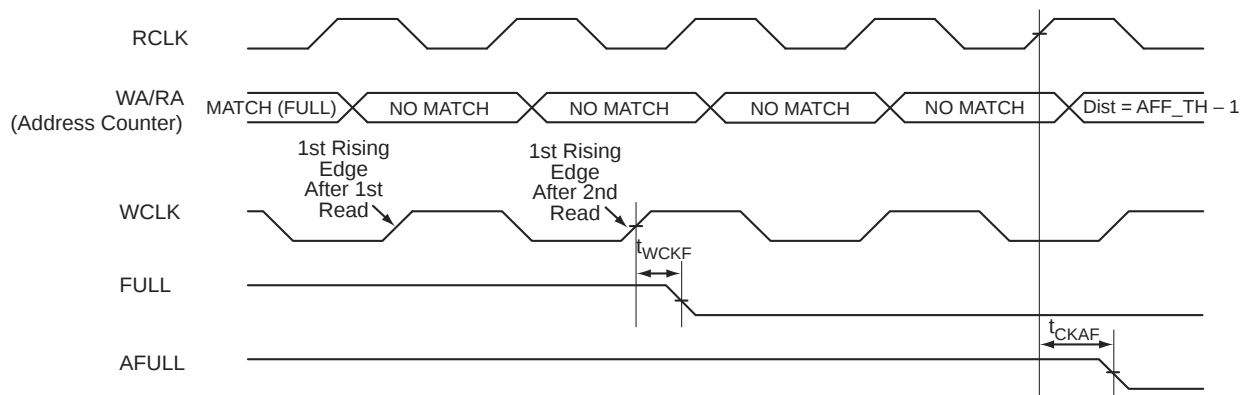
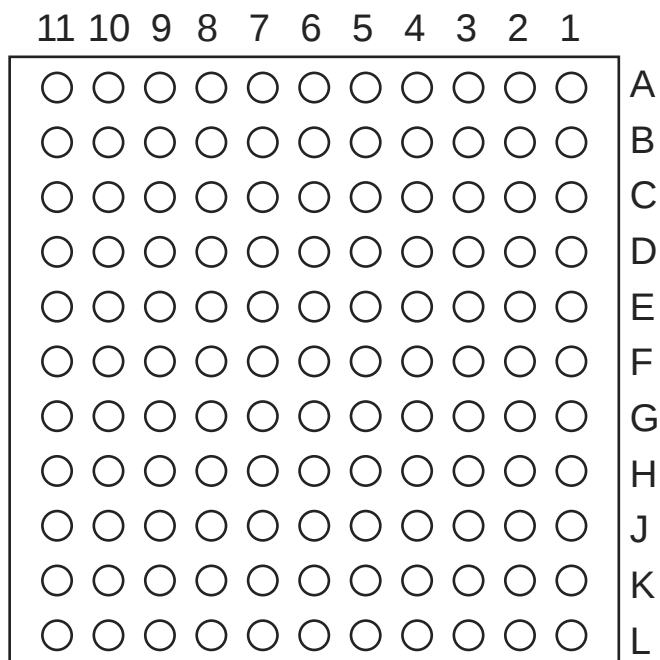


Figure 2-44 • FIFO FULL Flag and AFULL Flag Deassertion

CS121



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS121		CS121		CS121	
Pin Number	AGL060 Function	Pin Number	AGL060 Function	Pin Number	AGL060 Function
A1	GNDQ	D4	IO10RSB0	G7	VCC
A2	IO01RSB0	D5	IO11RSB0	G8	GDC0/IO46RSB0
A3	GAA1/IO03RSB0	D6	IO18RSB0	G9	GDA1/IO49RSB0
A4	GAC1/IO07RSB0	D7	IO32RSB0	G10	GDB0/IO48RSB0
A5	IO15RSB0	D8	IO31RSB0	G11	GCA0/IO40RSB0
A6	IO13RSB0	D9	GCA2/IO41RSB0	H1	IO75RSB1
A7	IO17RSB0	D10	IO30RSB0	H2	IO76RSB1
A8	GBB1/IO22RSB0	D11	IO33RSB0	H3	GFC2/IO78RSB1
A9	GBA1/IO24RSB0	E1	IO87RSB1	H4	GFA2/IO80RSB1
A10	GNDQ	E2	GFC0/IO85RSB1	H5	IO77RSB1
A11	VMV0	E3	IO92RSB1	H6	GEC2/IO66RSB1
B1	GAA2/IO95RSB1	E4	IO94RSB1	H7	IO54RSB1
B2	IO00RSB0	E5	VCC	H8	GDC2/IO53RSB1
B3	GAA0/IO02RSB0	E6	VCCIB0	H9	VJTAG
B4	GAC0/IO06RSB0	E7	GND	H10	TRST
B5	IO08RSB0	E8	GCC0/IO36RSB0	H11	IO44RSB0
B6	IO12RSB0	E9	IO34RSB0	J1	GEC1/IO74RSB1
B7	IO16RSB0	E10	GCB1/IO37RSB0	J2	GEC0/IO73RSB1
B8	GBC1/IO20RSB0	E11	GCC1/IO35RSB0	J3	GEB1/IO72RSB1
B9	GBB0/IO21RSB0	F1*	VCOMPLF	J4	GEA0/IO69RSB1
B10	GBB2/IO27RSB0	F2	GFB0/IO83RSB1	J5	FF/GEB2/IO67RSB1
B11	GBA2/IO25RSB0	F3	GFA0/IO82RSB1	J6	IO62RSB1
C1	IO89RSB1	F4	GFC1/IO86RSB1	J7	GDA2/IO51RSB1
C2	GAC2/IO91RSB1	F5	VCCIB1	J8	GDB2/IO52RSB1
C3	GAB1/IO05RSB0	F6	VCC	J9	TDI
C4	GAB0/IO04RSB0	F7	VCCIB0	J10	TDO
C5	IO09RSB0	F8	GCB2/IO42RSB0	J11	GDC1/IO45RSB0
C6	IO14RSB0	F9	GCC2/IO43RSB0	K1	GEB0/IO71RSB1
C7	GBA0/IO23RSB0	F10	GCB0/IO38RSB0	K2	GEA1/IO70RSB1
C8	GBC0/IO19RSB0	F11	GCA1/IO39RSB0	K3	GEA2/IO68RSB1
C9	IO26RSB0	G1*	VCCPLF	K4	IO64RSB1
C10	IO28RSB0	G2	GFB2/IO79RSB1	K5	IO60RSB1
C11	GBC2/IO29RSB0	G3	GFA1/IO81RSB1	K6	IO59RSB1
D1	IO88RSB1	G4	GFB1/IO84RSB1	K7	IO56RSB1
D2	IO90RSB1	G5	GND	K8	TCK
D3	GAB2/IO93RSB1	G6	VCCIB1	K9	TMS

Note: *Pin numbers F1 and G1 must be connected to ground because a PLL is not supported for AGL060-CS/G121.

CS196	
Pin Number	AGL125 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	AGL125 Function
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	AGL125 Function
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

CS281	
Pin Number	AGL600 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO68NPB1
H16	GCB0/IO70NPB1
H18	GCA1/IO71PPB1
H19	GCA2/IO72PPB1
J1	VCOMPLF
J2	GFA0/IO162NDB3
J4	VCCPLF
J5	GFC0/IO164NPB3
J7	GFA2/IO161PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO69PPB1
J15	GCA0/IO71NPB1
J16	GCB2/IO73PPB1
J18	IO72NPB1
J19	IO75PSB1
K1	VCCIB3
K2	GFA1/IO162PDB3
K4	GND
K5	IO159NPB3
K7	IO161NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO74PPB1

CS281	
Pin Number	AGL600 Function
K15	IO73NPB1
K16	GND
K18	IO74NPB1
K19	VCCIB1
L1	GFB2/IO160PDB3
L2	IO160NDB3
L4	GFC2/IO159PPB3
L5	IO153PPB3
L7	IO153NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO76PPB1
L15	IO76NPB1
L16	IO77PPB1
L18	IO78NPB1
L19	IO77NPB1
M1	IO158PDB3
M2	IO158NDB3
M4	IO154NPB3
M5	IO152PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO79NPB1
M16	IO81NPB1
M18	IO79PPB1
M19	IO78PPB1
N1	IO154PPB3
N2	IO152NPB3

CS281	
Pin Number	AGL600 Function
N4	IO150PPB3
N5	IO148NPB3
N7	GEA2/IO143RSB2
N8	VCCIB2
N9	IO117RSB2
N10	IO115RSB2
N11	IO114RSB2
N12	VCCIB2
N13	VPUMP
N15	IO82PPB1
N16	IO85PPB1
N18	IO82NPB1
N19	IO81PPB1
P1	IO151PDB3
P2	GND
P3	IO151NDB3
P4	IO149PPB3
P5	GEA0/IO144NPB3
P15	IO83NDB1
P16	IO83PDB1
P17	GDC1/IO86PPB1
P18	GND
P19	IO85NPB1
R1	IO150NPB3
R2	IO149NPB3
R4	GEC1/IO146PPB3
R5	GEB1/IO145PPB3
R6	IO138RSB2
R7	IO127RSB2
R8	IO123RSB2
R9	IO118RSB2
R10	IO111RSB2
R11	IO106RSB2
R12	IO103RSB2
R13	IO97RSB2
R14	IO95RSB2

QN132	
Pin Number	AGL030 Function
A1	IO80RSB1
A2	IO77RSB1
A3	NC
A4	IO76RSB1
A5	GEC0/IO73RSB1
A6	NC
A7	GEB0/IO71RSB1
A8	IO69RSB1
A9	NC
A10	VCC
A11	IO67RSB1
A12	IO64RSB1
A13	IO59RSB1
A14	IO56RSB1
A15	NC
A16	IO55RSB1
A17	IO53RSB1
A18	VCC
A19	IO50RSB1
A20	IO48RSB1
A21	IO45RSB1
A22	IO44RSB1
A23	IO43RSB1
A24	TDI
A25	TRST
A26	IO40RSB0
A27	NC
A28	IO39RSB0
A29	IO38RSB0
A30	IO36RSB0
A31	IO35RSB0
A32	GDC0/IO32RSB0
A33	NC
A34	VCC
A35	IO30RSB0
A36	IO27RSB0

QN132	
Pin Number	AGL030 Function
A37	IO22RSB0
A38	IO19RSB0
A39	NC
A40	IO18RSB0
A41	IO16RSB0
A42	IO14RSB0
A43	VCC
A44	IO11RSB0
A45	IO08RSB0
A46	IO06RSB0
A47	IO05RSB0
A48	IO02RSB0
B1	IO81RSB1
B2	IO78RSB1
B3	GND
B4	IO75RSB1
B5	NC
B6	GND
B7	IO70RSB1
B8	NC
B9	GND
B10	IO66RSB1
B11	IO63RSB1
B12	FF/IO60RSB1
B13	IO57RSB1
B14	GND
B15	IO54RSB1
B16	IO52RSB1
B17	GND
B18	IO49RSB1
B19	IO46RSB1
B20	GND
B21	IO42RSB1
B22	TMS
B23	TDO
B24	IO41RSB0

QN132	
Pin Number	AGL030 Function
B25	GND
B26	NC
B27	IO37RSB0
B28	GND
B29	GDA0/IO33RSB0
B30	NC
B31	GND
B32	IO29RSB0
B33	IO26RSB0
B34	IO23RSB0
B35	IO20RSB0
B36	GND
B37	IO17RSB0
B38	IO15RSB0
B39	GND
B40	IO12RSB0
B41	IO09RSB0
B42	GND
B43	IO04RSB0
B44	IO01RSB0
C1	IO82RSB1
C2	IO79RSB1
C3	NC
C4	IO74RSB1
C5	GEA0/IO72RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO65RSB1
C10	IO62RSB1
C11	IO61RSB1
C12	IO58RSB1
C13	NC
C14	NC
C15	IO51RSB1
C16	VCCIB1

FG144		FG144		FG144	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GNDQ	D1	IO149NDB3	G1	GFA1/IO145PPB3
A2	VMV0	D2	IO149PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO153VDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO155UPB3	G4	GFA0/IO145NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO30RSB0	D7	GBC0/IO54RSB0	G7	GND
A8	VCC	D8	GBC1/IO55RSB0	G8	GDC1/IO77UPB1
A9	IO34RSB0	D9	GBB2/IO61PDB1	G9	IO72NDB1
A10	GBA0/IO58RSB0	D10	IO61NDB1	G10	GCC2/IO72PDB1
A11	GBA1/IO59RSB0	D11	IO62NPB1	G11	IO71NDB1
A12	GNDQ	D12	GCB1/IO68PPB1	G12	GCB2/IO71PDB1
B1	GAB2/IO154UDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO147NDB3	H2	GFB2/IO143PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO147PDB3	H3	GFC2/IO142PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO137PDB3
B5	IO14RSB0	E5	IO155VPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO75PDB1
B7	IO23RSB0	E7	VCCIB0	H7	IO75NDB1
B8	IO31RSB0	E8	GCC1/IO67PDB1	H8	GDB2/IO81RSB2
B9	GBB0/IO56RSB0	E9	VCCIB1	H9	GDC0/IO77VPB1
B10	GBB1/IO57RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO69NDB1	H11	IO73PSB1
B12	VMV1	E12	IO70NDB1	H12	VCC
C1	IO154VDB3	F1	GFB0/IO146NPB3	J1	GEB1/IO136PDB3
C2	GFA2/IO144PPB3	F2	VCOMPLF	J2	IO143NDB3
C3	GAC2/IO153UDB3	F3	GFB1/IO146PPB3	J3	VCCIB3
C4	VCC	F4	IO144NPB3	J4	GEC0/IO137NDB3
C5	IO12RSB0	F5	GND	J5	IO125RSB2
C6	IO17RSB0	F6	GND	J6	IO116RSB2
C7	IO25RSB0	F7	GND	J7	VCC
C8	IO32RSB0	F8	GCC0/IO67NDB1	J8	TCK
C9	IO53RSB0	F9	GCB0/IO68NPB1	J9	GDA2/IO80RSB2
C10	GBA2/IO60PDB1	F10	GND	J10	TDO
C11	IO60NDB1	F11	GCA1/IO69PDB1	J11	GDA1/IO79UDB1
C12	GBC2/IO62PPB1	F12	GCA2/IO70PDB1	J12	GDB1/IO78UDB1

FG484	
Pin Number	AGL400 Function
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO154VDB3
F5	IO155VDB3
F6	IO11RSB0
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO45RSB0
F15	GBC0/IO54RSB0
F16	IO48RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	NC
G2	NC
G3	NC
G4	IO151VDB3

FG484	
Pin Number	AGL1000 Function
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO38RSB0
H12	IO47RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

FG484	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3