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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	235
Number of Gates	600000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1agl600v2-fgg484i

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.†

† *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-26 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings**
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	I_{OL}	I_{OH}
				Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VDD-0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS[4]	2 mA	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range[4]	100 µA	2 mA	High	–0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI – 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
3. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable to V2 Devices operating at VCCI ≥ VCC.*
5. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.*

Table 2-35 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI (per standard) Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option[1] (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12	High	5	–	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
2.5 V LVCMOS	12 mA	12	High	5	–	1.55	2.29	0.26	1.19	1.10	2.32	1.94	2.94	3.52	8.10	7.73	ns
1.8 V LVCMOS	8 mA	8	High	5	–	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
1.5 V LVCMOS	4 mA	4	High	5	–	1.55	2.68	0.26	1.27	1.10	2.72	2.39	3.07	3.37	8.50	8.18	ns
1.2 V LVCMOS	2 mA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
1.2 V LVCMOS Wide Range[3]	100 µA	2	High	5	–	1.55	3.22	0.26	1.59	1.10	3.11	2.78	3.29	3.48	8.90	8.57	ns
3.3 V PCI	Per PCI spec	–	High	10	25[2]	1.55	2.53	0.26	0.84	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25[2]	1.55	2.53	0.25	0.85	1.10	2.57	1.98	2.93	3.64	8.35	7.76	ns

Notes:

1. *The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
5. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-62 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Applies to 1.2 V Core Voltage

Table 2-89 • **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-91 • **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-97 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

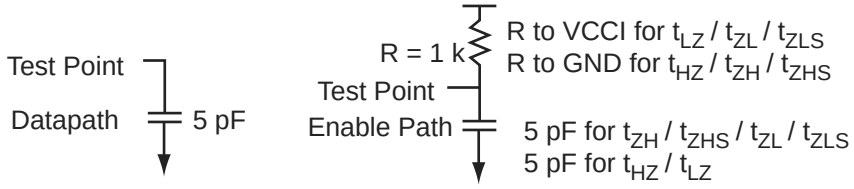


Figure 2-9 • AC Loading

Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-99 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-104 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	2.62	0.18	0.98	0.66	2.67	2.59	1.67	1.29	2.62	ns
4 mA	Std.	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	2.18	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-105 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.97	0.26	1.11	1.10	7.08	6.48	2.87	2.29	12.87	12.27	ns
4 mA	Std.	1.55	5.91	0.26	1.11	1.10	6.01	5.57	3.21	3.14	11.79	11.36	ns
6 mA	Std.	1.55	5.16	0.26	1.11	1.10	5.24	4.95	3.45	3.55	11.03	10.74	ns
8 mA	Std.	1.55	4.90	0.26	1.11	1.10	4.98	4.81	3.50	3.66	10.77	10.60	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-106 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.86	2.34	9.49	9.51	ns
4 mA	Std.	1.55	3.12	0.26	1.11	1.10	3.16	2.97	3.21	3.22	8.95	8.75	ns
6 mA	Std.	1.55	2.79	0.26	1.11	1.10	2.83	2.59	3.45	3.65	8.62	8.38	ns
8 mA	Std.	1.55	2.73	0.26	1.11	1.10	2.77	2.52	3.50	3.75	8.56	8.30	ns
12 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
16 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-119 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-120 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-121 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-122 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Input Register

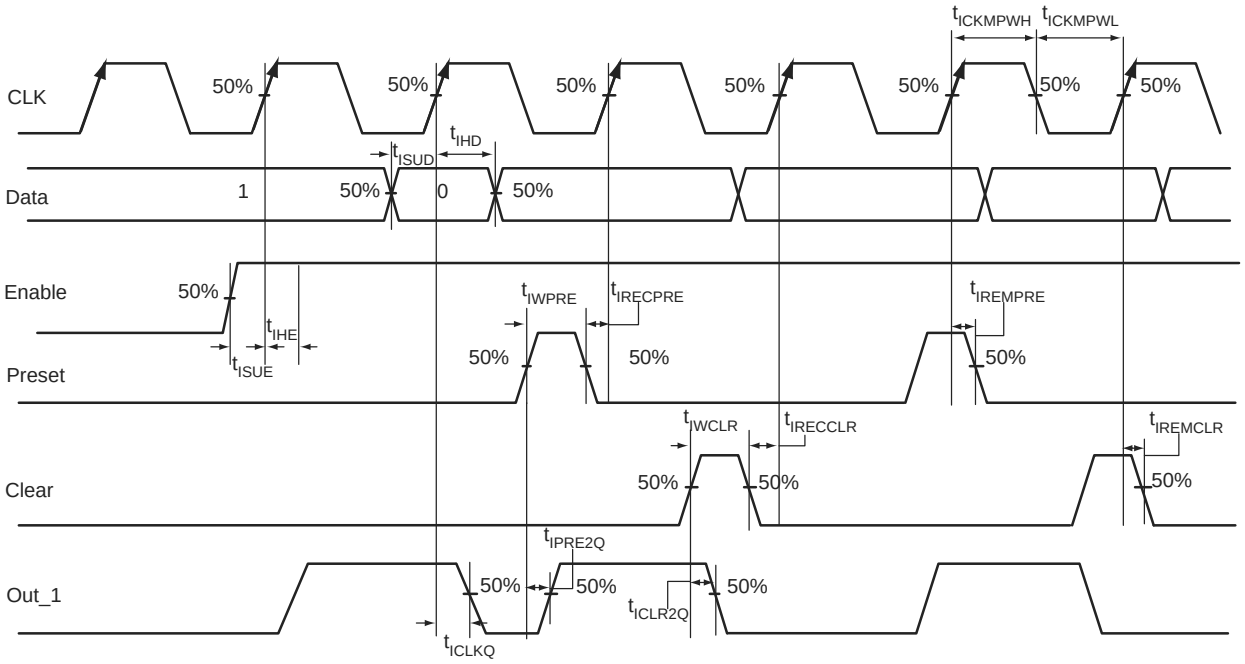


Figure 2-18 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-157 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

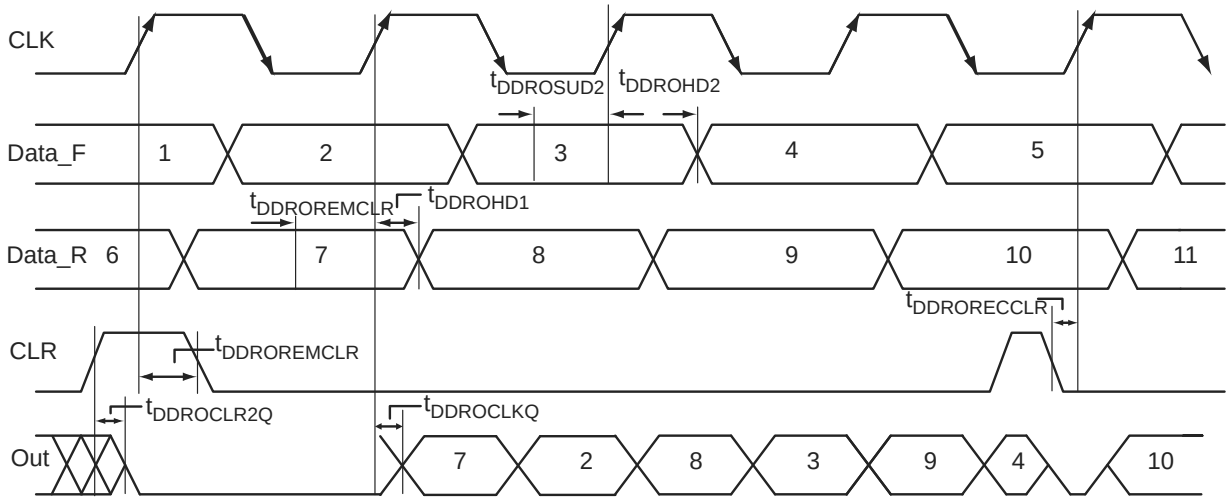


Figure 2-24 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-167 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-199 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-200 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

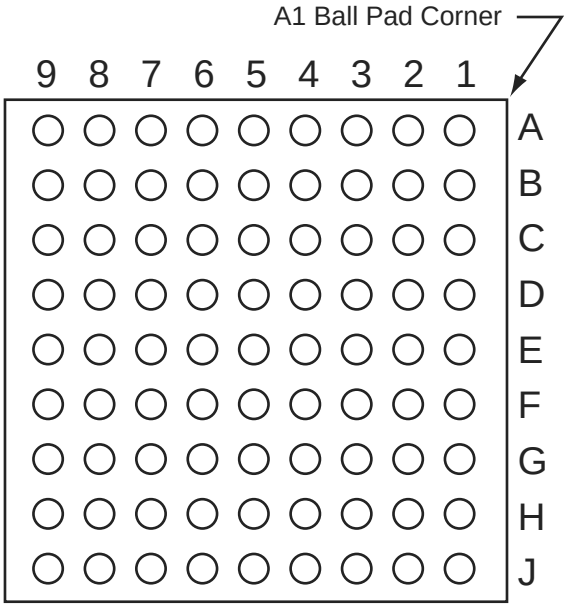
Table 3-1 shows the Flash*Freeze pin location on the available packages for IGLOO a devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to the "Flash*Freeze Technology and Low Power Modes" chapter of the *IGLOO FPGA Fabric User Guide* for more information on I/O states during Flash*Freeze mode.

***Table 3-1* • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)**

IGLOO Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
CS281	W2
QN48	14
QN68	18
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

4 – Package Pin Assignments

UC81



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS281	
Pin Number	**AGL1000 Function**
R15	IO122RSB2
R16	GDA1/IO113PPB1
R18	GDB0/IO112NPB1
R19	GDC0/IO111NPB1
T1	IO197PPB3
T2	GEC0/IO190NPB3
T4	GEB0/IO189NPB3
T5	IO181RSB2
T6	IO172RSB2
T7	IO171RSB2
T8	IO156RSB2
T9	IO159RSB2
T10	GND
T11	IO139RSB2
T12	IO138RSB2
T13	IO129RSB2
T14	IO123RSB2
T15	GDC2/IO116RSB2
T16	TMS
T18	VJTAG
T19	GDB1/IO112PPB1
U1	IO193PDB3
U2	GEA1/IO188PPB3
U6	IO167RSB2
U14	IO128RSB2
U18	TRST
U19	GDA0/IO113NPB1
V1	IO193NDB3
V2	VCCIB3
V3	GEC2/IO185RSB2
V4	IO182RSB2
V5	IO175RSB2
V6	GND
V7	IO161RSB2
V8	IO143RSB2
V9	IO146RSB2

CS281	
Pin Number	**AGL1000 Function**
V10	IO145RSB2
V11	IO144RSB2
V12	IO134RSB2
V13	IO133RSB2
V14	GND
V15	IO119RSB2
V16	GDA2/IO114RSB2
V17	TDI
V18	VCCIB2
V19	TDO
W1	GND
W2	FF/GEB2/IO186RSB2
W3	IO183RSB2
W4	IO176RSB2
W5	IO170RSB2
W6	IO162RSB2
W7	IO157RSB2
W8	IO152RSB2
W9	IO149RSB2
W10	VCCIB2
W11	IO140RSB2
W12	IO135RSB2
W13	IO130RSB2
W14	IO125RSB2
W15	IO120RSB2
W16	IO118RSB2
W17	GDB2/IO115RSB2
W18	TCK
W19	GND

FG144	
Pin Number	**AGL400 Function**
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484	
Pin Number	**AGL400 Function**
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

FG484	
Pin Number	**AGL600 Function**
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3

FG484	
Pin Number	**AGL600 Function**
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	**AGL1000 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	VCCIB0
A21	GND
A22	GND
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC