Microsemi Corporation - M1AGL600V5-FGG484 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	13824
Total RAM Bits	110592
Number of I/O	235
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1agl600v5-fgg484

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IGLOO Device Family Overview

IGLOO DC and Switching Characteristics

Pin Descriptions

Package Pin Assignments

Datasheet Information

2 – IGLOO DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits[1]	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI and VMV [2]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [3]	Storage Temperature	–65 to +150	°C
T_J [3]	Junction Temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information.*
3. *For flash programming and retention, maximum limits refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

1.2 V DC Core Voltage

Table 2-165 **• Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Output DDR Module

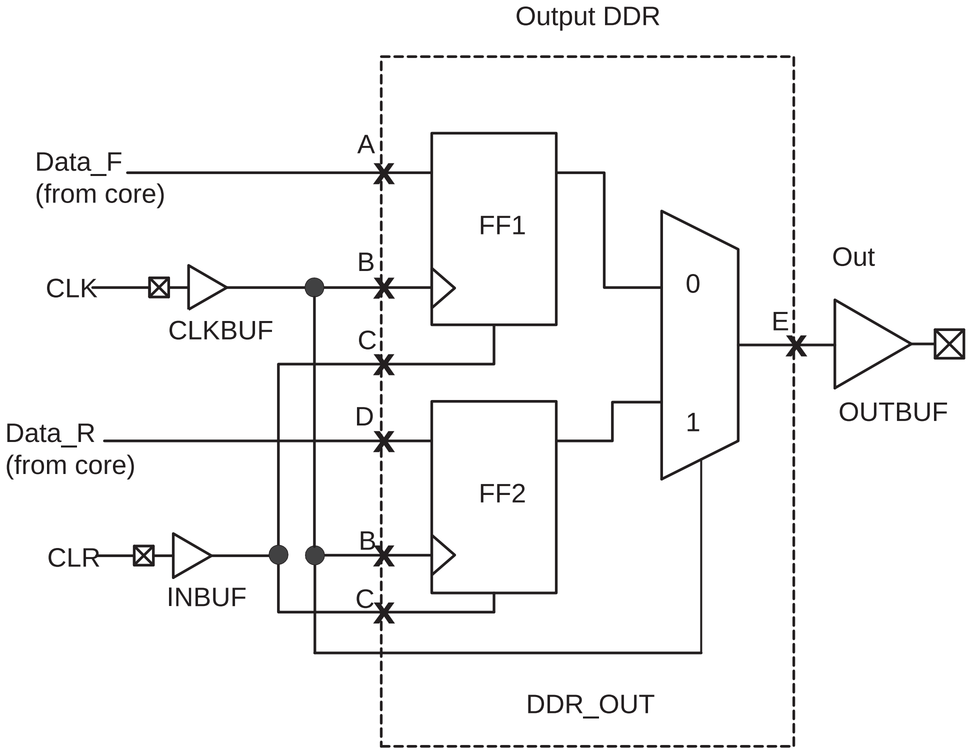


Figure 2-23 • **Output DDR Timing Model**

Table 2-166 • **Parameter Definitions**

Parameter Name	**Parameter Definition**	**Measuring Nodes (from, to)**
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

1.2 V DC Core Voltage

Table 2-168 • Output DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

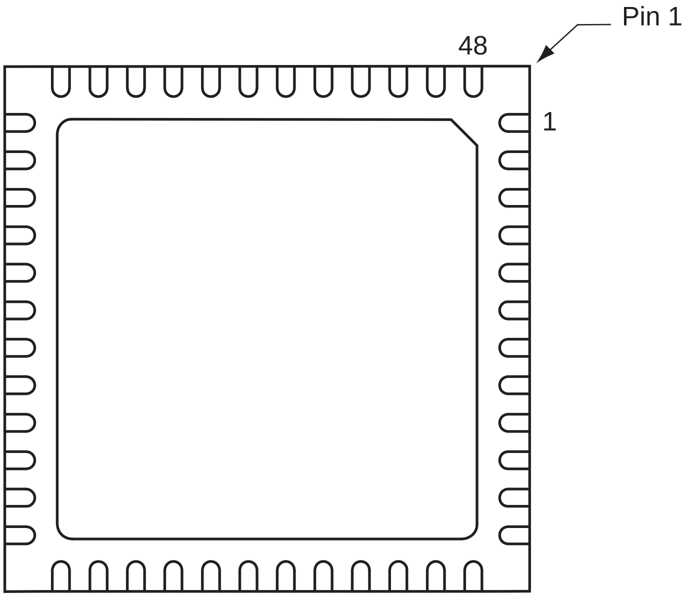
***Table 2-172* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

CS281	
Pin Number	AGL600 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO68NPB1
H16	GCB0/IO70NPB1
H18	GCA1/IO71PPB1
H19	GCA2/IO72PPB1
J1	VCOMPLF
J2	GFA0/IO162NDB3
J4	VCCPLF
J5	GFC0/IO164NPB3
J7	GFA2/IO161PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO69PPB1
J15	GCA0/IO71NPB1
J16	GCB2/IO73PPB1
J18	IO72NPB1
J19	IO75PSB1
K1	VCCIB3
K2	GFA1/IO162PDB3
K4	GND
K5	IO159NPB3
K7	IO161NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO74PPB1
K15	IO73NPB1
K16	GND
K18	IO74NPB1
K19	VCCIB1
L1	GFB2/IO160PDB3
L2	IO160NDB3
L4	GFC2/IO159PPB3
L5	IO153PPB3
L7	IO153NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO76PPB1
L15	IO76NPB1
L16	IO77PPB1
L18	IO78NPB1
L19	IO77NPB1
M1	IO158PDB3
M2	IO158NDB3
M4	IO154NPB3
M5	IO152PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO79NPB1
M16	IO81NPB1
M18	IO79PPB1
M19	IO78PPB1
N1	IO154PPB3
N2	IO152NPB3
N4	IO150PPB3
N5	IO148NPB3
N7	GEA2/IO143RSB2
N8	VCCIB2
N9	IO117RSB2
N10	IO115RSB2
N11	IO114RSB2
N12	VCCIB2
N13	VPUMP
N15	IO82PPB1
N16	IO85PPB1
N18	IO82NPB1
N19	IO81PPB1
P1	IO151PDB3
P2	GND
P3	IO151NDB3
P4	IO149PPB3
P5	GEA0/IO144NPB3
P15	IO83NDB1
P16	IO83PDB1
P17	GDC1/IO86PPB1
P18	GND
P19	IO85NPB1
R1	IO150NPB3
R2	IO149NPB3
R4	GEC1/IO146PPB3
R5	GEB1/IO145PPB3
R6	IO138RSB2
R7	IO127RSB2
R8	IO123RSB2
R9	IO118RSB2
R10	IO111RSB2
R11	IO106RSB2
R12	IO103RSB2
R13	IO97RSB2
R14	IO95RSB2

QN48



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	**AGL600 Function**
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	VCOMPLF
L8	GFC0/IO164NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3

FG484	
Pin Number	**AGL600 Function**
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

FG484	
Pin Number	**AGL1000 Function**
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO38RSB0
H12	IO47RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

5 – Datasheet Information

List of Changes

The following tables list critical changes that were made in each revision of the IGLOO datasheet.

Revision	Changes	Page
Revision 27 (May 2016)	Added the deleted package FG144 from AGL125 device in "IGLOO Devices" (SAR 79355).	1-I
Revision 26 (March 2016)	Updated "IGLOO Ordering Information" and "Temperature Grade Offerings" notes by: • Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352). • Replacing Industrial (–40°C to +85°C Ambient Temperature) with Industrial (–40°C to +100°C Junction Temperature) (SAR 48352).	1-III and 1-IV
	Ambient temperature row removed in Table 2-2 (SAR 48352).	2-2
	Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087).	2-2
	Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087)	2-2
	Added 2 mA drive strengths in tables same as 4 mA (SAR 57179).	NA
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777).	NA
Revision 25 (June2015)	Removed package FG144 from AGL060 device in the following tables: "IGLOO Devices", "I/Os Per Package1" and "Temperature Grade Offerings" (SAR 68517)	I, II, and IV
	Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517)	-
Revision 24 (March 2014)	Note added for the discontinuance of QN132 package to the following tables: "IGLOO Devices", "I/Os Per Package1", "IGLOO FPGAs Package Sizes Dimensions", and"Temperature Grade Offerings" and "QN132" section (SAR 55117, PDN 1306).	I, II, IV, and 4-28
	Removed packages CS81 and QN132 from AGL250 device in the following tables: "IGLOO Devices", "I/Os Per Package1", and "Temperature Grade Offerings" (SAR 49472).	I, II, and IV