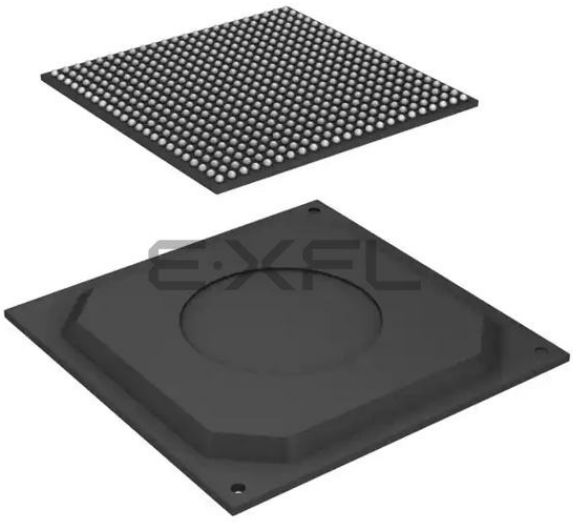


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx534avv8c2

provides all the interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, camera sensors, and dual displays.

Features of the i.MX53xA processor include the following:

- Multilevel memory system—The multilevel memory system of the i.MX53xA is based on the L1 instruction and data caches, L2 cache, internal and external memory. The i.MX53xA supports many types of external memory devices, including DDR2, low voltage DDR2, LPDDR2, DDR3, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND including eMMC up to rev 4.4.
- Smart speed technology—The i.MX53xA device has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product requiring levels of power far lower than industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX53xA processor ARM core is boosted by a multilevel cache system, Neon (including advanced SIMD, 32-bit single-precision floating point support) and vector floating point coprocessors. The system is further enhanced by a multi-standard hardware video codec, autonomous image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration— The i.MX53xA processors provide two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator (33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance) and an OpenVG™ 1.1 2D graphics accelerator (200 Mpix/s).
- Interface flexibility—The i.MX53xA processor supports connection to a variety of interfaces, including LCD controller for two displays and CMOS sensor interface, high-speed USB on-the-go with PHY, plus three high-speed USB hosts, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, and I^2S serial audio, among others).
- Automotive environment support—Includes interfaces such as two CAN ports, an MLB port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The i.MX53xA processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the i.MX53xA security features contact a Freescale representative.

The i.MX53xA application processor is a follow-on to the i.MX51xA, with improved performance, power efficiency, and multimedia capabilities.

Table 11. GPIO I/O DC Electrical Characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input current (100 kΩ Pull-down)	Iin	Vin = 0 V Vin = OVDD	—	—	10 40	µA
Keeper Circuit Resistance			—	130[4]	—	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.2 LPDDR2 I/O DC Parameters

The LPDDR2 I/O pads support DDR2/LVDDR2, LPDDR2, and DDR3 operational modes.

4.3.2.1 DDR2 Mode I/O DC Parameters

The DDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The parameters in Table 12 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 12. DDR2 I/O DC Electrical Parameters[1]

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[2]	Voh	Ioh = -0.1 mA	0.9 x OVDD	—	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	—	0.1 x OVDD	V
Input Reference Voltage	Vref		0.49 x OVDD	0.5 x OVDD	0.51 x OVDD	
DC input High Voltage (data pins)	Vihd (dc)	—	Vref+0.125V	—	OVDD+0.3	V
DC input Low Voltage (data pins)	Vild (dc)	—	-0.3	—	Vref - 0.125V	V
DC Input voltage range of each differential input[3]	Vin (dc)	—	-0.3	—	OVDD + 0.3	V
DC Differential input voltage required for switching [4]	Vid (dc)	—	0.25	—	OVDD + 0.6	V
Termination Voltage	Vtt	Vtt	Vref - 0.04	Vref	Vref + 0.04	V
Input current (no pull-up/down)	Iin	Vin = 0 V Vin = OVDD	— —	— —	1 1	µA
Keeper Circuit Resistance	—	—	—	130[5]	—	kΩ

1 Note that the JEDEC SSTL_18 specification (JESD8-15a) for a SSTL interface for class II operation supersedes any specification in this document.

2 OVDD is the I/O power supply (1.7 V–1.9 V for DDR2)

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

3 Hysteresis of 350 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

4.3.4 Ultra-High Voltage I/O (UHVIO) DC Parameters

The parameters in Table 16 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 16. UHVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage[1]	Voh	Iout = -0.8 mA	OVDD-0.15	—	—	V
Low-level output voltage[1]	Vol	Iout = 0.8 mA	—	—	0.15	V
High-Level DC input voltage[1, 2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1, 2]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	low voltage mode high voltage mode	0.38 0.95	—	0.43 1.33	V
Schmitt trigger VT+[2, 3]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT-[2, 3]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0 V	—	—	1	µA
Input current (22 kΩ Pull-up)	Iin	Vin = 0 Vin = OVDD	—	—	202 1	µA
Input current (75 kΩ Pull-up)	Iin	Vin = 0 Vin = OVDD	—	—	61 1	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0 Vin = OVDD	—	—	47 1	µA
Input current (360 kΩ Pull-down)	Iin	Vin = 0 Vin = OVDD	—	—	1 5.7	µA
Keeper Circuit Resistance	—	—	—	130[4]	—	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s. VIL and VIH do not apply when hysteresis is enabled.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 Use an off-chip pull resistor of less than 60 kΩ to override this keeper.

Table 19 shows DDR output driver average impedance of the i.MX53xA processor.

Table 19. DDR Output Driver Average Impedance[1]

Parameter	Symbol	Test Conditions	Drive strength (DSE)								Unit
			000	001	010	011	100	101	110	111	
Output Driver Impedance	Rdrv[2]	LPDDR1/DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 00 Calibration resistance = 300 Ω[3]	Hi-Z	300	150	100	75	60	50	43	Ω
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 01 Calibration resistance = 180 Ω[3]	Hi-Z	180	90	60	45	36	30	26	
		DDR2 mode NVCC_DRAM = 1.8 V DDR_SEL = 10 Calibration resistance = 200 Ω[3]	Hi-Z	200	100	66	50	40	33	28	
		DDR2 mode NVCC_DRAM= 1.8 V DDR_SEL = 11 Calibration resistance = 140 Ω[3]	Hi-Z	140	70	46	35	28	23	20	
		LPDDR2 mode NVCC_DRAM= 1.2 V DDR_SEL = 01[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 10 Calibration resistance = 240 Ω[3]	Hi-Z	240	120	80	60	48	40	34	
		LPDDR2 mode NVCC_DRAM = 1.2 V DDR_SEL = 11[4] Calibration resistance = 160 Ω[3]	Hi-Z	160	80	53	40	32	27	23	
		DDR3 mode NVCC_DRAM = 1.5 V DDR_SEL = 00 Calibration resistance = 200 Ω[3]	Hi-Z	240	120	80	60	48	48	34	

1 Output driver impedance is controlled across PVTs (process, voltages, and temperatures) using calibration procedure and pu_*cal, pd_*cal input pins.

2 Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

3 Calibration is done against external reference resistor. Value of the resistor should be varied depending on DDR mode and DDR_SEL setting.

4 If DDR_SEL = ‘01’ or DDR_SEL = ‘11’ are selected with NVCC_DRAM = 1.2 V for LPDDR2 operation, the external reference resistor value must be 160 Ω for a correct ZQ calibration. In any case, reference resistors attached to the DDR memory devices should be kept to 240 Ω per the JEDEC standard.

4.4.3 UHVIO Output Buffer Impedance

Table 20 shows the UHVIO output buffer impedance.

Table 20. UHVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.0 V	OVDD 1.875 V	OVDD 3.3 V	OVDD 1.65 V	OVDD 3.6 V	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	98 49 32	114 57 38	124 62 41	135 67 45	198 99 66	206 103 69	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	97 49 32	118 59 40	126 63 42	154 77 51	179 89 60	217 109 72	Ω

4.4.4 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.5 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate 3 I/O (DDR3) for DDR2/LVDDR2, LPDDR2 and DDR3 modes
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- LVDS I/O

The load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

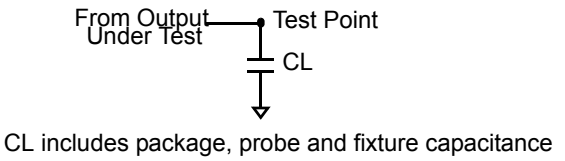


Figure 5. Load Circuit for Output

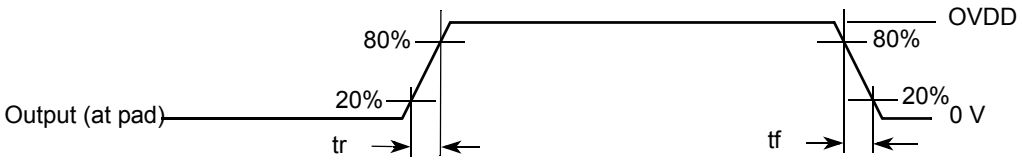


Figure 6. Output Transition Time Waveform

4.5.1 GPIO I/O AC Electrical Characteristics

AC electrical characteristics for GPIO I/O in slow and fast modes are presented in the Table 21 and Table 22, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bit in the IOMUXC control registers.

Table 21. GPIO I/O AC Parameters Slow Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.91/1.52 3.07/2.65	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.22/1.81 3.81/3.42	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.88/2.42 5.43/5.02	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.94/4.50 10.55/9.70	ns
Output Pad Slew Rate (Max Drive)[1]	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)[1]	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	
Output Pad Slew Rate (Medium Drive)[1]	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	
Output Pad Slew Rate (Low Drive)[1]	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	
Output Pad di/dt (Low drive)	tdit	—	—	—	7	
Input Transition Times[2]	trm	—	—	—	25	ns

1 tps is measured between VIL to VIH for rising edge and between VIH to VIL for falling edge.

2 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 22. GPIO I/O AC Parameters Fast Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.45/1.24 2.76/2.54	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.81/1.59 3.57/3.33	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.54/2.29 5.25/5.01	ns

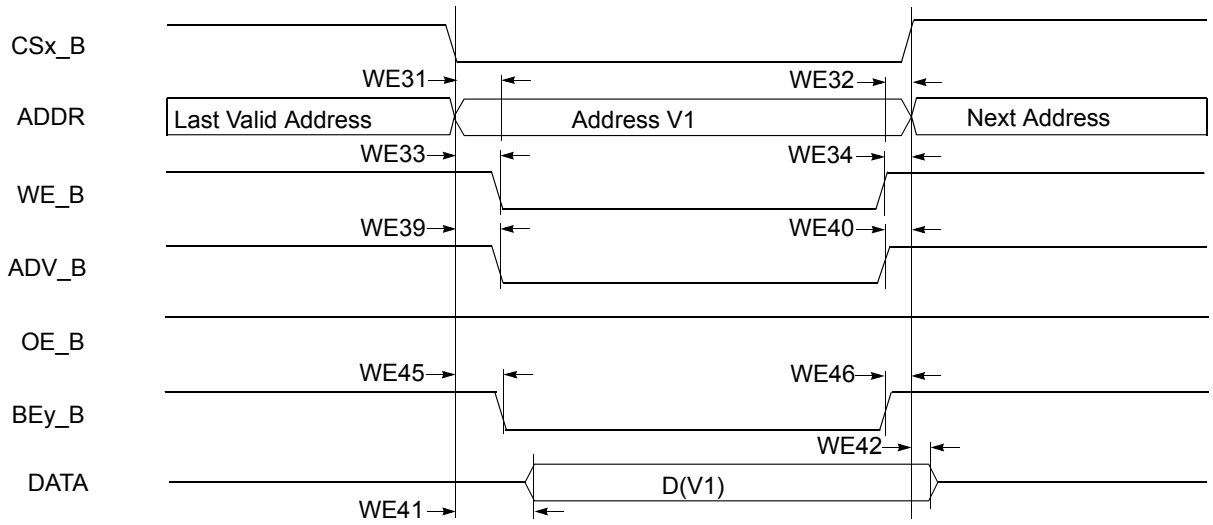


Figure 24. Asynchronous Memory Write Access

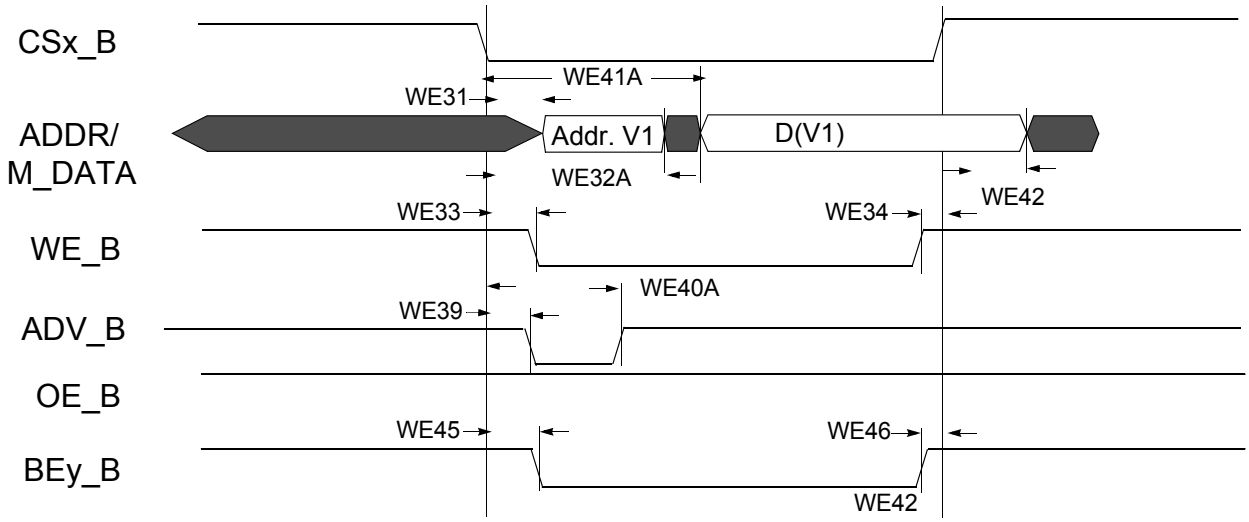


Figure 25. Asynchronous A/D Muxed Write Access

4.7.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 43 depicts the timing of I²C module, and Table 57 lists the I²C module timing characteristics.

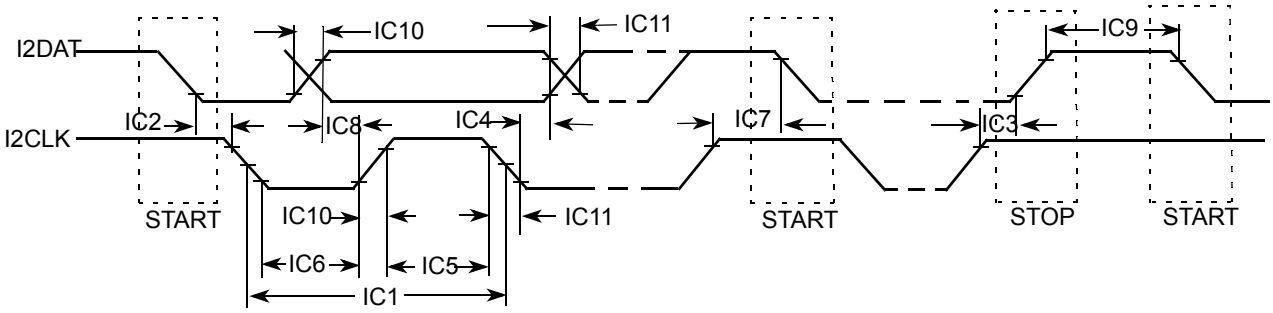


Figure 43. I²C Bus Timing

Table 57. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

Table 61 shows timing characteristics of signals presented in Figure 48 and Figure 49.

Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	Width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

Figure 64 depicts the timing of the PWM, and Table 71 lists the PWM timing parameters.

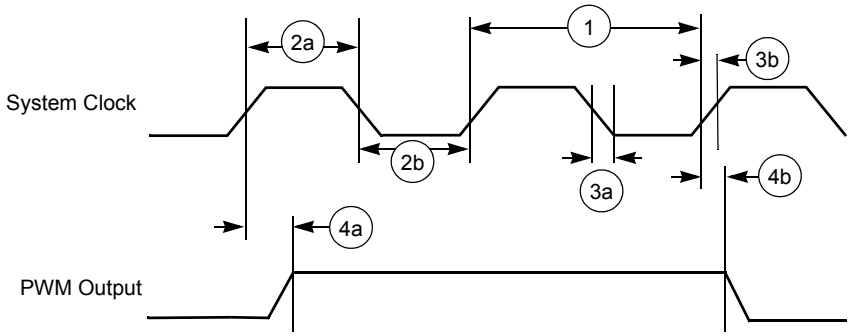


Figure 64. PWM Timing

Table 71. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.13 PATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-6 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 100MB/s. Parallel ATA module interface consist of a total of 29 pins. Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-6 specification and these requirements are configurable by the ATA module registers.

Table 72 and Figure 65 define the AC characteristics of all the PATA interface signals in all data transfer modes.

4.7.13.1 PIO Mode Read Timing

Figure 66 shows timing for PIO read. Table 74 lists the timing parameters for PIO read.

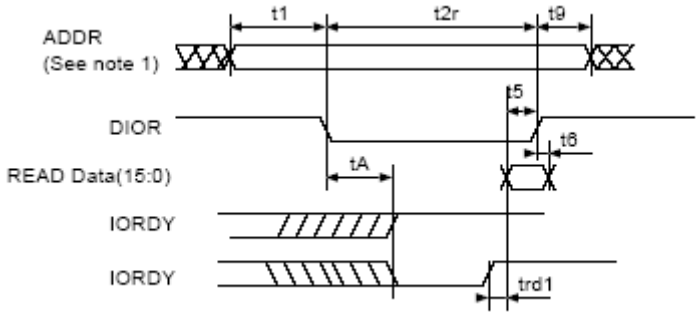


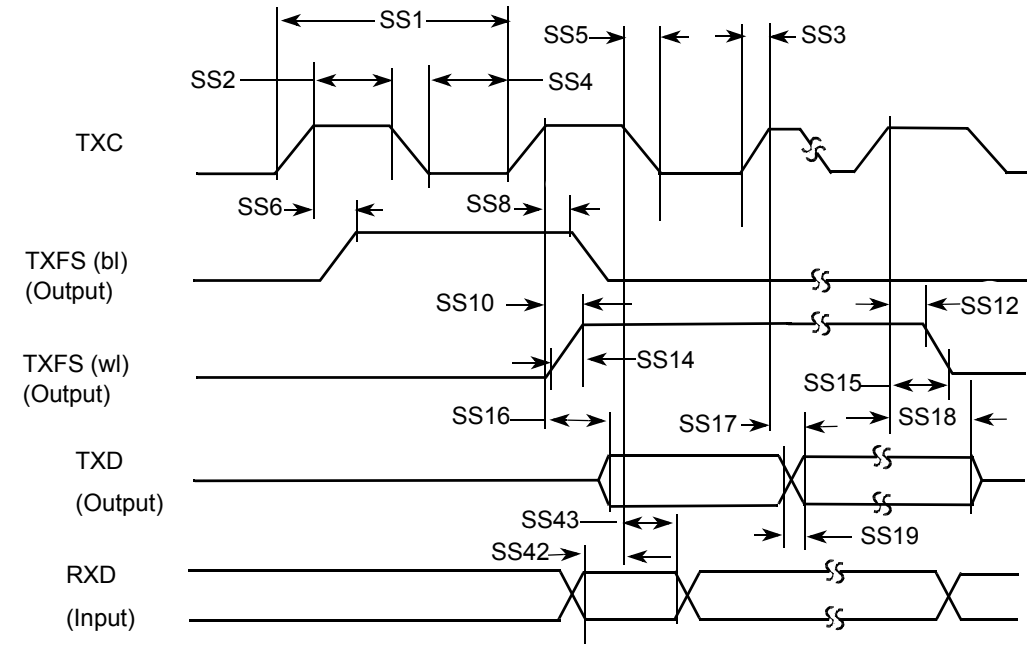
Figure 66. PIO Read Timing Diagram

Table 74. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 66	Value	Controlling Variable
t1	t1	t1(min) = time_1 x T - (tskew1 + tskew2 + tskew5)	time_1
t2 (read)	t2r	t2(min) = time_2r x T - (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9(min) = time_9 x T - (tskew1 + tskew2 + tskew6)	time_9
t5	t5	t5(min) = tco + tsu + tbuf + tbuf+ tcable1 + tcable2	time_2 (affects tsu and tco)
t6	t6	0	—
tA	tA	tA(min) = (1.5 + time_ax) x T - (tco + tsui + tcable2 + tcable2 + 2 x tbuf)	time_ax
trd	trd1	trd1(max) = (-trd)+ (tskew3 + tskew4) trd1(min) = (time_pio_rdx - 0.5) x T - (tsu + thi) (time_pio_rdx - 0.5) x T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0(min) = (time_1 + time_2r+ time_9) x T	time_1, time_2r, time_9

4.7.17.1 SSI Transmitter Timing with Internal Clock

Figure 83 depicts the SSI transmitter internal clock timing and Table 85 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only
: SRXD input in synchronous mode only

Figure 83. SSI Transmitter Internal Clock Timing Diagram

Table 85. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns

Table 86. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

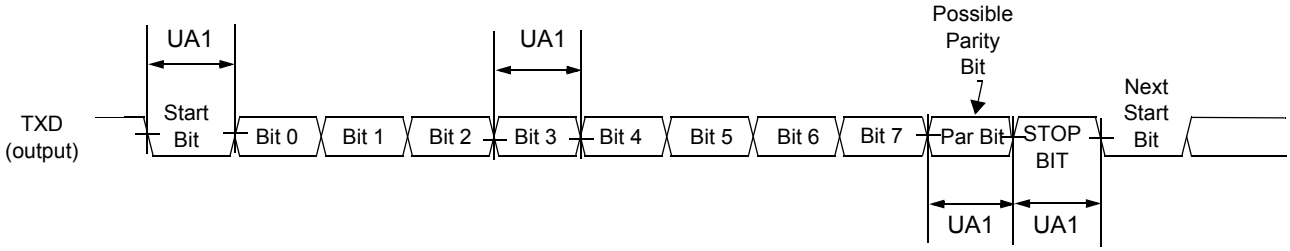


Figure 87. UART RS-232 Serial Mode Transmit Timing Diagram

Table 90. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.18.2.2 UART Receiver

Figure 88 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 91 lists serial mode receive timing characteristics.

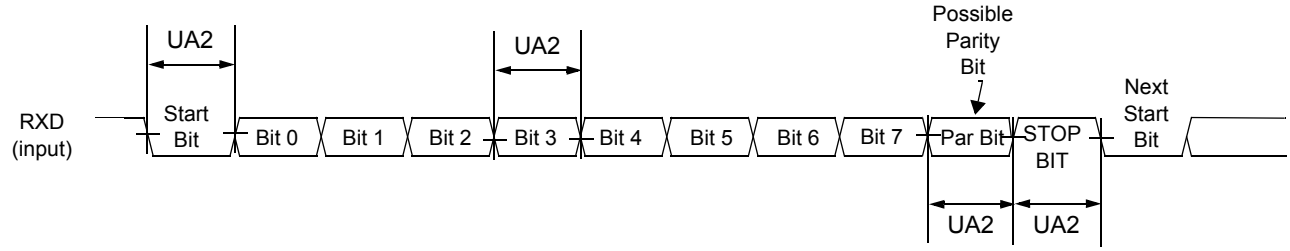


Figure 88. UART RS-232 Serial Mode Receive Timing Diagram

Table 91. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.18.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.18.3.3 UART IrDA Mode Transmitter

Figure 89 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 92 lists the transmit timing characteristics.

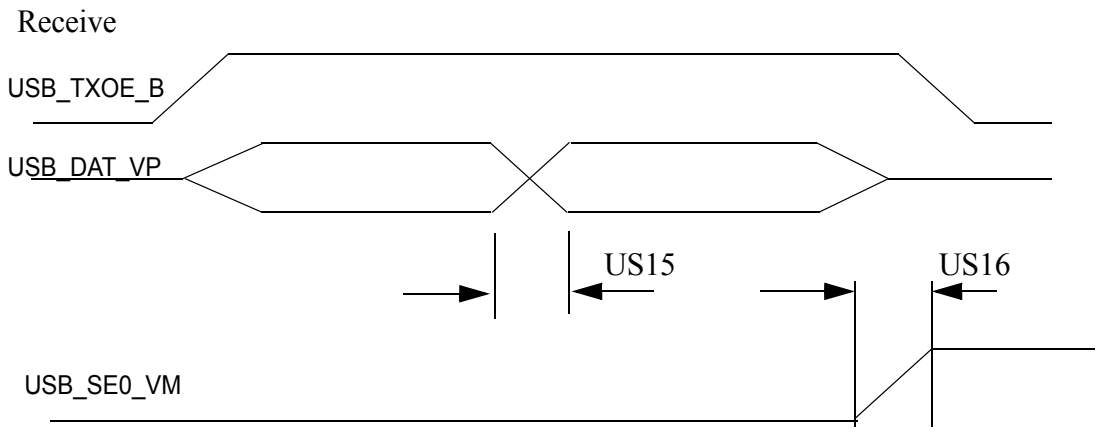


Figure 94. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 97. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition / Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF

Table 111. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFUSE Name	Details
EIM_A22	Input	BOOT_CFG1[7]/Test Mode Selection	Boot Options, Pin value overrides fuse settings for **BT_FUSE_SEL = '0'**. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_A21	Input	BOOT_CFG1[6]/Test Mode Selection	
EIM_A20	Input	BOOT_CFG1[5]/Test Mode Selection	
EIM_A19	Input	BOOT_CFG1[4]	
EIM_A18	Input	BOOT_CFG1[3]	
EIM_A17	Input	BOOT_CFG1[2]	
EIM_A16	Input	BOOT_CFG1[1]	
EIM_LBA	Input	BOOT_CFG1[0]	
EIM_EB0	Input	BOOT_CFG2[7]	
EIM_EB1	Input	BOOT_CFG2[6]	
EIM_DA0	Input	BOOT_CFG2[5]	
EIM_DA1	Input	BOOT_CFG2[4]	
EIM_DA2	Input	BOOT_CFG2[3]	
EIM_DA3	Input	BOOT_CFG2[2]	
EIM_DA4	Input	BOOT_CFG3[7]	
EIM_DA5	Input	BOOT_CFG3[6]	
EIM_DA6	Input	BOOT_CFG3[5]	
EIM_DA7	Input	BOOT_CFG3[4]	
EIM_DA8	Input	BOOT_CFG3[3]	
EIM_DA9	Input	BOOT_CFG3[2]	
EIM_DA10	Input	BOOT_CFG3[1]	

5.2 Boot Devices Interfaces Allocation

Table 112 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 112. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	CSPI	EIM_A25, EIM_D21, EIM_D22, EIM_D28	Only SS1 is supported
SPI	ECSPI-1	EIM_D[19:16]	Only SS1 is supported
SPI	ECSPI-2	CSI_DAT[10:8], EIM_LBA	Only SS1 is supported

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
CSI0_DAT10	R5	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[28]	Input	100 KΩ PU
CSI0_DAT11	T2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[29]	Input	100 KΩ PU
CSI0_DAT12	T3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[30]	Input	360 KΩ PD
CSI0_DAT13	T6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[31]	Input	360 KΩ PD
CSI0_DAT14	U1	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[0]	Input	360 KΩ PD
CSI0_DAT15	U2	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[1]	Input	360 KΩ PD
CSI0_DAT16	T4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[2]	Input	360 KΩ PD
CSI0_DAT17	T5	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[3]	Input	360 KΩ PD
CSI0_DAT18	U3	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[4]	Input	360 KΩ PD
CSI0_DAT19	U4	NVCC_CSI	UHVIO	ALT1	GPIO-6	gpio6_GPIO[5]	Input	360 KΩ PD
CSI0_DAT4	R1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[22]	Input	100 KΩ PU
CSI0_DAT5	R2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[23]	Input	360 KΩ PD
CSI0_DAT6	R6	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[24]	Input	100 KΩ PU
CSI0_DAT7	R3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[25]	Input	100 KΩ PU
CSI0_DAT8	T1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[26]	Input	100 KΩ PU
CSI0_DAT9	R4	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[27]	Input	360 KΩ PD
CSI0_DATA_EN	P3	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[20]	Input	100 KΩ PU
CSI0_MCLK	P2	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[19]	Input	100 KΩ PU
CSI0_PIXCLK	P1	NVCC_CSI	UHVIO	ALT1	GPIO-5	gpio5_GPIO[18]	Input	100 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
PATA_DA_1	L3	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[7]	Input	100 KΩ PU
PATA_DA_2	L4	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[8]	Input	100 KΩ PU
PATA_DATA0	L1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[0]	Input	100 KΩ PU
PATA_DATA1	M1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[1]	Input	100 KΩ PU
PATA_DATA10	N4	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[10]	Input	100 KΩ PU
PATA_DATA11	M6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[11]	Input	100 KΩ PU
PATA_DATA12	N5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[12]	Input	100 KΩ PU
PATA_DATA13	N6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[13]	Input	100 KΩ PU
PATA_DATA14	P6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[14]	Input	100 KΩ PU
PATA_DATA15	P5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[15]	Input	100 KΩ PU
PATA_DATA2	L6	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[2]	Input	100 KΩ PU
PATA_DATA3	M2	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[3]	Input	100 KΩ PU
PATA_DATA4	M3	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[4]	Input	100 KΩ PU
PATA_DATA5	M4	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[5]	Input	100 KΩ PU
PATA_DATA6	N1	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[6]	Input	100 KΩ PU
PATA_DATA7	M5	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[7]	Input	100 KΩ PU
PATA_DATA8	N2	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[8]	Input	100 KΩ PU
PATA_DATA9	N3	NVCC_PATA	UHVIO	ALT1	GPIO-2	gpio2_GPIO[9]	Input	100 KΩ PU
PATA_DIOR	K3	NVCC_PATA	UHVIO	ALT1	GPIO-7	gpio7_GPIO[3]	Input	100 KΩ PU

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
USB_H1_GPANAIO	A16	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB	USB_H1_GPANAIO	—	—
USB_H1_RREFEXT	B16	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG25	—	USB	USB_H1_RREFEXT	—	—
USB_H1_VBUS	D15	USB_H1_VDDA25, USB_H1_VDDA33	ANALOG50	—	USB	USB_H1_VBUS	—	—
USB_OTG_DN	A19	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_DN	—	—
USB_OTG_DP	B19	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_DP	—	—
USB_OTG_GPANAIO	F15	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_GPANAIO	—	—
USB_OTG_ID	C16	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_ID	—	—
USB_OTG_RREFEXT	D16	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG25	—	USB	USB_OTG_RREFEXT	—	—
USB_OTG_VBUS	E15	USB_OTG_VDDA25, USB_OTG_VDDA33	ANALOG50	—	USB	USB_OTG_VBUS	—	—
XTAL	AC11	NVCC_XTAL	ANALOG	—	XTALOSC	XTAL	—	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 During power-on reset, this port acts as input for fuse override. See Section 5.1, “Boot Mode Configuration Pins” for details. For appropriate resistor values, see Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG).

3 During power-on reset, this port acts as output for diagnostic signal INT_BOOT

4 During power-on reset, this port acts as output for diagnostic signal ANY_PU_RST

NOTE

KEY_COL0 and GPIO_19 act as output for diagnostic signals during power-on reset.

Table 115. 19 x 19 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P
EIM_D23	EIM_D20	EIM_D18	CSI0_DAT14	CSI0_DAT8	CSI0_DAT4	CSI0_PIXCLK
EIM_D24	EIM_D22	EIM_D19	CSI0_DAT15	CSI0_DAT11	CSI0_DAT5	CSI0_MCLK
EIM_EB2	EIM_D25	EIM_D21	CSI0_DAT18	CSI0_DAT12	CSI0_DAT7	CSI0_DATA_EN
EIM_EB3	EIM_D30	EIM_D27	CSI0_DAT19	CSI0_DAT16	CSI0_DAT9	CSI0_VSYNC
EIM_A24	EIM_D31	EIM_D26	EIM_D17	CSI0_DAT17	CSI0_DAT10	PATA_DATA15
EIM_A20	EIM_A25	EIM_A23	EIM_D16	CSI0_DAT13	CSI0_DAT6	PATA_DATA14
EIM_CS1	EIM_A19	EIM_A17	NVCC_EIM_SEC	VCC	NVCC_CSI	GND
EIM_DA0	EIM_CS0	EIM_OE	VCC	GND	VCC	GND
EIM_DA6	EIM_DA3	EIM_DA5	NVCC_EIM_MAIN	VCC	GND	VCC
EIM_DA14	EIM_DA9	EIM_DA12	NVCC_EIM_MAIN	GND	VCC	GND
NANDF_ALE	EIM_BCLK	NVCC_SRTC_POW	NANDF_RB0	VCC	GND	VCC
LVDS1_TX3_P	NANDF_CS0	NVCC_XTAL	VDDA	NVCC_NANDF	VCC	GND
LVDS1_CLK_P	NANDF_CS3	NANDF_CS1	NVCC_LVDS	VCC	GND	VCC
GND	PMIC_ON_REQ	NANDF_CS2	NVCC_LVDS_BG	GND	VCC	GND
GND	PMIC_STBY_REQ	GND	GND	VCC	GND	VCC
LVDS0_TX2_N	GPIO_10	TVDAC_AHVDDRGB	TVDAC_DHVDD	GND	VCC	GND
LVDS0_TX0_N	GPIO_12	GPIO_11	TVDAC_AHVDDRGB	VCC	GND	NVCC_EMI_DRAM
TVDAC_VREF	GPIO_14	GND	VCC	NVCC_EMI_DRAM	DRAM_SDODT1	DRAM_RESET
GND	GND	GND	GND	DRAM_SDCKE1	DRAM_SDBA0	DRAM_CS1
DRAM_D24	DRAM_DQM3	GND	DRAM_D16	DRAM_DQM2	GND	DRAM_SDBA1
DRAM_D26	DRAM_D25	GND	DRAM_D18	DRAM_D17	DRAM_D19	GND
DRAM_SDQS3	DRAM_D27	GND	DRAM_D22	DRAM_SDQS2	DRAM_D21	DRAM_SDCLK_1
DRAM_SDQS3_B	DRAM_D31	DRAM_D29	DRAM_D20	DRAM_SDQS2_B	DRAM_D23	DRAM_SDCLK_1_B
Y	W	V	U	T	R	P