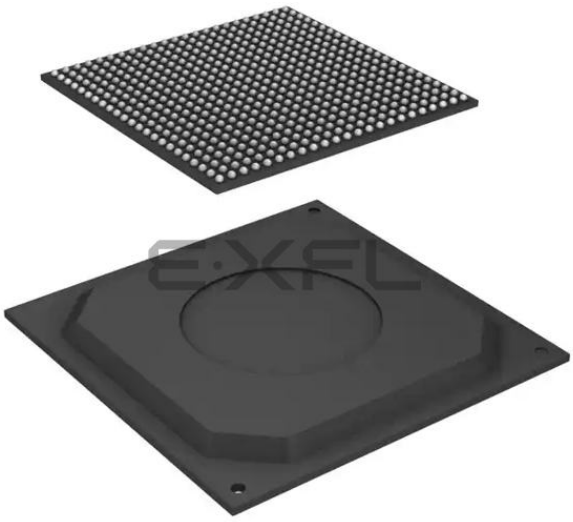

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR2, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	SATA 1.5Gbps (1)
USB	USB 2.0 (2), USB 2.0 + PHY (2)
Voltage - I/O	1.3V, 1.8V, 2.775V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	529-FBGA
Supplier Device Package	529-FBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx534avv8c2r2

  - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4).
- USB
  - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high-speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Automotive environment interfaces:
  - Two controller area network (FlexCAN) interfaces, 1 Mbps each
  - Media local bus or MediaLB (MLB) provides interface to most networks (50 Mbps)
  - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
- Miscellaneous interfaces:
  - One-wire (OWIRE) port
  - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
  - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
  - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
  - Three I^2C ports, supporting 400 kbps
  - Fast Ethernet controller, designed to be compliant with IEEE1588 V1, 10/100 Mbps
  - Sony Phillips Digital Interface (SPDIF), Rx and Tx
  - Key pad port (KPP)
  - Two pulse-width modulators (PWM)
  - GPIO with interrupt capabilities

The system supports efficient and smart power control and clocking:

- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware/features:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX53xA processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX53xA processor system.

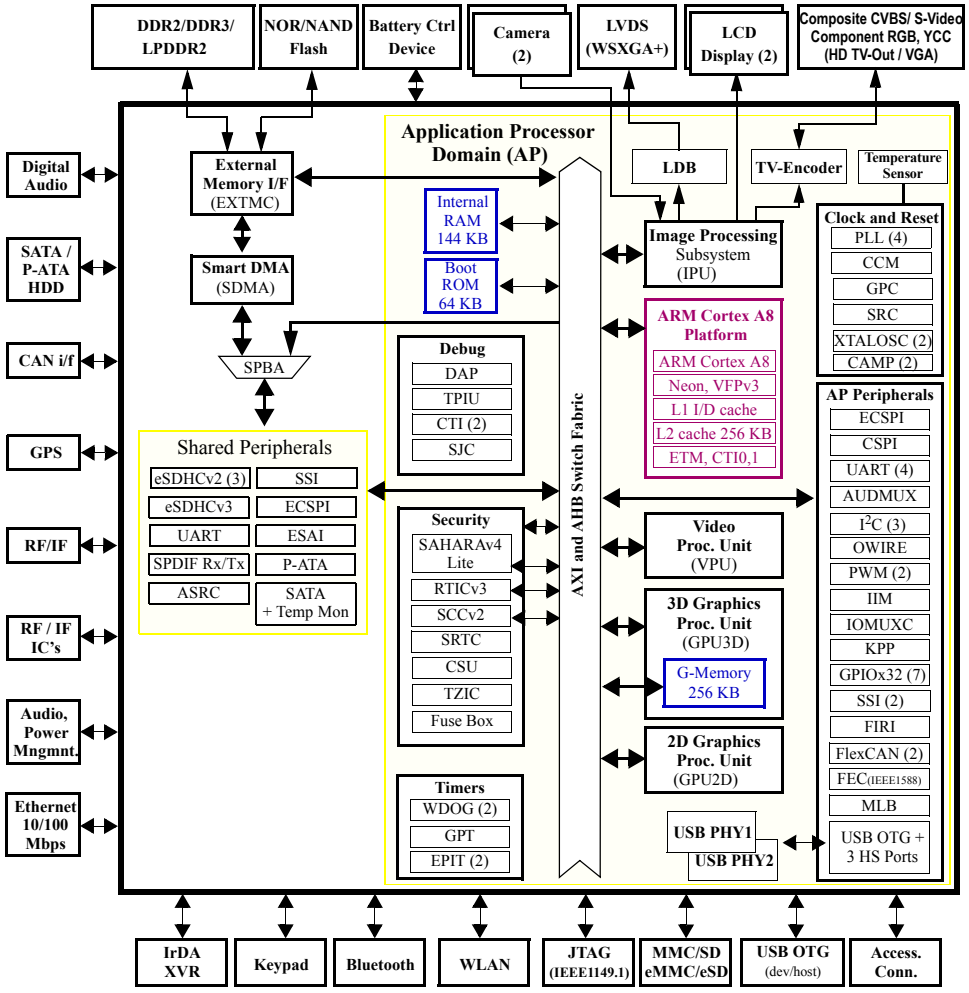

Figure 1. i.MX53xA System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

Table 3. i.MX53xA Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (copy mode) • Up to 8-word buffer for configurable burst transfers to / from the EXTMC • Support of byte swapping and CRC calculations • A library of scripts and API is available
SECRAM	Secure / Non-secure RAM	Internal Memory	Secure / non-secure Internal RAM, controlled by SCC.
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX53xA processor incorporates a mechanism for regulating JTAG access. SJC provides four different JTAG security modes that can be selected through an e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (shared peripheral bus arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported.

4.1.3 Operating Ranges

Table 7 provides the operating ranges of i.MX53xA processor.

Table 7. i.MX53xA Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP	ARM core supply voltage $f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VCC	Peripheral supply voltage[3]	1.25	1.3	1.35	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.35	V
VDDA[4]	Memory arrays voltage	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDDAL1[4]	L1 Cache Memory arrays voltage	1.25	1.30	1.35	V
	L1 Cache Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDD_DIG_PLL[5]	PLL Digital supplies—external regulator option	1.25	1.3	1.35	V
VDD_ANA_PLL[6]	PLL Analog supplies—external regulator option	1.75	1.8	1.95	V
NVCC_CKIH	ESD protection of the CKIH pins, FUSE read Supply and 1.8V bias for the UHVIO pads	1.65	1.8	1.95	V
NVCC_LCD NVCC_JTAG	GPIO digital power supplies	1.65	1.8 or 2.775	3.1	V
NVCC_LVDS	LVDS interface Supply	2.375	2.5	2.75	V
NVCC_LVDS_BG	LVDS Band Gap Supply	2.375	2.5	2.75	V
NVCC_EMI_DRAM	DDR Supply DDR2 range	1.7	1.8	1.9	V
	DDR Supply LPDDR2 range	1.14	1.2	1.3	
	DDR Supply LV-DDR2 range	1.47	1.55	1.63	
		1.42	1.5	1.58	
	DDR Supply DDR3 range	1.42	1.5	1.58	
VDD_FUSE[7]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_PATA NVCC_KEYPAD NVCC_GPIO NVCC_FEC NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_CSI	Ultra High voltage I/O (UHVIO) supplies:				V
	• UHVIO_L	1.65	1.8	1.95	
	• UHVIO_H	2.5	2.775	3.1	
	• UHVIO_UH	3.0	3.3	3.6	

4.4.1 GPIO Output Buffer Impedance

Table 18 shows the GPIO output buffer impedance.

Table 18. GPIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min	Typ		Max	Unit
				OVDD 2.775 V	OVDD 1.875 V		
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 DDR Output Driver Average Impedance

The DDR2/LVDDR2 interface fully complies with JESD79-2E DDR2 JEDEC standard release April, 2008. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

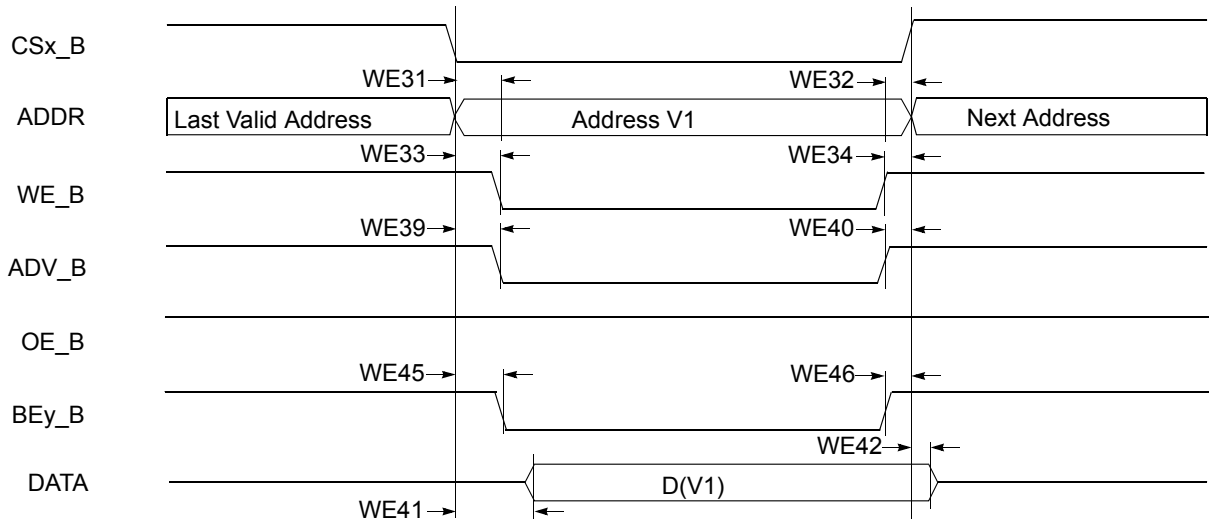

Figure 24. Asynchronous Memory Write Access

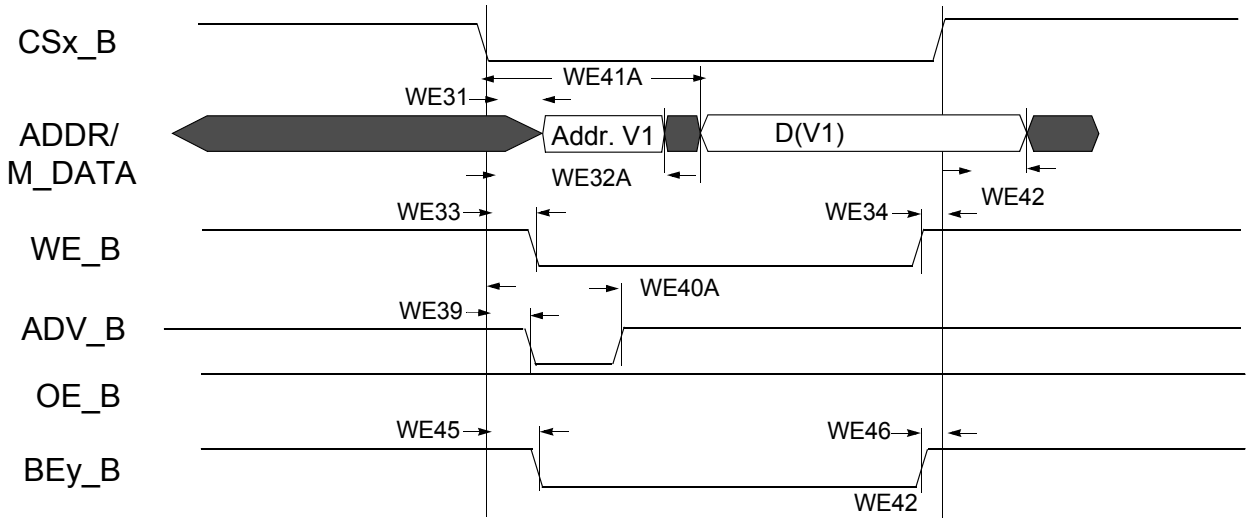

Figure 25. Asynchronous A/D Muxed Write Access

Figure 28 and Table 41 show the address and control timing parameters for DDR2 and DDR3.

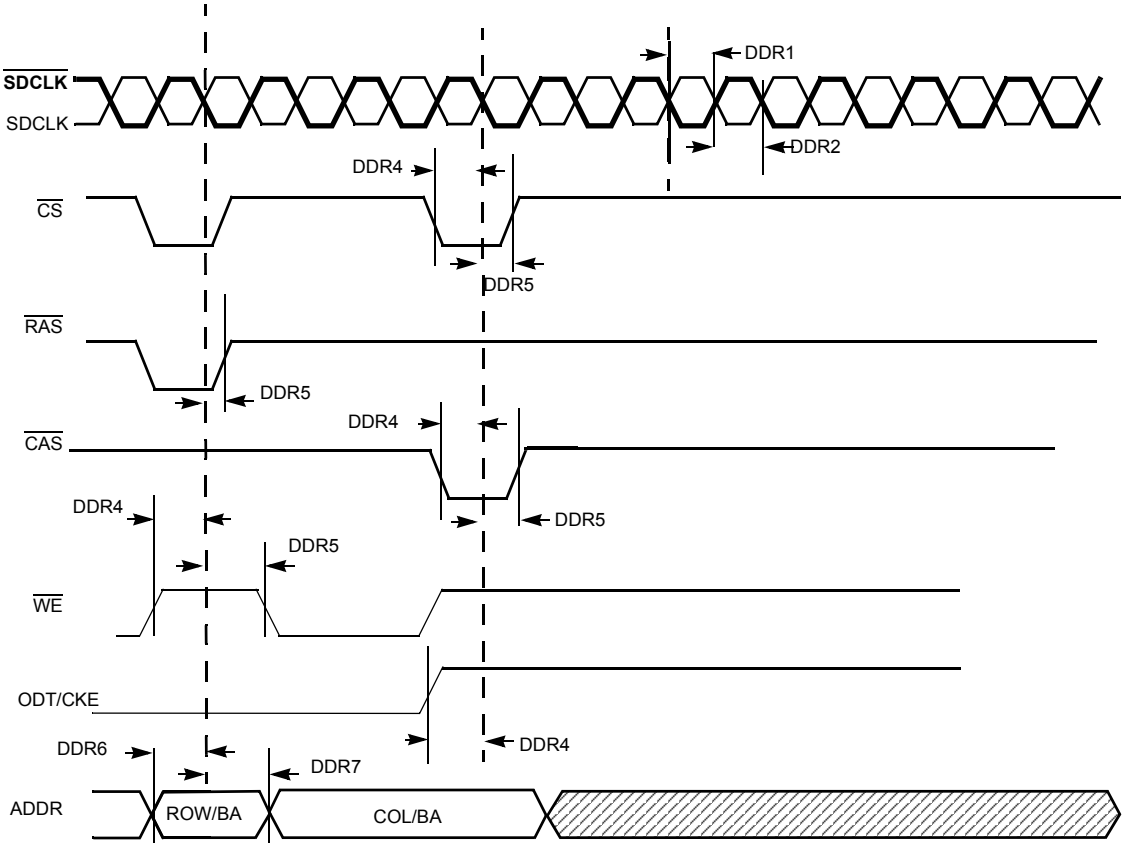

Figure 28. DDR SDRAM Address and Control Parameters for DDR2 and DDR3

Table 41. DDR SDRAM Timing Parameter Table[1] [2]

ID	Parameter	Symbol	SDCLK = 400 MHz		Units
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.48	0.52	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.48	0.52	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	0.6	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	0.6	—	ns
DDR6	Address output setup time	t_{IS}	0.6	—	ns
DDR7	Address output hold time	t_{IH}	0.6	—	ns

1 All timings are refer to Vref level cross point.

2 Reference load model is 25 Ω resistor from each of the DDR outputs to VDD_REF.

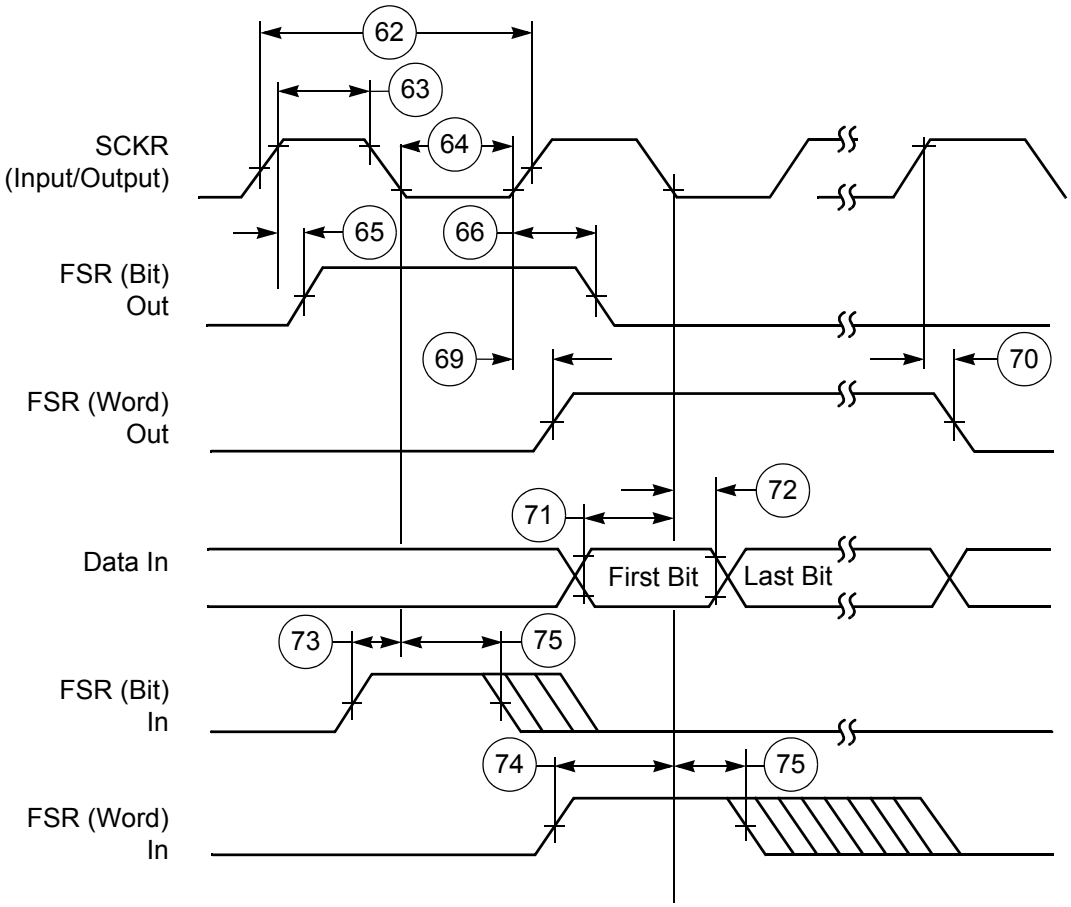

Figure 35. ESAI Receiver Timing

Table 56. RMII Signal Timing (continued)

No.	Characteristics[1]	Min	Max	Unit
M20	FEC_RXD[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RXD[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

1 Test conditions: 25pF on each output signal.

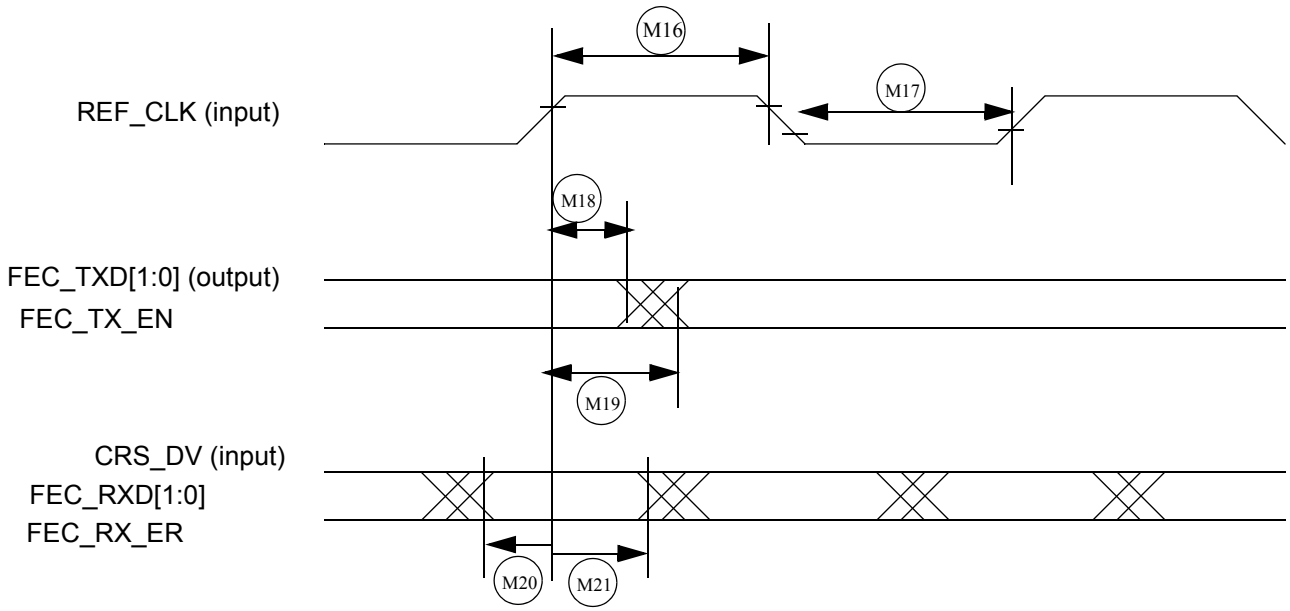

Figure 42. RMII Mode Signal Timing Diagram

4.7.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The electrical characteristics are related to the CAN transceiver external to i.MX53xA such as MC33902 from Freescale. The i.MX53xA has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX53 Reference Manual to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

Table 60. Video Signal Cross-Reference (continued)

i.MX53xA	LCD							Comment[1]
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—	—
DIx_DISP_CLK	PixCLK							—	—
DIx_PIN1	—							VSYNC_IN	May be required for anti-tearing
DIx_PIN2	HSYNC							—	—
DIx_PIN3	VSYNC							—	VSYNC out
DIx_PIN4	—							—	Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							—	
DIx_PIN6	—							—	
DIx_PIN7	—							—	
DIx_PIN8	—							—	
DIx_D0_CS	—							CS0	—
DIx_D1_CS	—							CS1	Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							WR	—
DIx_PIN12	—							RD	—
DIx_PIN13	—							RS1	Register select signal
DIx_PIN14	—							RS2	Optional RS2
DIx_PIN15	DRDY/DV							DRDY	Data validation/blank, data enable
DIx_PIN16	—							—	Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							—	

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

Table 61. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

Table 64. Asynchronous Display Interface Timing Parameters (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP35	Write start	Tdcsw	UP#	write strobe switch, predefined value in DI REGISTER	ns
IP36	Controls hold time for write	Tdchw	DOWN#	write strobe release, predefined value in DI REGISTER	ns

Table 65. Asynchronous Parallel Interface Timing Parameters (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP28	Write system cycle time	Tcycw	Tdicpw - 1.24	Tdicpw[2]	Tdicpw+1.24	ns
IP29	RS start	Tdcsrr	Tdicurs - 1.24	Tdicurs	Tdicurs+1.24	ns
IP30	CS start	Tdcsc	Tdicucs - 1.24	Tdicur	Tdicucs+1.24	ns
IP31	CS hold	Tdchc	Tdicdcs - Tdicucs - 1.24	Tdicdcs[3]-Tdicucs[4]	Tdicdcs - Tdicucs+1.24	ns
IP32	RS hold	Tdchrr	Tdicdrs - Tdicurs - 1.24	Tdicdrs[5]-Tdicurs[6]	Tdicdrs - Tdicurs+1.24	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw - 1.24	Tdicuw	Tdicuw+1.24	ns
IP36	Controls hold time for write	Tdchw	Tdicdw - Tdicuw - 1.24	Tdicpw[7]-Tdicuw[8]	Tdicdw-Tdicuw+1.24	ns
IP38	Slave device data hold time[8]	Troh	Tdrp - Tlbd - Tdicdr+1.24	—	Tdicpr - Tdicdr - 1.24	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display period value for write

$$Tdicpw = T_{DI\_CLK} \times ceil\left[\frac{DI\_ACCESS\_SIZE\_\#}{DI\_CLK\_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER.

[3]Display control down for CS

$$Tdicdcs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

[4]Display control up for CS

$$Tdicucs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_UP\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER.

[5]Display control down for RS

$$Tdicdrs = \frac{1}{2}\left(T_{DI\_CLK} \times ceil\left[\frac{2 \times DISP\_DOWN\_\#}{DI\_CLK\_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER.

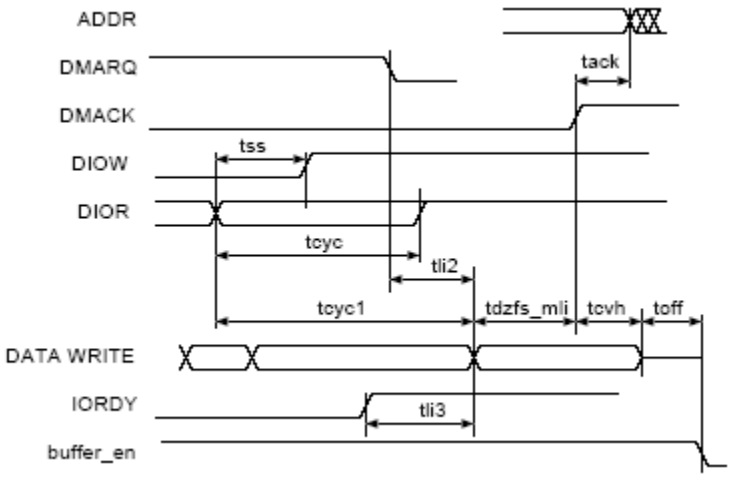

Figure 74. UDMA Out Host Terminates Transfer Timing Diagram

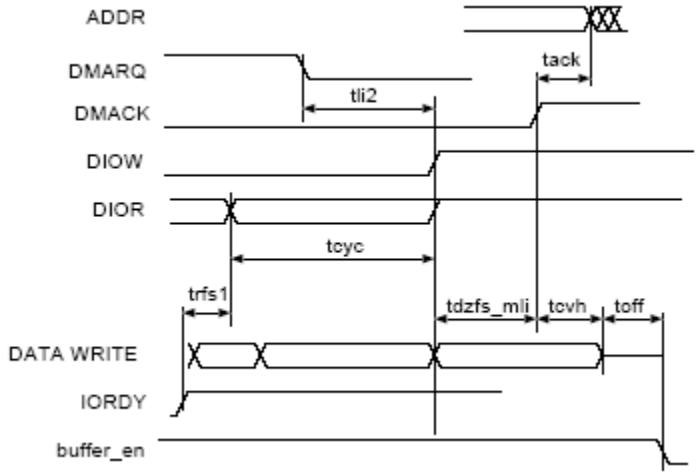

Figure 75. UDMA Out Device Terminates Transfer Timing Diagram

Table 78. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 73, Figure 74, Figure 75	Value	Controlling Variable
tack	tack	tack (min) = (time_ack × T) - (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) - (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) - (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) - (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T - (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc

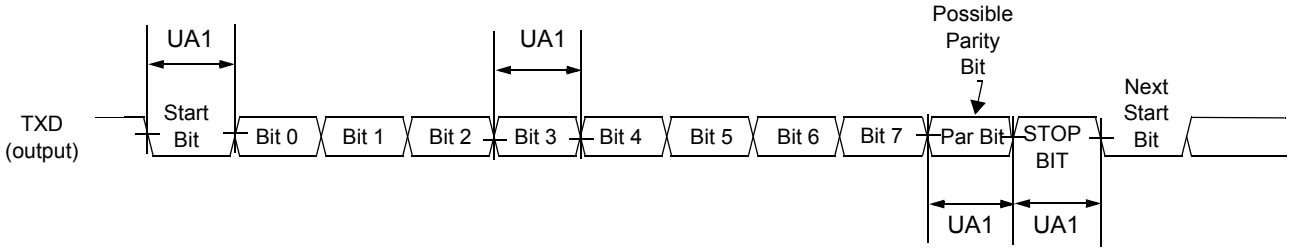

Figure 87. UART RS-232 Serial Mode Transmit Timing Diagram

Table 90. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.7.18.2.2 UART Receiver

Figure 88 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 91 lists serial mode receive timing characteristics.

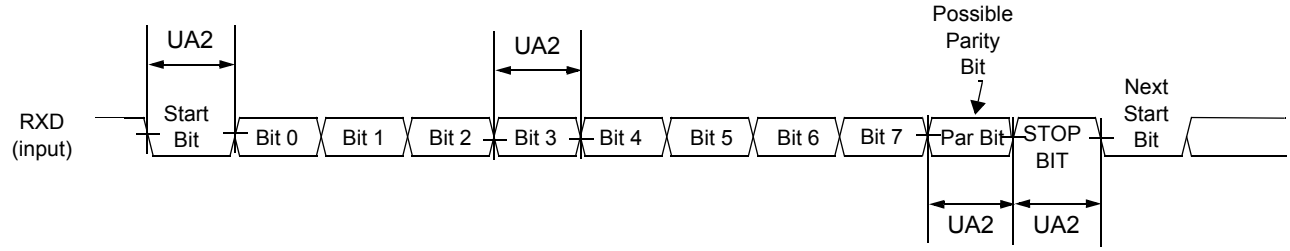

Figure 88. UART RS-232 Serial Mode Receive Timing Diagram

Table 91. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.7.18.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

4.7.18.3.3 UART IrDA Mode Transmitter

Figure 89 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 92 lists the transmit timing characteristics.

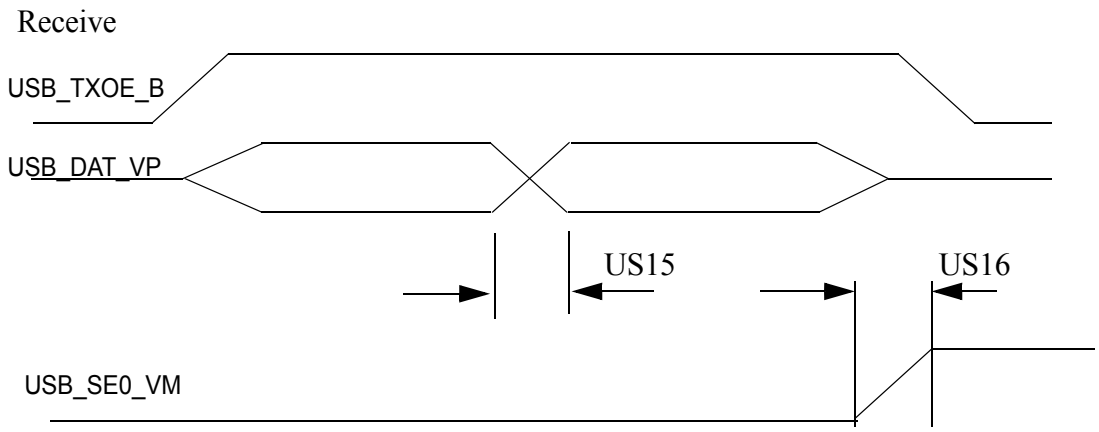

Figure 94. USB Receive Waveform in DAT_SE0 Unidirectional Mode

Table 97. USB Port Timing Specification in DAT_SE0 Unidirectional Mode

No.	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition / Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF

Table 112. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
EIM	EIM	EIM	• Lower 16-bit data bus A/D multiplexed or upper 16 bit data bus non multiplexed • Only CS0 is supported.
NAND Flash	EXTMC	NAND	• 8/16-bit • NAND data can be muxed either over EIM data or PATA data • Only CS0 is supported
SD/MMC	eSDHCv2-1	PATA_DATA[11:8], SD1_DATA[3:0], SD1_CMD, SD1_CLK	1, 4, or 8 bit
SD/MMC	eSDHCv2-2	PATA_DATA[15:12], SD2_CLK, SD2_CMD, SD2_DATA[3:0]	1, 4, or 8 bit
SD/MMC	eSDHCv3-3	PATA_RESET_B, PATA_IORDY, PATA_DA_0, PATA_DATA[3:0], PATA_DATA[11:8]	1, 4, or 8 bit
SD/MMC	eSDHCv2-4	PATA_DA1, PATA_DA_2, PATA_DATA[7:4], PATA_DATA[15:12]	1, 4, or 8 bit
I2C	I2C-1	EIM_D21, EIM_D28	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D[18:17]	—
PATA	PATA	PATA_DIOW, PATA_DMACK, PATA_DMARQ, PATA_BUFFER_EN, PATA_INTRQ, PATA_DIOR, PATA_RESET_B, PATA_IORDY, PATA_DA_[2:0], PATA_CS_[1:0], PATA_DATA[15:0]	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT, SATA_REFCLKM, SATA_REFCLKP	—
UART	UARTv2-1	CSI0_DAT[11:10]	RXD/TXD only
UART	UARTv2-2	PATA_DMARQ, PATA_BUFFER_EN	RXD/TXD only
UART	UARTv2-3	EIM_D24, EIM_D25	RXD/TXD only
UART	UARTv2-4	CSI0_DAT[13:12]	RXD/TXD only
UART	UARTv2-5	CSI0_DAT[15:14]	RXD/TXD only
USB	USB-OTG PHY	USB_H1_GPANAIO USB_H1_RREFEXT USB_H1_DP USB_H1_DN USB_H1_VBUS	—

5.3 Power Setup During Boot

By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In order to achieve the standard operating mode (see VDD_DIG_PLL on Table 7), LDO output to VDD_DIG_PLL should be configured by software by boot code after power-up to 1.3 V output. This is done by programming the PLL1P2_VREG bits.

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
DRAM_SDODT0	J18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_ODT[0]	Output	Low
DRAM_SDODT1	R18	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_ODT[1]	Output	Low
DRAM_SDQS0	H23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[0]	Input	Low
DRAM_SDQS0_B	H22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[0]	Input	High
DRAM_SDQS1	D23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[1]	Input	Low
DRAM_SDQS1_B	D22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[1]	Input	High
DRAM_SDQS2	T22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[2]	Input	Low
DRAM_SDQS2_B	T23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[2]	Input	High
DRAM_SDQS3	Y22	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS[3]	Input	Low
DRAM_SDQS3_B	Y23	NVCC_EMI_DRAM	DDR3CLK	ALT0	EXTMC	emi_DRAM_SDQS_B[3]	Input	High
DRAM_SDWE	L19	NVCC_EMI_DRAM	DDR3	ALT0	EXTMC	emi_DRAM_SDWE	Output	High
ECKIL	AC10	NVCC_SRTC_POW	ANALOG	—	SRTC	ECKIL {no block I/O by this name in RM}	—	—
EIM_A16	AA5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[16]	Output[2]	—
EIM_A17	V7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[17]	Output[2]	—
EIM_A18	AB3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[18]	Output[2]	—
EIM_A19	W7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[19]	Output[2]	—
EIM_A20	Y6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[20]	Output[2]	—
EIM_A21	AA4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[21]	Output[2]	—
EIM_A22	AA3	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[22]	Output[2]	—
EIM_A23	V6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[23]	Output	—
EIM_A24	Y5	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[24]	Output	—
EIM_A25	W6	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_A[25]	Output	—
EIM_BCLK	W11	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_BCLK	Output	—

Table 114. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Out of Reset Condition[1]				
				Alt. Mode	Block Instance	Block I/O	Direction	Config. Value
EIM_CS0	W8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[0]	Output	—
EIM_CS1	Y7	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_EIM_CS[1]	Output	—
EIM_D16	U6	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[16]	Input	100 KΩ PU
EIM_D17	U5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[17]	Input	100 KΩ PU
EIM_D18	V1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[18]	Input	100 KΩ PU
EIM_D19	V2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[19]	Input	100 KΩ PU
EIM_D20	W1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[20]	Input	100 KΩ PU
EIM_D21	V3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[21]	Input	100 KΩ PU
EIM_D22	W2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[22]	Input	360 KΩ PD
EIM_D23	Y1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[23]	Input	100 KΩ PU
EIM_D24	Y2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[24]	Input	100 KΩ PU
EIM_D25	W3	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[25]	Input	100 KΩ PU
EIM_D26	V5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[26]	Input	100 KΩ PU
EIM_D27	V4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[27]	Input	100 KΩ PU
EIM_D28	AA1	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[28]	Input	100 KΩ PU
EIM_D29	AA2	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[29]	Input	100 KΩ PU
EIM_D30	W4	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[30]	Input	100 KΩ PU
EIM_D31	W5	NVCC_EIM_SEC	UHVIO	ALT1	GPIO-3	gpio3_GPIO[31]	Input	360 KΩ PD
EIM_DA0	Y8	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[0]	Input[2]	100 KΩ PU
EIM_DA1	AC4	NVCC_EIM_MAIN	UHVIO	ALT0	EXTMC	emi_NAND_EIM_DA[1]	Input[2]	100 KΩ PU

6.1.4 19 x 19 mm, 0.8 mm Pitch Ball Map

Table 115 shows the 19 × 19 mm, 0.8 mm pitch ball map.

Table 115. 19 x 19 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	GND	GPIO_17	GPIO_7	GPIO_5	GPIO_3	JTAG_TDO	JTAG_TMS	VPH	SATA_TXP	GND	SATA_RXM	GND	SATA_REFCLKM	VP	USB_H1_GPANAIO	USB_H1_DP	GND	USB_OTG_DN	SD1_DATA0	RESET_IN_B	GND	GND	A
B	GND	SVDDGP	KEY_ROW0	GPIO_19	GPIO_8	GPIO_6	GPIO_1	JTAG_TDI	VPH	SATA_TXM	GND	SATA_RXP	GND	SATA_REFCLKP	VP	USB_H1_RREFEXT	USB_H1_DN	GND	USB_OTG_DP	BOOT_MODE1	CKIH1	SVCC	GND	B
C	DISP0_DAT21	DI0_PIN3	DISP0_DAT23	KEY_COL2	KEY_COL0	GPIO_16	GPIO_2	GPIO_0	JTAG_MOD	FEC_TX_EN	FEC_RXD0	GND	SATA_REXT	SD2_DATA1	SD2_CMD	USB_OTG_ID	SD1_DATA1	BOOT_MODE0	POR_B	GND	GND	DRAM_D15	DRAM_D13	C
D	DISP0_DAT16	DI0_PIN4	DI0_PIN2	KEY_ROW3	KEY_ROW2	KEY_ROW1	GPIO_18	GPIO_4	JTAG_TCK	FEC_TXD1	FEC_CRS_DV	FEC_MDIO	SD2_DATA0	SD2_DATA2	USB_H1_VBUS	USB_OTG_RREFEXT	TEST_MODE	CKIH2	GND	DRAM_D11	DRAM_D9	DRAM_SDQS1_B	DRAM_SDQS1	D
E	DISP0_DAT13	DISP0_DAT9	DISP0_DAT22	DI0_PIN15	KEY_COL4	KEY_ROW4	KEY_COL1	GPIO_9	JTAG_TRSTB	FEC_MDC	FEC_RXD1	FEC_REF_CLK	SD2_DATA3	SD2_CLK	USB_OTG_VBUS	SD1_CLK	FASTR_DIG	FASTR_ANA	GND	DRAM_DQM1	DRAM_D8	DRAM_D10	DRAM_D12	E
F	DISP0_DAT3	DISP0_DAT14	DISP0_DAT15	DISP0_DAT20	DISP0_DAT17	KEY_COL3	NVCC_KEYPAD	NVCC_GPIO	VDDAL1	FEC_TXD0	NVCC_FEC	FEC_RX_ER	USB_H1_VDDA25	USB_OTG_VDDA25	USB_OTG_GPANAIO	SD1_DATA3	SD1_DATA2	SD1_CMD	GND	GND	GND	GND	DRAM_D14	F

Table 116. i.MX53xA Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 4 (continued)	11/2011	• In Table 17, "LVDS DC Electrical Characteristics," on page 35, changed test condition “Rload=100Ω padP, –padN” to “Rload = 100Ω between padP and padN”. • In Table 36, " NFC—Timing Characteristics," on page 52, corrected footnote number for TdI. • In Table 50, "SD/eMMC4.3 Interface Timing Specification," on page 75, updated eSDHC output delay. • In Table 51, "eMMC4.4 Interface Timing Specification," on page 76, updated eSDHC output delay. • In Table 63, "TV Encoder Video Performance Specifications," on page 97, changed test condition “Fout = 9.28 MHz” for SFDR to “Fout = 8.3 MHz”. • Updated Figure 58, "MediaLB Timing," on page 106. • In Table 66, "MLB 256/512 Fs Timing Parameters," on page 107: —Changed the Min value for t_{dsmcf}, t_{dhmcf}, and t_{mcfdz} parameters to 2, 2.5, and 4, respectively —Changed the Max value for t_{mcfdz} parameter to 10 —Added a new row for t_{delay} parameter at the end of the table • In Table 67, "MLB Device 1024 Fs Timing Parameters," on page 108: —Changed the Min value for t_{dsmcf}, t_{dhmcf}, and t_{mcfdz} parameters to 2, 2.5, and 4, respectively —Changed the Max value for t_{mcfdz} parameter to 10 —Added a new row for t_{delay} parameter at the end of the table
Rev. 3	06/2011	• In Section 4.1.1, “Absolute Maximum Ratings,” updated the caution note on page 19.