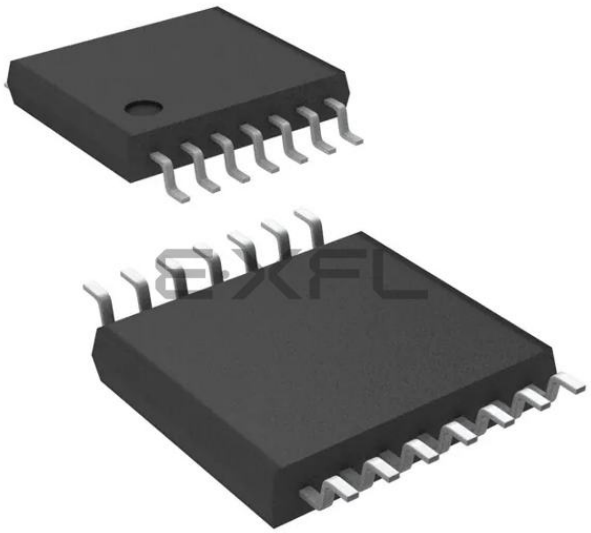

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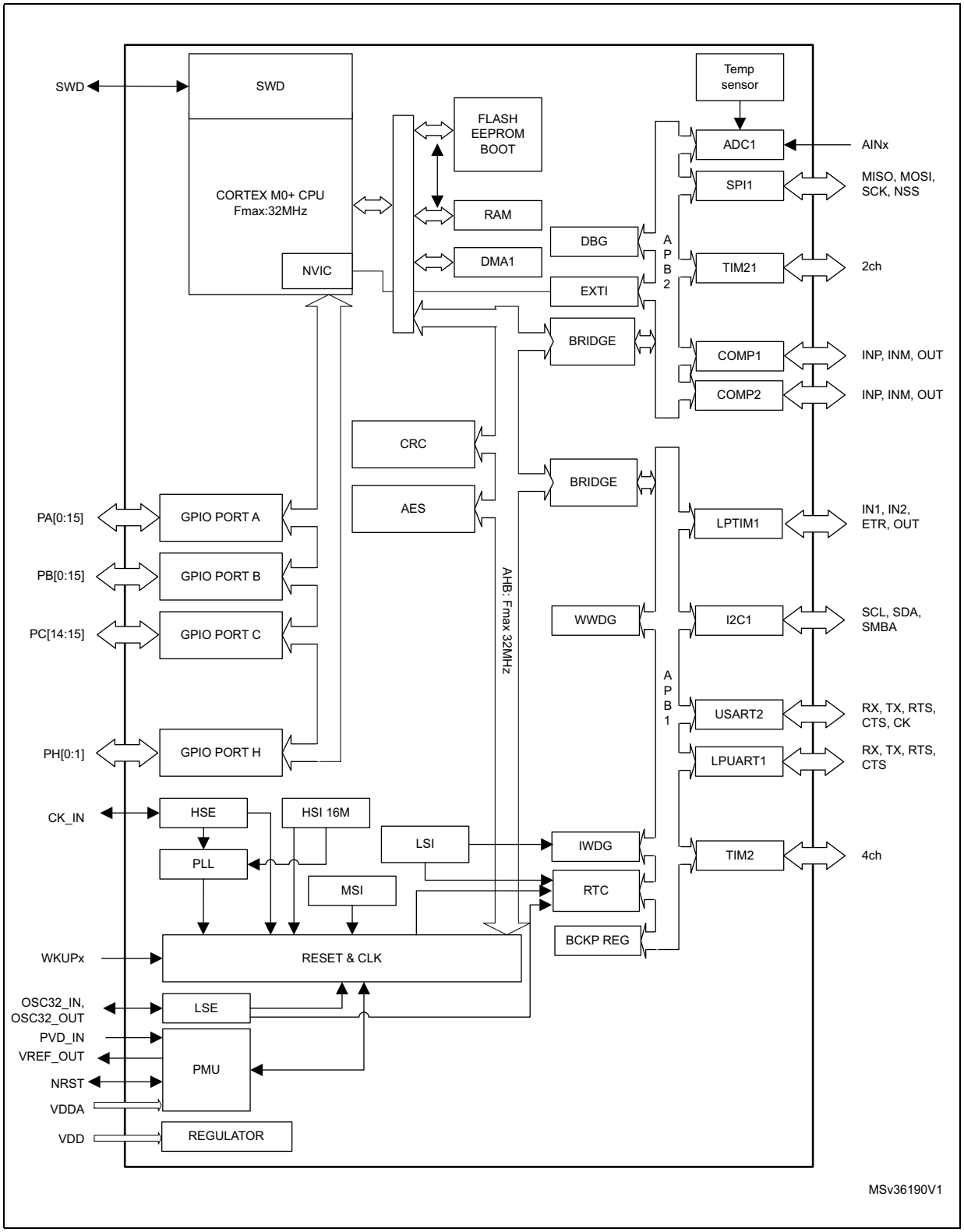
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.65V ~ 3.6V |
| Data Converters | A/D 4x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 14-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | 14-TSSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l021d4p6 |

# Contents

**Figure 1. STM32L021x4 block diagram**



# 3 Functional overview

## 3.1 Low-power modes

The ultra-low-power STM32L021x4 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 ($V_{DD}$ range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full $V_{DD}$ range), with a maximum CPU frequency of 16 MHz
- Range 3 (full $V_{DD}$ range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the $V_{CORE}$ domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage ($V_{REFINT}$) in Stop mode. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

*Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.*

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD/VDDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

### 3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nBOOT_SEL option bits are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA7, PA13 and PA14 on TSSOP14 package or PA4, PA5, PA6 and PA7 on other packages) or USART2 (PA2, PA3 and PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

## 3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

## 3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

The BOOT0 pin is shared with PB9 GPIO pin. This pin is an input-only pin. If nBOOT_SEL option bit is reset, sampling this pin on NRST rising edge gives the internal BOOT0 state. This pin then works as PB9 pin. The input voltage characteristics of this pin are specific for BOOT0 pin type (see *Table 49: I/O static characteristics*).

### Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 26 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event

Table 12. Pin definitions (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP14 | UFQFPN20 | TSSOP20 | UFQFPN28 | LQFP32 | UFQFPN32[1] | | | | | Alternate functions | Additional functions |
| 14 | 17 | 20 | 22 | 24 | 24 | PA14 | I/O | FT | - | SWCLK, LPTIM1_OUT, I2C1_SMBA, USART2_TX, SPI1_MISO, LPUART1_TX, COMP2_OUT | - |
| - | - | - | 23 | 25 | 25 | PA15 | I/O | FT | - | SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1 | - |
| - | - | - | 24 | 26 | 26 | PB3 | I/O | FT | - | SPI1_SCK, TIM2_CH2, EVENTOUT | COMP2_INM |
| - | - | - | 25 | 27 | 27 | PB4 | I/O | FT | - | SPI1_MISO, EVENTOUT | COMP2_INP |
| - | - | - | 26 | 28 | 28 | PB5 | I/O | FT | - | SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM21_CH1 | COMP2_INP |
| - | 18 | - | 27 | 29 | 29 | PB6 | I/O | FTf | - | USART2_TX, I2C1_SCL, LPTIM1_ETR, TIM2_CH3, LPUART1_TX | COMP2_INP |
| - | 19 | - | 28 | 30 | 30 | PB7 | I/O | FTf | - | USART2_RX, I2C1_SDA, LPTIM1_IN2, TIM2_CH4, LPUART1_RX | COMP2_INP, VREF_PVD_IN |
| 1 | 20 | 1 | 1 | 31 | 31 | PB9-BOOT0 | I | B | - | - | BOOT0 (Boot memory selection) |
| - | - | - | - | - | 32 | PB8 | I/O | FTf | - | USART2_TX, EVENTOUT, I2C1_SCL, SPI1_NSS | - |

**Table 12. Pin definitions (continued)**

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TSSOP14 | UFQFPN20 | TSSOP20 | UFQFPN28 | LQFP32 | UFQFPN32[1] | | | | | Alternate functions | Additional functions |
| - | - | - | - | 32 | - | VSS | S | | (4) | - | - |
| - | - | - | - | 1 | 1 | VDD | S | - | (5) | - | - |

1. VSS pins are connected to the exposed pad (see *Figure 35: UFQFPN32, 5 x 5 mm, 32-pin package outline*).
2. Device reset input/internal reset output (active low).
3. Analog power supply.
4. On TSSOP14 package, $V_{DDA}$ is internally connected to $V_{DD}$.
5. Digital and analog ground.
6. Digital power supply.

## 6.3 Operating conditions

### 6.3.1 General operating conditions

**Table 17. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 32 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 32 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 32 | |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled | 1.65 | 3.6 | V |
| | | BOR detector enabled, at power on | 1.8 | 3.6 | |
| | | BOR detector disabled, after power on | 1.65 | 3.6 | |
| $V_{DDA}$ | Analog operating voltage (all features) | Must be the same voltage as $V_{DD}$(1) | 1.65 | 3.6 | V |
| $V_{IN}$ | Input voltage on FT, FTf and RST pins(2) | 2.0 V ≤ $V_{DD}$ ≤3.6 V | -0.3 | 5.5 | V |
| | | 1.65 V ≤ $V_{DD}$ ≤2.0 V | -0.3 | 5.2 | |
| | Input voltage on BOOT0 pin | - | 0 | 5.5 | |
| | Input voltage on TC pin | - | -0.3 | $V_{DD}$+0.3 | |
| $P_D$ | Power dissipation at $T_A$ = 85 °C (range 6) or $T_A$ =105 °C (rage 7) (3) | LQFP32 package | - | 333 | mW |
| | | UFQFPN32 package | - | 513 | |
| | | UFQFPN28 package | - | 206 | |
| | | TSSOP20 package | - | 270 | |
| | | UFQFPN20 package | - | 196 | |
| | | TSSOP14 package | - | 210 | |
| | Power dissipation at $T_A$ = 125 °C (range 3) (3) | LQFP32 package | - | 83 | |
| | | UFQFPN32 package | - | 128 | |
| | | UFQFPN28 package | - | 52 | |
| | | TSSOP20 package | - | 67 | |
| | | UFQFPN20 package | - | 49 | |
| | | TSSOP14 package | - | 53 | |

**Table 18. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BOR3}$ | Brown-out reset threshold 3 | Falling edge | 2.45 | 2.55 | 2.6 | V |
| | | Rising edge | 2.54 | 2.66 | 2.7 | |
| $V_{BOR4}$ | Brown-out reset threshold 4 | Falling edge | 2.68 | 2.8 | 2.85 | |
| | | Rising edge | 2.78 | 2.9 | 2.95 | |
| $V_{PVD0}$ | Programmable voltage detector threshold 0 | Falling edge | 1.8 | 1.85 | 1.88 | |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| $V_{PVD1}$ | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| $V_{PVD2}$ | PVD threshold 2 | Falling edge | 2.20 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| $V_{PVD3}$ | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| $V_{PVD4}$ | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| $V_{PVD5}$ | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| $V_{hyst}$ | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Guaranteed by characterization results, not tested in production.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

**Table 25. Current consumption in Sleep mode**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Sleep) | Supply current in Sleep mode, Flash OFF | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 1 MHz | 36.5 | 70 | µA |
| | | | | 2 MHz | 58 | 95 | |
| | | | | 4 MHz | 100 | 150 | |
| | | | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10 | 4 MHz | 125 | 170 | |
| | | | | 8 MHz | 230 | 300 | |
| | | | | 16 MHz | 450 | 540 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 8 MHz | 275 | 350 | |
| | | | | 16 MHz | 555 | 650 | |
| | | | | 32 MHz | 1350 | 1600 | |
| | | MSI clock | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 65 kHz | 15.5 | 32 | |
| | | | | 524 kHz | 26.5 | 55 | |
| | | | | 4.2 MHz | 115 | 160 | |
| | | HSI16 clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10 | 16 MHz | 585 | 670 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 32 MHz | 1500 | 1700 | |
| | Supply current in Sleep mode, Flash ON | $f_{HSE}$ = $f_{HCLK}$ up to 16 MHz included, $f_{HSE}$ = $f_{HCLK}$/2 above 16 MHz (PLL ON)(2) | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 1 MHz | 49 | 88 | |
| | | | | 2 MHz | 69 | 120 | |
| | | | | 4 MHz | 115 | 190 | |
| | | | Range 2, CORE=1.5 V, VOS[1:0]=10 | 4 MHz | 135 | 200 | |
| | | | | 8 MHz | 240 | 340 | |
| | | | | 16 MHz | 460 | 650 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 8 MHz | 290 | 400 | |
| | | | | 16 MHz | 565 | 750 | |
| | | | | 32 MHz | 1350 | 1900 | |
| | | MSI clock | Range 3, $V_{CORE}$=1.2 V, VOS[1:0]=11 | 65 kHz | 26.5 | 46 | |
| | | | | 524 kHz | 38.5 | 70 | |
| | | | | 4.2 MHz | 125 | 190 | |
| | | HSI16 clock source (16 MHz) | Range 2, $V_{CORE}$=1.5 V, VOS[1:0]=10 | 16 MHz | 600 | 760 | |
| | | | Range 1, $V_{CORE}$=1.8 V, VOS[1:0]=01 | 32 MHz | 1500 | 1850 | |

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 26. Current consumption in Low-power Run mode**

| Symbol | Parameter | Conditions | | | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (LP Run) | Supply current in Low-power run mode | All peripherals OFF, code executed from RAM, Flash switched OFF, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 5.7 | 8.1 | µA |
| | | | | $T_A$ = 85 °C | 6.5 | 9 | |
| | | | | $T_A$ = 105 °C | 8 | 13 | |
| | | | | $T_A$ = 125 °C | 11.5 | 22 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ =-40 °C to 25 °C | 8.7 | 11 | |
| | | | | $T_A$ = 85 °C | 9.5 | 12 | |
| | | | | $T_A$ = 105 °C | 11 | 15 | |
| | | | | $T_A$ = 125 °C | 15 | 24 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 17 | 19 | |
| | | | | $T_A$ = 55 °C | 17 | 19.5 | |
| | | | | $T_A$ = 85 °C | 17.5 | 20 | |
| | | | | $T_A$ = 105 °C | 19 | 22 | |
| | | | | $T_A$ = 125 °C | 22.5 | 31 | |
| | | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | MSI clock, 65 kHz $f_{HCLK}$ = 32 kHz | $T_A$ = -40 °C to 25 °C | 18 | 22 | |
| | | | | $T_A$ = 85 °C | 20 | 24 | |
| | | | | $T_A$ = 105 °C | 22 | 27 | |
| | | | | $T_A$ = 125 °C | 26.5 | 37 | |
| | | | MSI clock, 65 kHz $f_{HCLK}$ = 65 kHz | $T_A$ = -40 °C to 25 °C | 22 | 25 | |
| | | | | $T_A$ = 85 °C | 24 | 27 | |
| | | | | $T_A$ = 105 °C | 26 | 30 | |
| | | | | $T_A$ = 125 °C | 30.5 | 39 | |
| | | | MSI clock, 131 kHz $f_{HCLK}$ = 131 kHz | $T_A$ = -40 °C to 25 °C | 32 | 34 | |
| | | | | $T_A$ = 55 °C | 32.5 | 35 | |
| | | | | $T_A$ = 85 °C | 34 | 37 | |
| | | | | $T_A$ = 105 °C | 36 | 39 | |
| | | | | $T_A$ = 125 °C | 40 | 47 | |

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

**Table 28. Typical and maximum current consumptions in Stop mode**

| Symbol | Parameter | Conditions | Typ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ (Stop) | Supply current in Stop mode | $T_A$ = -40°C to 25°C | 0.34 | 0.99 | µA |
| | | $T_A$ = 55°C | 0.43 | 1.9 | |
| | | $T_A$= 85°C | 0.94 | 4.2 | |
| | | $T_A$ = 105°C | 2.0 | 9 | |
| | | $T_A$ = 125°C | 4.9 | 19 | |

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

**Figure 17. $I_{DD}$ vs $V_{DD}$, at $T_A$= -40/25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive**

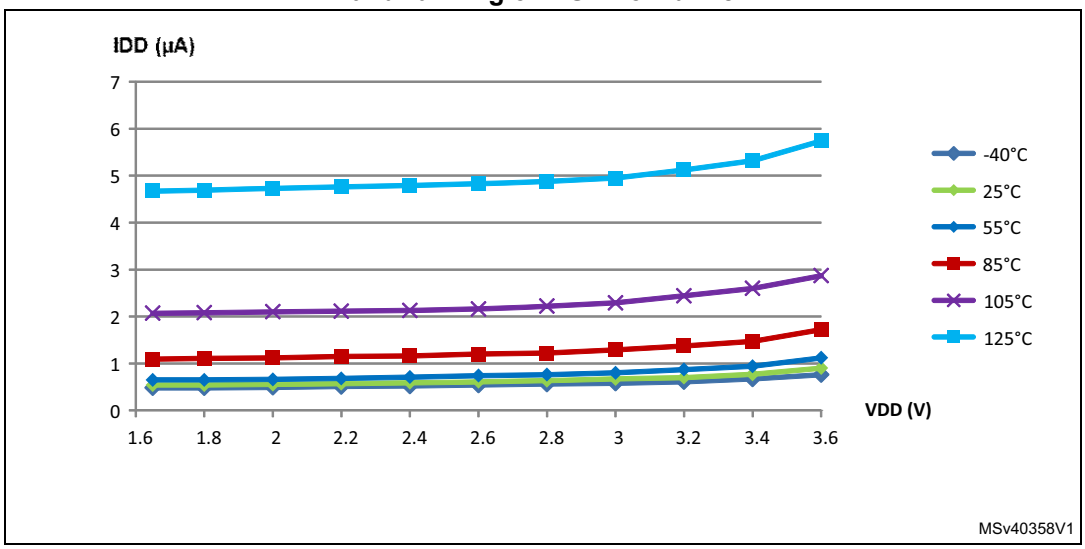
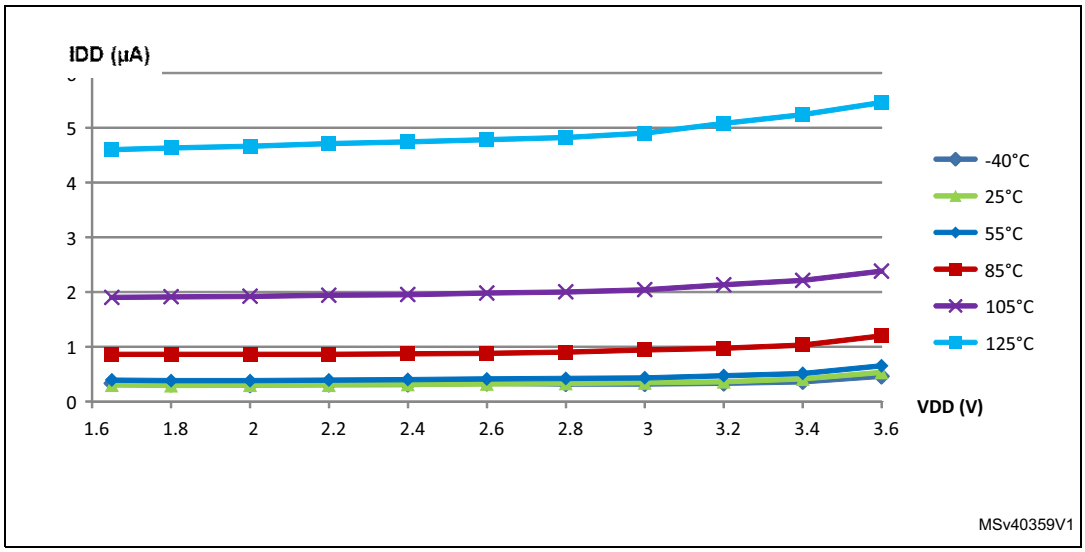



**Figure 18. $I_{DD}$ vs $V_{DD}$, at $T_A$= -40/25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF**



## 6.3.7 Internal clock source characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 17*.

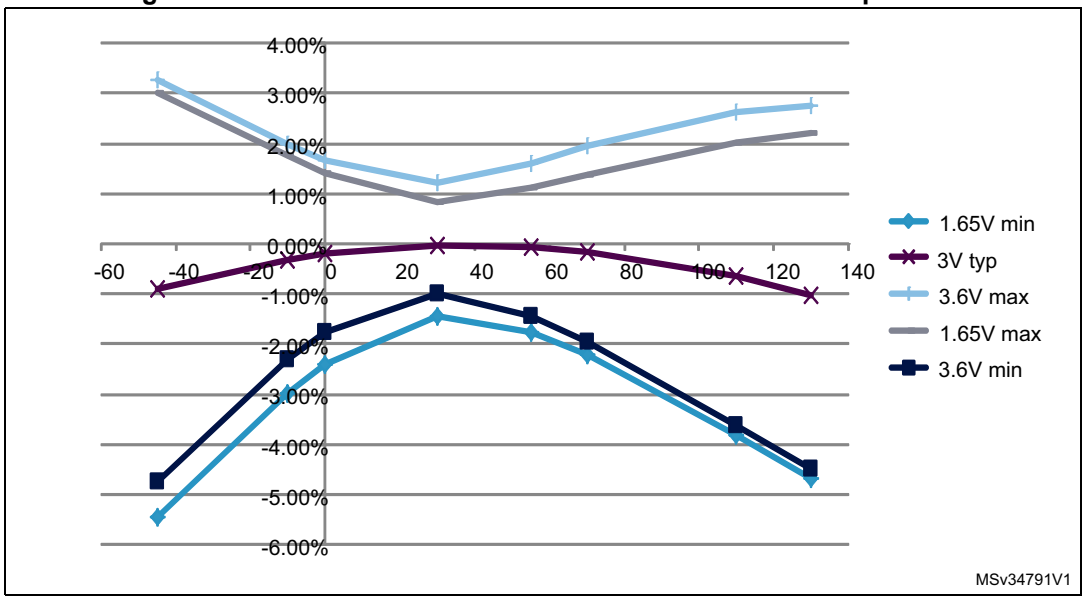
### High-speed internal 16 MHz (HSI16) RC oscillator

**Table 37. 16 MHz HSI16 oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI16}$ | Frequency | $V_{DD}$ = 3.0 V | - | 16 | - | MHz |
| $TRIM^{(1)(2)}$ | HSI16 user-trimmed resolution | Trimming code is not a multiple of 16 | - | ±0.4 | 0.7 | % |
| | | Trimming code is a multiple of 16 | - | - | ±1.5 | % |
| $ACC_{HSI16}$ (2) | Accuracy of the factory-calibrated HSI16 oscillator | $V_{DDA}$ = 3.0 V, $T_A$ = 25 °C | -1(3) | - | 1(3) | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = 0 to 55 °C | -1.5 | - | 1.5 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 70 °C | -2 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 85 °C | -2.5 | - | 2 | % |
| | | $V_{DDA}$ = 3.0 V, $T_A$ = -10 to 105 °C | -4 | - | 2 | % |
| | | $V_{DDA}$ = 1.65 V to 3.6 V<br>$T_A$ = -40 to 125 °C | -5.45 | - | 3.25 | % |
| $t_{SU(HSI16)}^{(2)}$ | HSI16 oscillator startup time | - | - | 3.7 | 6 | µs |
| $I_{DD(HSI16)}^{(2)}$ | HSI16 oscillator power consumption | - | - | 100 | 140 | µA |

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by test in production.

**Figure 22. HSI16 minimum and maximum value versus temperature**



## Low-speed internal (LSI) RC oscillator

**Table 38. LSI oscillator characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(1) | LSI frequency | 26 | 38 | 56 | kHz |
| $D_{LSI}$(2) | LSI oscillator frequency drift<br>0°C ≤ $T_A$ ≤ 85°C | -10 | - | 4 | % |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | - | 200 | µs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | 400 | 510 | nA |

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design, not tested in production.

## Multi-speed internal (MSI) RC oscillator

**Table 39. MSI oscillator characteristics**

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{MSI}$ | Frequency after factory calibration, done at $V_{DD}$= 3.3 V and $T_A$ = 25 °C | MSI range 0 | 65.5 | - | kHz |
| | | MSI range 1 | 131 | - | |
| | | MSI range 2 | 262 | - | |
| | | MSI range 3 | 524 | - | |
| | | MSI range 4 | 1.05 | - | MHz |
| | | MSI range 5 | 2.1 | - | |
| | | MSI range 6 | 4.2 | - | |
| $ACC_{MSI}$ | Frequency error after factory calibration | - | ±0.5 | - | % |
| $D_{TEMP(MSI)}$(1) | MSI oscillator frequency drift<br>0 °C ≤ $T_A$ ≤ 85 °C | - | ±3 | - | % |
| $D_{VOLT(MSI)}$(1) | MSI oscillator frequency drift<br>1.65 V ≤ $V_{DD}$ ≤ 3.6 V, $T_A$ = 25 °C | - | - | 2.5 | %/V |
| $I_{DD(MSI)}$(2) | MSI oscillator power consumption | MSI range 0 | 0.75 | - | µA |
| | | MSI range 1 | 1 | - | |
| | | MSI range 2 | 1.5 | - | |
| | | MSI range 3 | 2.5 | - | |
| | | MSI range 4 | 4.5 | - | |
| | | MSI range 5 | 8 | - | |
| | | MSI range 6 | 15 | - | |

**Table 47. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +125 °C conforming to JESD78A | II level A |

## 6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 48*.

**Table 48. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on all FT pins | -5 (1) | NA | |
| | Injected current on any other pin | -5 (1) | +5 | |

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

## 6.3.19 Communications interfaces

### I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 62*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 61* for the analog filter characteristics).

**Table 61. I2C analog filter characteristics(1)**

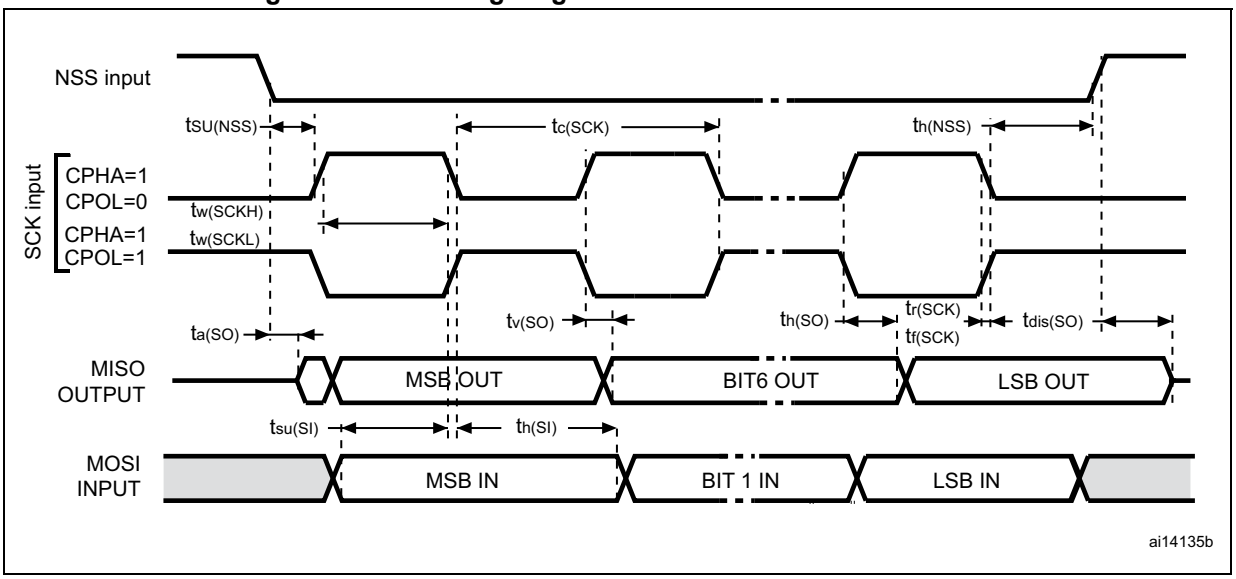
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by the analog filter | 50(2) | 100(3) | ns |

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

**Table 62. I2C frequency in all I2C modes**

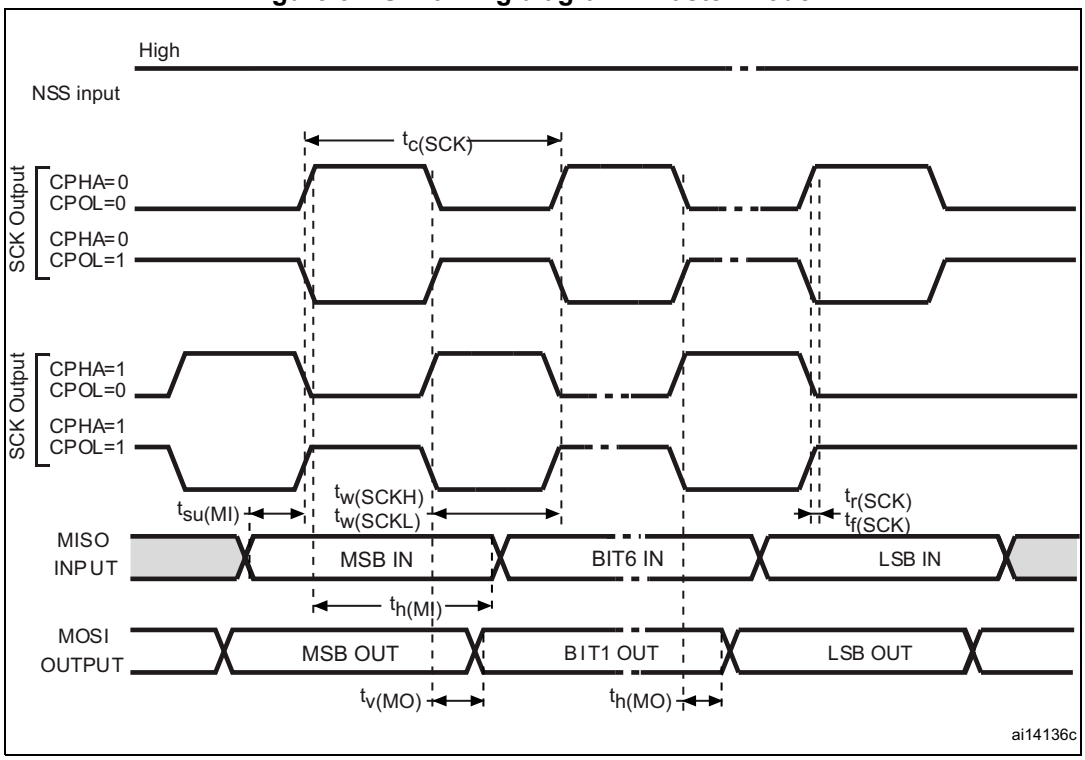
| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| $f_{I2CCLK}$ | I2C clock frequency | Standard-mode | | 2 | MHz |
| | | Fast-mode | | 8 | |
| | | Fast-mode Plus | Analog filter ON, DNF = 0 | 18 | |
| | | | Analog filter OFF, DNF = 1 | 16 | |

**Figure 30. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 31. SPI timing diagram - master mode(1)**



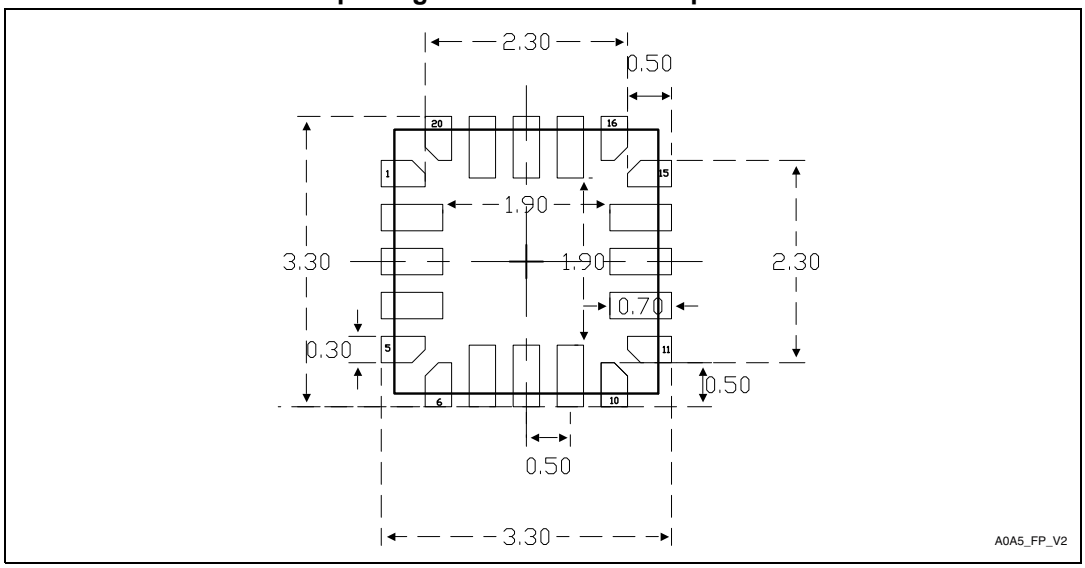

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 70. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| A3 | - | 0.152 | - | - | 0.060 | - |
| D | - | 3.000 | - | - | 0.1181 | - |
| E | - | 3.000 | - | - | 0.1181 | - |
| L1 | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| L2 | 0.300 | 0.350 | 0.400 | 0.0118 | 0.0138 | 0.0157 |
| L3 | - | 0.375 | - | - | 0.0148 | - |
| L4 | - | 0.200 | - | - | 0.0079 | - |
| L5 | - | 0.150 | - | - | 0.0059 | - |
| b | 0.180 | 0.250 | 0.300 | 0.0071 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 41. UFQFPN20 - 20-lead, 3x3 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

# 9 Revision history

**Table 75. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-Dec-2015 | 1 | Initial release. |
| 11-Feb-2016 | 2 | *Features*: modified current consumption in run mode, Cortex®-M0+ core frequency range and total number of timers.<br>Updated ADC conversion consumption on cover page.<br>Updated ADC conversion consumption on cover page.<br>Updated UFQFPN28 pinout: *Figure 5: STM32L021x4 UFQFPN28 pinout* and *Table 12: Pin definitions*.<br>Updated *Table 54: RAIN max for fADC = 16 MHz*.<br>Modified TS_CAL2 description in *Table 56: Temperature sensor calibration values*.<br>Added *Section : UFQFPN20 device marking*, *Section : TSSOP14 device marking* and *Section : UFQFPN28 device marking*. |
| 17-Mar-2016 | 3 | Changed minimum comparator supply voltage to 1.65 V on cover page.<br>Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.16.3: Low-power universal asynchronous receiver transmitter (LPUART)*.<br>Added number of fast and standard channels in *Section 3.10: Analog-to-digital converter (ADC)*.<br>Updated *Table 15: Current characteristics* to add the total output current for STM32L021GxUx.<br>Changed $V_{DDA}$ minimum value to 1.65 V in *Table 17: General operating conditions*.<br>Updated *Table 25: Current consumption in Sleep mode*, *Table 26: Current consumption in Low-power Run mode*, *Table 27: Current consumption in Low-power Sleep mode* and *Table 29: Typical and maximum current consumptions in Standby mode*.<br>*Section 6.3.15: 12-bit ADC characteristics*:<br>– *Table 53: ADC characteristics*:<br>Distinction made between $V_{DDA}$ for fast and standard channels; added note *1.*<br>Updated condition for $f_{TRIG}$ measurement.<br>Added note *4.* related to $R_{ADC}$ and removed measurement condition.<br>Updated $t_S$ and $t_{CONV}$.<br>– Updated equation 1 description.<br>– Updated *Table 54: RAIN max for fADC = 16 MHz* for $f_{ADC}$ = 16 MHz and distinction made between fast and standard channels.<br>– Updated measurement condition in *Table 55: ADC accuracy*.<br>Added *Table 63: USART/LPUART characteristics*. |