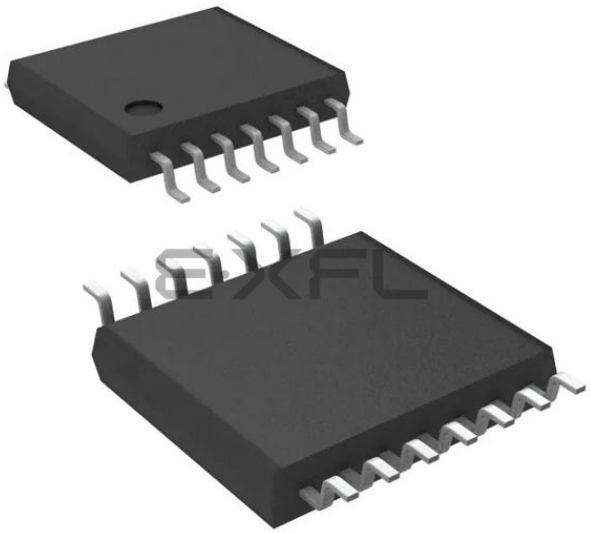

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l021d4p7

Contents

2.1 Device overview

Table 1. Ultra-low-power STM32L021x4 device features and peripheral counts

Peripheral		STM32 L021D4	STM32 L021F4	STM32 L021G4	STM32L021K4
Flash (Kbytes)		16			
Data EEPROM (bytes)		512			
RAM (Kbytes)		2			
AES		1			
Timers	General-purpose	2			
	LPTIM	1			
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1			
Communication interfaces	SPI	1			
	I^2C	1			
	USART	1			
	LPUART	1			
GPIOs		11	16	24	26/28(1)
Clocks: HSE(2)/LSE/HSI/MSI/LSI		1/1/1/1/1			
12-bit synchronized ADC Number of channels		1 4	1 7/9(3)	1 10	
Comparators		2			
Max. CPU frequency		32 MHz			
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option			
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C			
Packages		TSSOP14	TSSOP20, UFQFPN20	UFQFPN28	LQFP32, UFQFPN32

1. The devices feature 26 and 28 GPIOs on LQFP32 and UFQFPN32, respectively.
2. HSE available only as external clock input (HSE bypass).
3. The devices feature 7 and 9 ADC channels on UFQFPN20 and TSSOP20, respectively.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L021x4 supports dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

- **Stop mode with RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event

Table 4. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Wakeup time to Run mode	0 µs	6 CPU cycles	3 µs	7 CPU cycles	5 µs	65 µs
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 128 µA/MHz (from Flash)	Down to 31 µA/MHz (from Flash)	Down to 7 µA	Down to 3.8 µA	0.29 µA (No RTC) V_{DD}=1.8 V	0.18 µA (No RTC) V_{DD}=1.8 V
					0.54 µA (with RTC) V_{DD}=1.8 V	0.41 µA (with RTC) V_{DD}=1.8 V
					0.34 µA (No RTC) V_{DD}=3.0 V	0.23 µA (No RTC) V_{DD}=3.0 V
					0.67 µA (with RTC) V_{DD}=3.0 V	0.53 µA (with RTC) V_{DD}=3.0 V

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional, can be enabled/disabled by software)
   "-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start.To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 5. STM32L021x4 peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM1	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nBOOT_SEL option bits are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA7, PA13 and PA14 on TSSOP14 package or PA4, PA5, PA6 and PA7 on other packages) or USART2 (PA2, PA3 and PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.16.4 Serial peripheral interface (SPI)

The SPI is able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI can be served by the DMA controller.

Refer to *Table 10* for the supported modes and features of SPI interface.

Table 10. SPI implementation

SPI features(1)	SPI1
Hardware CRC calculation	X
I2S mode	-
TI mode	X

1. X = supported.

3.17 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

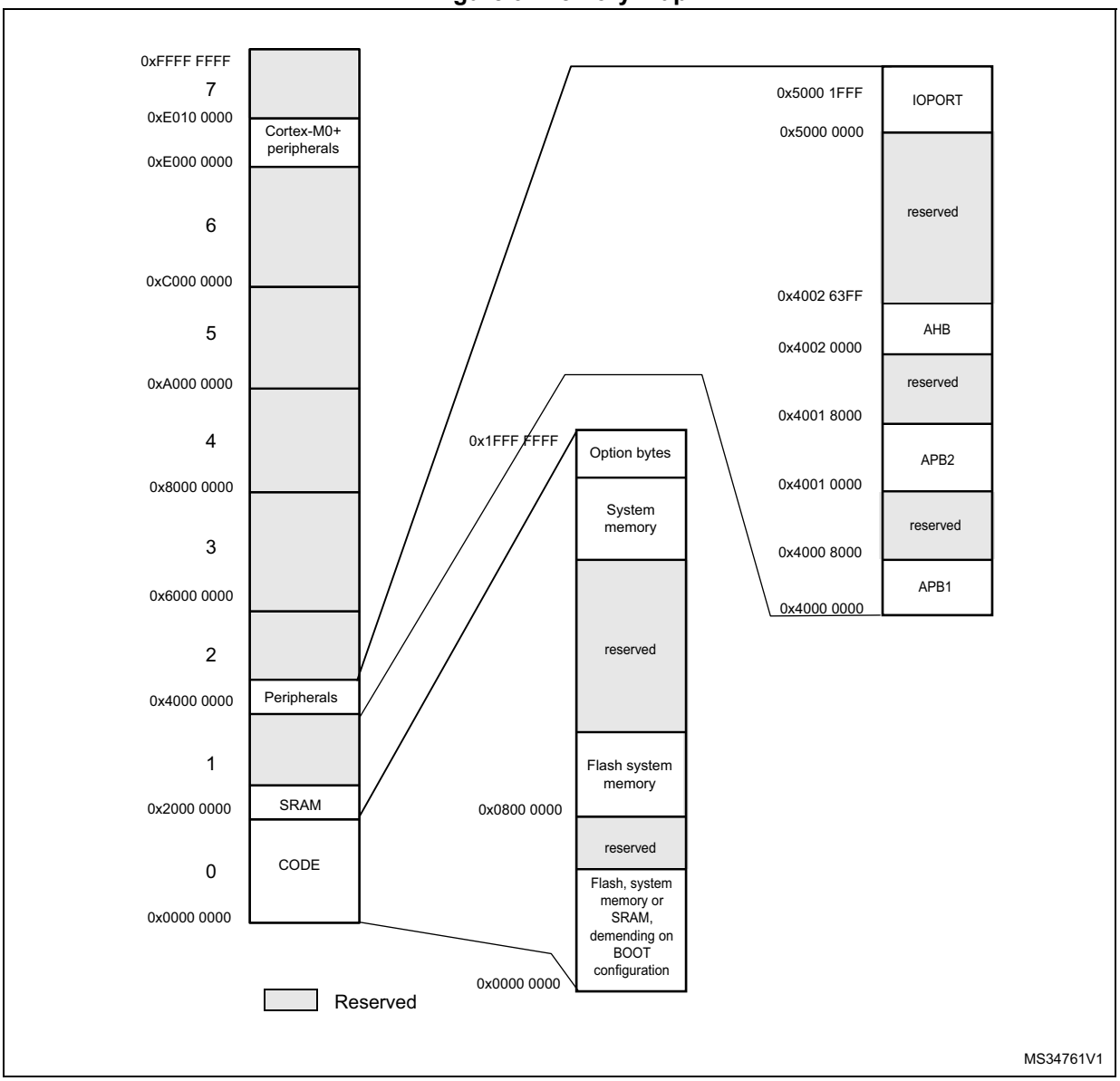
Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.18 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

5 Memory mapping

Figure 9. Memory map



1. Refer to the STM32L021x4 reference manual for details on the Flash memory organization for each memory size.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

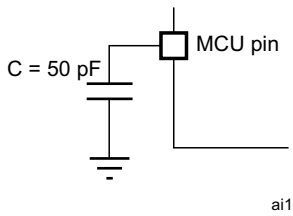
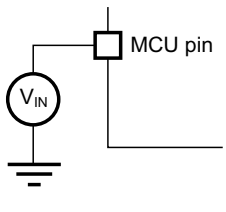
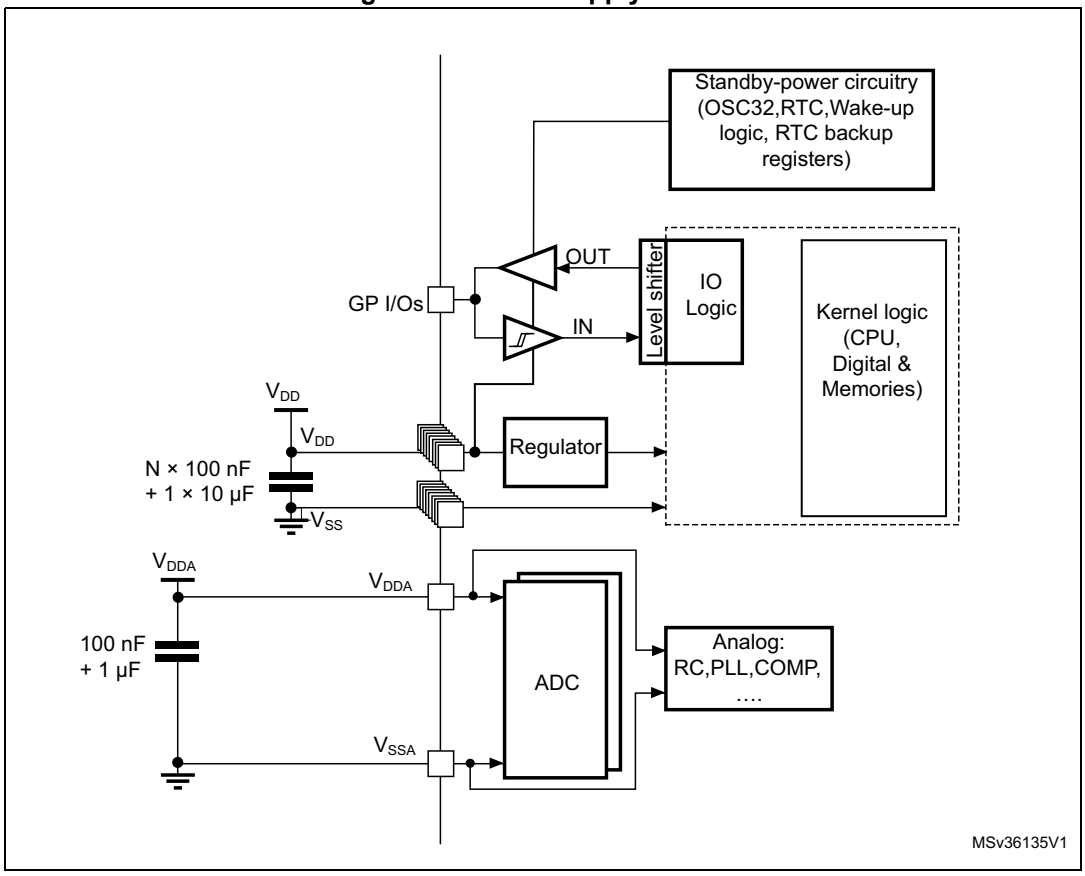


Figure 11. Pin input voltage



6.1.6 Power supply scheme

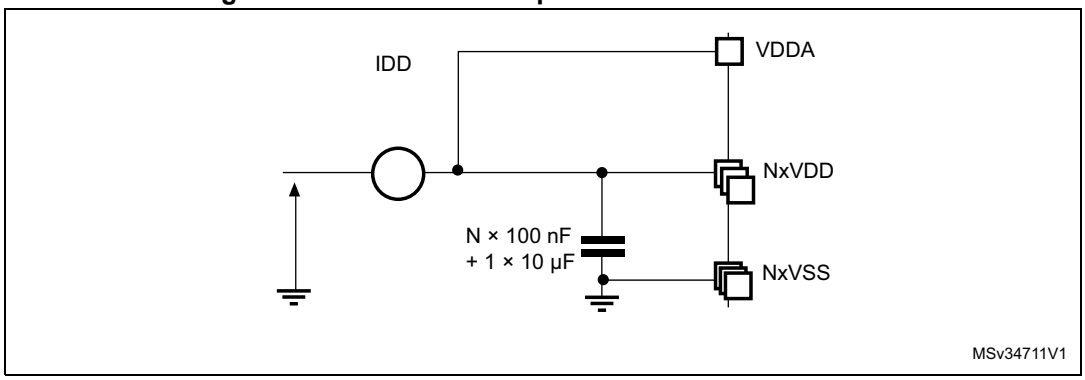
Figure 12. Power supply scheme



1. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
2. V_{SSA} is internally connected to V_{SS} on all packages.

6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme



6.3.3 Embedded internal reference voltage

The parameters given in *Table 20* are based on characterization results, unless otherwise specified.

Table 19. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25°C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 20. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$(2)	Internal reference voltage	– 40 °C < T_J < +125 °C	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	–40 °C < T_J < +125 °C	-	25	100	ppm/°C
		0 °C < T_J < +50 °C	-	-	20	
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(4)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(4)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(4)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(4)	3/4 reference voltage	-	74	75	76	

1. Refer to *Table 32: Peripheral current consumption in Stop and Standby mode* for the value of the internal reference current consumption (I_{REFINT}).
2. Guaranteed by test in production.
3. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.

Figure 14. I_{DD} vs V_{DD}, at T_A= 25 °C, Run mode, code running from Flash memory, Range 2, 16 MHz HSE, 1WS

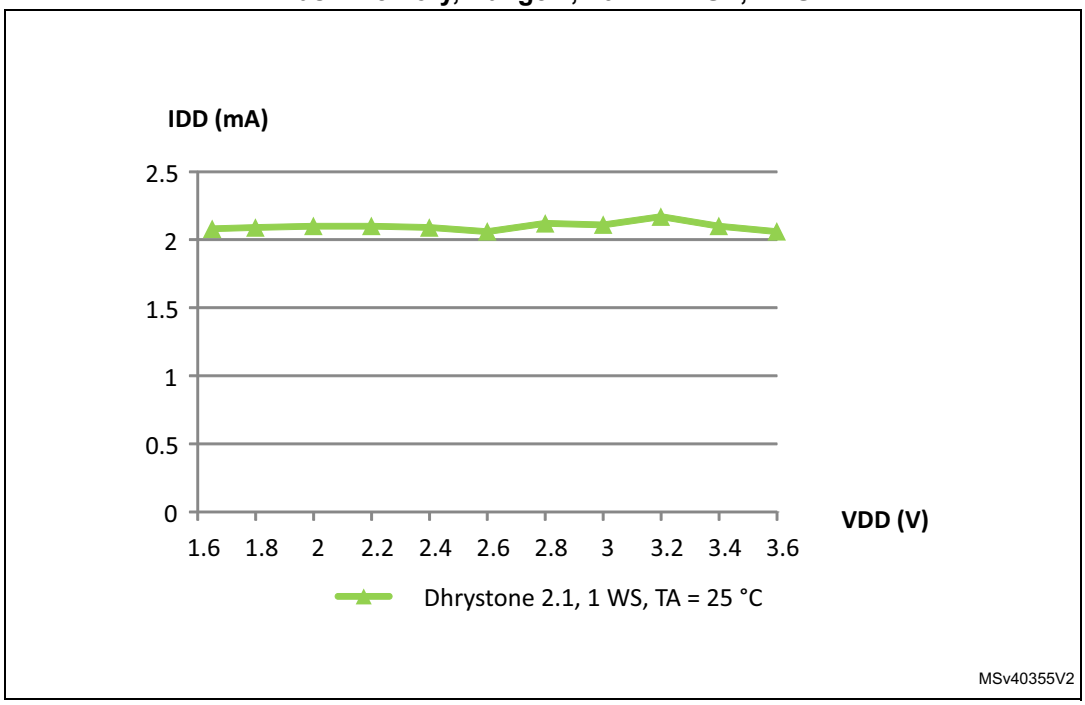


Figure 15. I_{DD} vs V_{DD}, at T_A= 25 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS

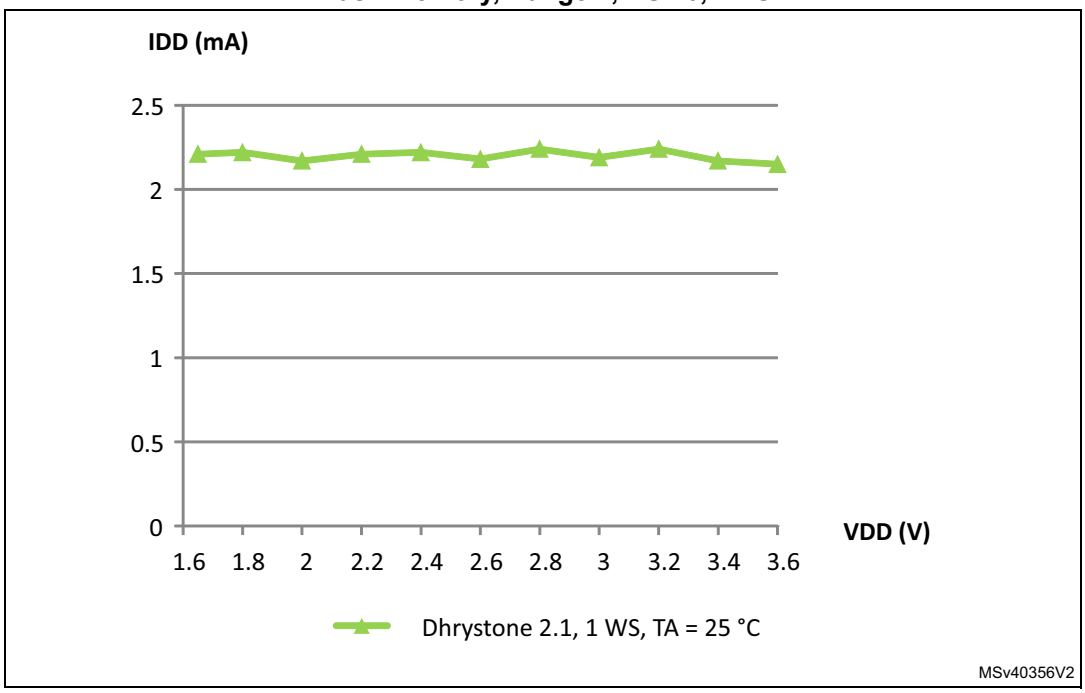


Table 28. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = -40°C to 25°C	0.34	0.99	µA
		T_A = 55°C	0.43	1.9	
		T_A= 85°C	0.94	4.2	
		T_A = 105°C	2.0	9	
		T_A = 125°C	4.9	19	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

Figure 17. I_{DD} vs V_{DD}, at T_A= -40/25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

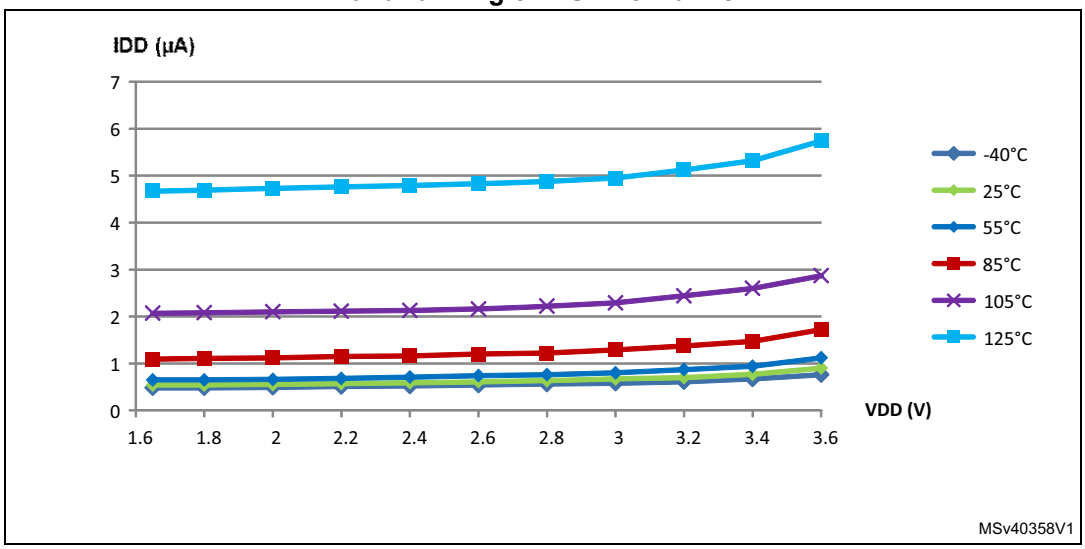


Figure 18. I_{DD} vs V_{DD}, at T_A= -40/25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF

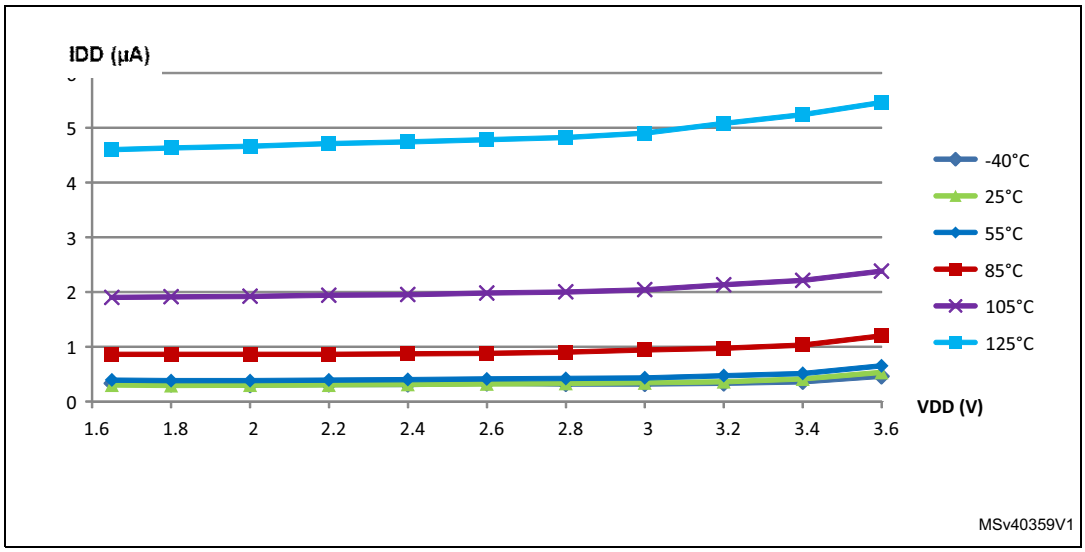


Table 31. Peripheral current consumption in run or Sleep mode(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	WWDG	2.5	2	1.6	2	µA/MHz (f_{HCLK})
	LPUART1	8.3	7.2	5.4	7.2	
	I2C1	11	8.2	6.8	8.9	
	LPTIM1	14	11	8.7	11	
	TIM2	10.5	8.5	6.4	8.5	
	USART2	8.5	6.8	5.4	7.1	
APB2	ADC1(2)	5.0	3.9	3.3	4	µA/MHz (f_{HCLK})
	SPI1	4.5	3.5	2.9	3.6	
	TIM21	6.8	6.1	4.5	5.6	
	DBGMCU	1.7	1.7	1.1	1.4	
	SYSCFG/ COMP	2.5	2.4	1.6	2.3	
Cortex-M0+ core I/O port	GPIOA	7.6	6.3	4.9	6.5	µA/MHz (f_{HCLK})
	GPIOB	5.1	4.1	3.2	4	
	GPIOC	1.1	0.7	0.6	0.8	
AHB	CRC	1.5	1.1	1	1.2	µA/MHz (f_{HCLK})
	FLASH(3)	10	8.5	7	8.5	
	AES	3.6	3.0	2.4	2.8	
	DMA1	5.3	4.2	3.5	4.8	
All enabled		96	80	62	88	
PWR		2.1	1.9	1.4	1.8	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. These values correspond to the Flash memory dynamic current consumption. The Flash memory static consumption (Flash memory ON) equals 12 µA and does not depend on the frequency.
The Flash memory consumption is already taken into account in all the supply current consumption tables (Flash memory ON cases).

time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

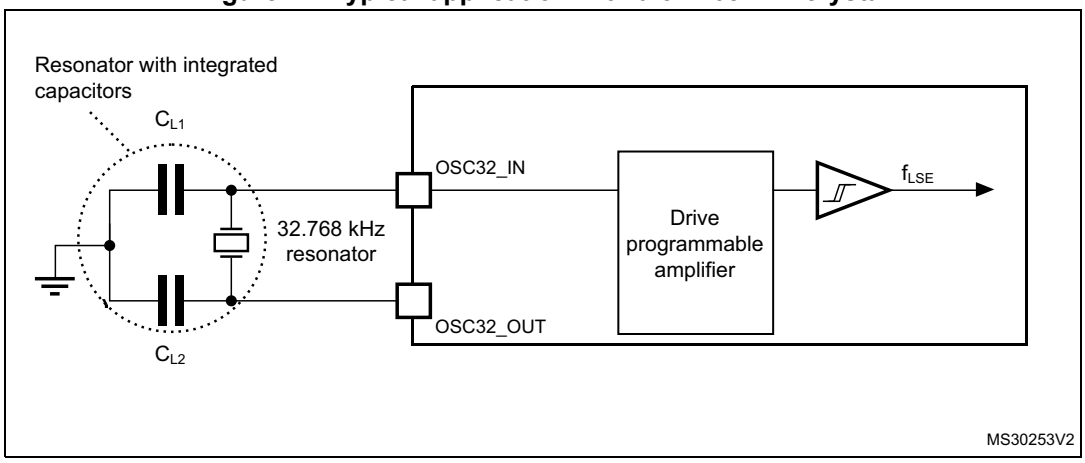
Table 36. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results, not tested in production. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website http://www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Table 47. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence oscillator frequency deviation).

The test results are given in the *Table 48*.

Table 48. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	-0	NA	mA
	Injected current on all FT pins	-5 (1)	NA	
	Injected current on any other pin	-5 (1)	+5	

1. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

6.3.17 Comparators

Table 58. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
V_{offset}	Comparator offset(3)	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions(3)	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(4)	-	-	160	260	nA

1. Guaranteed by characterization, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the comparator performance.
4. Comparator consumption only. Internal reference voltage not included.

Table 59. Comparator 2 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65	-	3.6	V
V_{IN}	Comparator 2 input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	Fast mode	-	15	20	µs
		Slow mode	-	20	25	
$t_{d\ slow}$	Propagation delay(2) in slow mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	1.8	3.5	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	2.5	6	
$t_{d\ fast}$	Propagation delay(2) in fast mode	1.65 V ≤ V_{DDA} ≤ 2.7 V	-	0.8	2	
		2.7 V ≤ V_{DDA} ≤ 3.6 V	-	1.2	4	
V_{offset}	Comparator offset error(3)		-	±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient	V_{DDA} = 3.3V T_A = 0 to 50 °C V- = V_{REFINT}, 3/4 V_{REFINT}, 1/2 V_{REFINT}, 1/4 V_{REFINT}.	-	15	30	ppm /°C

Table 59. Comparator 2 characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
I_{COMP2}	Current consumption(4)	Fast mode	-	3.5	5	µA
		Slow mode	-	0.5	2	

1. Guaranteed by characterization results, not tested in production.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. In TSSOP14 package, where V_{DDA} pin is shared with V_{DD} pin, I/O toggling should be minimized to reach the values given in the above table. I/O toggling with loaded I/O pins can generate ripple on V_{DD}/V_{DDA} and degrade the comparator performance.
4. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

6.3.18 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 60* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 60. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2 and TIM21 timers.

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 63. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	µs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

8 Part numbering

Table 74. STM32L021x4 ordering information scheme

Example: STM32 L 021 K 4 T 6 D xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

L = Low power

Device subfamily

021 = Access line with AES

Pin count

K = 32 pins

G = 28 pins

F = 20 pins

D = 14 pins

Flash memory size

4 = 16 Kbytes

Package

T = LQFP

U = UFQFPN

P = TSSOP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

3 = Industrial temperature range, –40 to 125 °C

Options

No character = V_{DD} range: 1.8 to 3.6 V and BOR enabled

D = V_{DD} range: 1.65 to 3.6 V and BOR disabled

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.