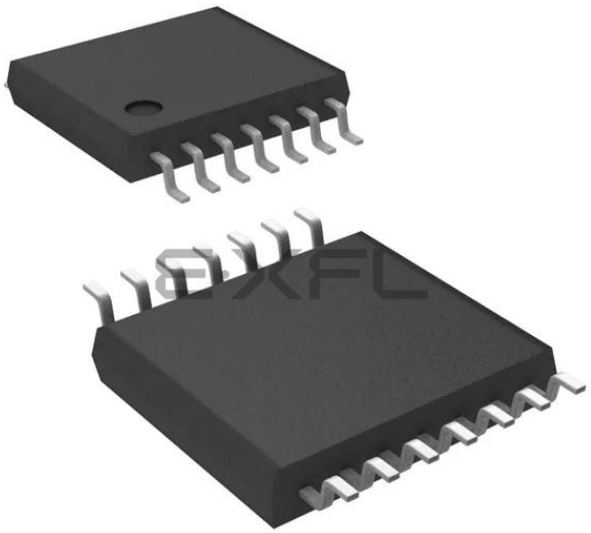

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l021d4p7tr

Contents

2.1 Device overview

Table 1. Ultra-low-power STM32L021x4 device features and peripheral counts

Peripheral		STM32 L021D4	STM32 L021F4	STM32 L021G4	STM32L021K4
Flash (Kbytes)		16			
Data EEPROM (bytes)		512			
RAM (Kbytes)		2			
AES		1			
Timers	General-purpose	2			
	LPTIM	1			
RTC/SYSTICK/IWDG/ WWDG		1/1/1/1			
Communication interfaces	SPI	1			
	I^2C	1			
	USART	1			
	LPUART	1			
GPIOs		11	16	24	26/28(1)
Clocks: HSE(2)/LSE/HSI/MSI/LSI		1/1/1/1/1			
12-bit synchronized ADC Number of channels		1 4	1 7/9(3)	1 10	
Comparators		2			
Max. CPU frequency		32 MHz			
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option			
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C			
Packages		TSSOP14	TSSOP20, UFQFPN20	UFQFPN28	LQFP32, UFQFPN32

1. The devices feature 26 and 28 GPIOs on LQFP32 and UFQFPN32, respectively.
2. HSE available only as external clock input (HSE bypass).
3. The devices feature 7 and 9 ADC channels on UFQFPN20 and TSSOP20, respectively.

Table 4. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)(2)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop	Standby
					Wakeup capability	Wakeup capability
Wakeup time to Run mode	0 µs	6 CPU cycles	3 µs	7 CPU cycles	5 µs	65 µs
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 128 µA/MHz (from Flash)	Down to 31 µA/MHz (from Flash)	Down to 7 µA	Down to 3.8 µA	0.29 µA (No RTC) V_{DD}=1.8 V	0.18 µA (No RTC) V_{DD}=1.8 V
					0.54 µA (with RTC) V_{DD}=1.8 V	0.41 µA (with RTC) V_{DD}=1.8 V
					0.34 µA (No RTC) V_{DD}=3.0 V	0.23 µA (No RTC) V_{DD}=3.0 V
					0.67 µA (with RTC) V_{DD}=3.0 V	0.53 µA (with RTC) V_{DD}=3.0 V

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional, can be enabled/disabled by software)
   "-" = Not available
2. The consumption values given in this table are preliminary data given for indication. They are subject to slight changes.
3. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.
4. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start.To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.
5. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 5. STM32L021x4 peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM1	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y

Table 5. STM32L021x4 peripherals interconnect matrix (continued)

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM1	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM1	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC	Conversion trigger	Y	Y	Y	Y	-

3.3 ARM® Cortex®-M0+ core

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

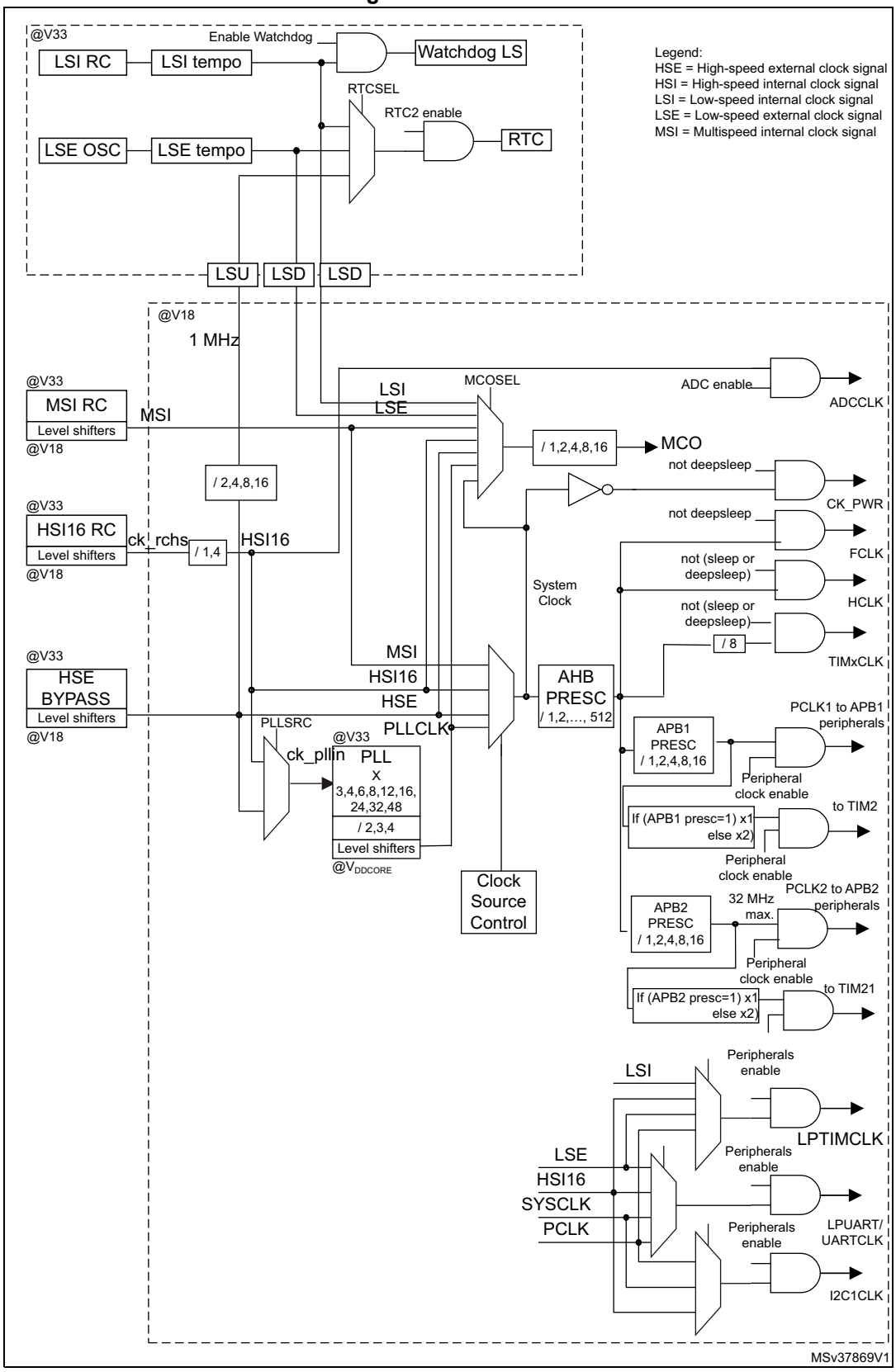
- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L021x4 are compatible with all ARM tools and software.

Figure 2. Clock tree



3.10 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L021x4 devices. It has up to 10 external channels and 2 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.11 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

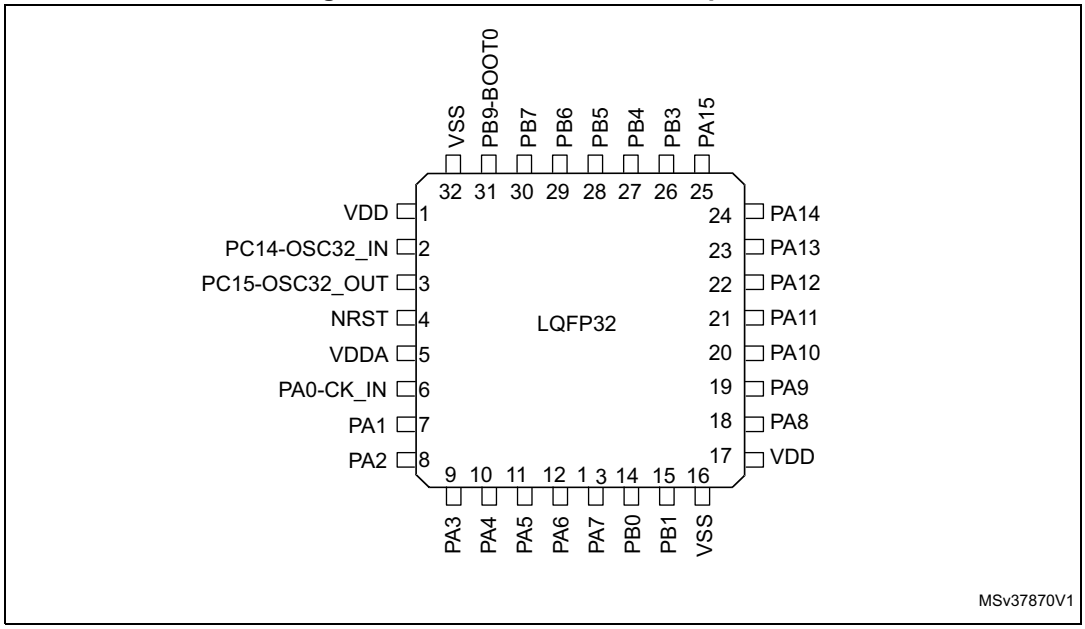
To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode (see *Table 56: Temperature sensor calibration values*).

3.11.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (since no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area (see *Table 19: Embedded internal reference voltage calibration values*). It is accessible in read-only mode.

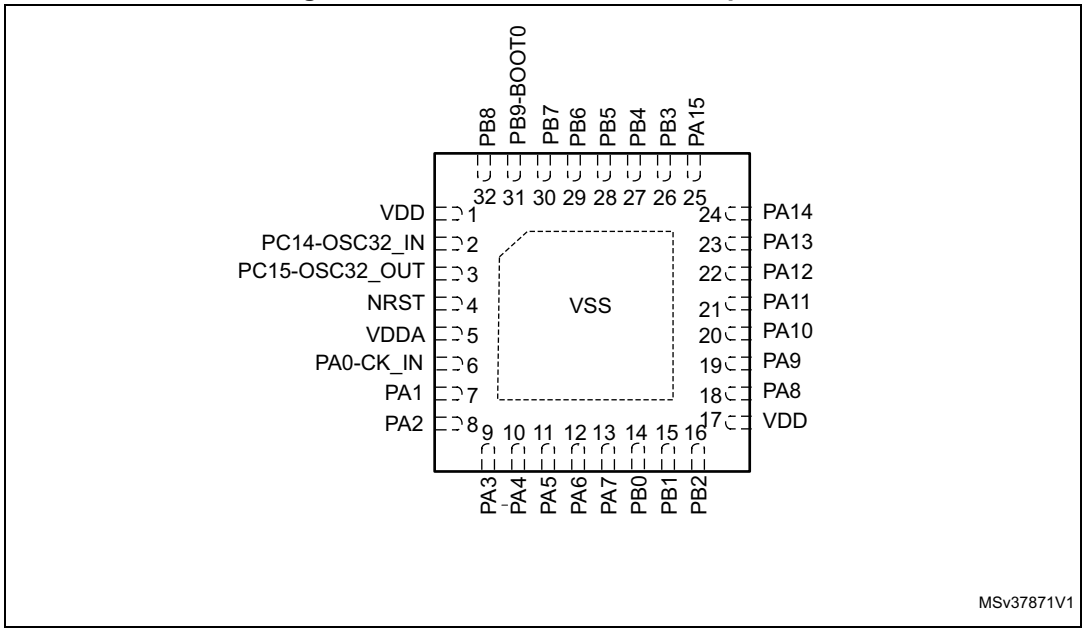
4 Pin descriptions

Figure 3. STM32L021x4 LQFP32 pinout



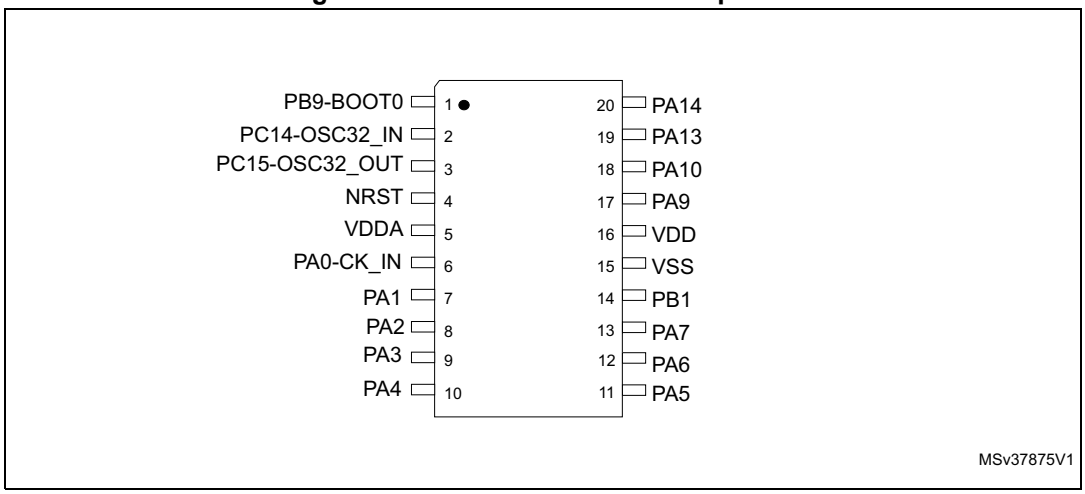
1. The above figure shows the package top view.

Figure 4. STM32L021x4 UFQFPN32 pinout



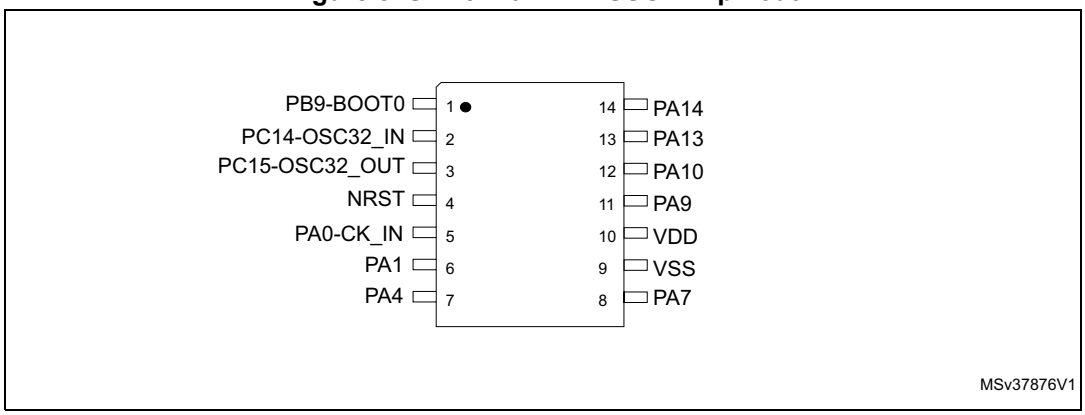
1. The above figure shows the package top view.

Figure 7. STM32L021x4 TSSOP20 pinout



1. The above figure shows the package top view.

Figure 8. STM32L021x4 TSSOP14 pinout



1. The above figure shows the package top view.

Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TTa	3.3 V tolerant I/O directly connected to the ADC
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor

Table 12. Pin definitions (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]					Alternate functions	Additional functions
-	-	9	9	9	9	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, USART2_RX, LPUART1_RX	COMP2_INP, ADC_IN3
7	7	10	10	10	10	PA4	I/O	TTa	-	SPI1_NSS, LPTIM1_IN1, LPTIM1_ETR, I2C1_SCL, USART2_CK, TIM2_ETR, LPUART1_TX, COMP2_OUT	COMP1_INM, COMP2_INM, ADC_IN4
-	8	11	11	11	11	PA5	I/O	TTa	-	SPI1_SCK, LPTIM1_IN2, TIM2_ETR, TIM2_CH1	COMP1_INM, COMP2_INM, ADC_IN5
-	9	12	12	12	12	PA6	I/O	FT	-	SPI1_MISO, LPTIM1_ETR, LPUART1_CTS, EVENTOUT, COMP1_OUT	ADC_IN6
8	10	13	13	13	13	PA7	I/O	FT	-	SPI1_MOSI, LPTIM1_OUT, USART2_CTS, TIM21_ETR, EVENTOUT, COMP2_OUT	COMP2_INP, ADC_IN7
-	-	-	14	14	14	PB0	I/O	FT	-	EVENTOUT, SPI1_MISO, TIM2_CH2, USART2_RTS, TIM2_CH3	ADC_IN8, VREF_OUT
-	11	14	15	15	15	PB1	I/O	FT	-	USART2_CK, SPI1_MOSI, LPTIM1_IN1, LPUART1_RTS, TIM2_CH4	ADC_IN9, VREF_OUT
-	-	-	-	-	16	PB2	I/O	FT	-	LPTIM1_OUT	-

Table 12. Pin definitions (continued)

Pin number						Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
TSSOP14	UFQFPN20	TSSOP20	UFQFPN28	LQFP32	UFQFPN32[1]					Alternate functions	Additional functions
-	-	-	-	32	-	VSS	S		(4)	-	-
-	-	-	-	1	1	VDD	S	-	(5)	-	-

1. VSS pins are connected to the exposed pad (see *Figure 35: UFQFPN32, 5 x 5 mm, 32-pin package outline*).
2. Device reset input/internal reset output (active low).
3. Analog power supply.
4. On TSSOP14 package, V_{DDA} is internally connected to V_{DD}.
5. Digital and analog ground.
6. Digital power supply.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

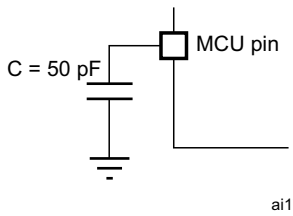
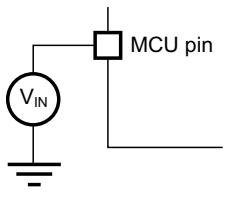


Figure 11. Pin input voltage



6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

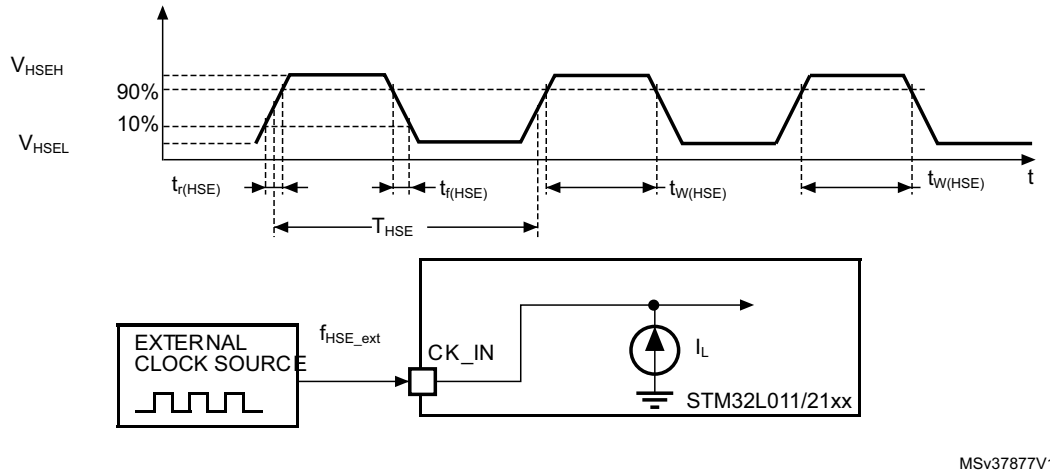
In bypass mode the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 19*.

Table 34. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is ON or PLL is used	1	8	32	MHz
		CSS is OFF, PLL not used	0	8	32	MHz
V_{HSEH}	CK_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	CK_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	CK_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	CK_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	CK_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	CK_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 19. High-speed external clock source AC timing diagram



time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

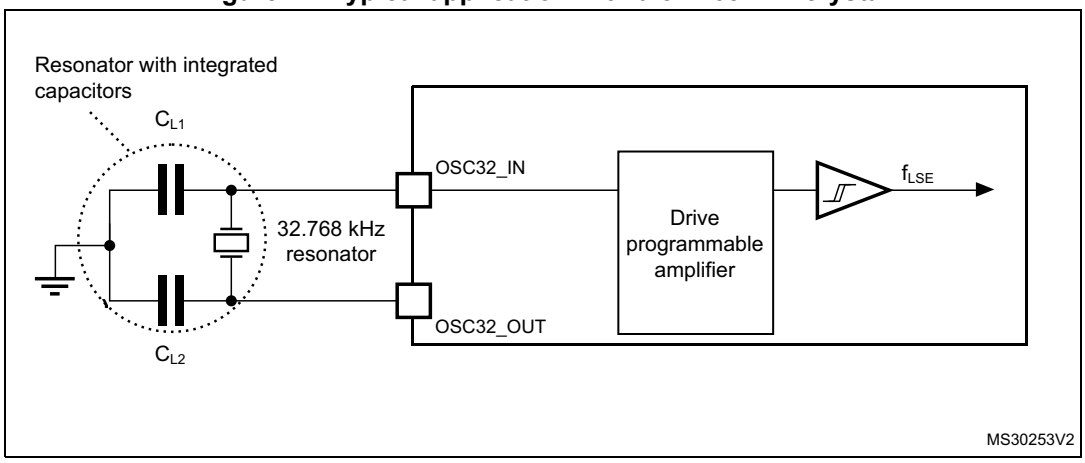
Table 36. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results, not tested in production. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

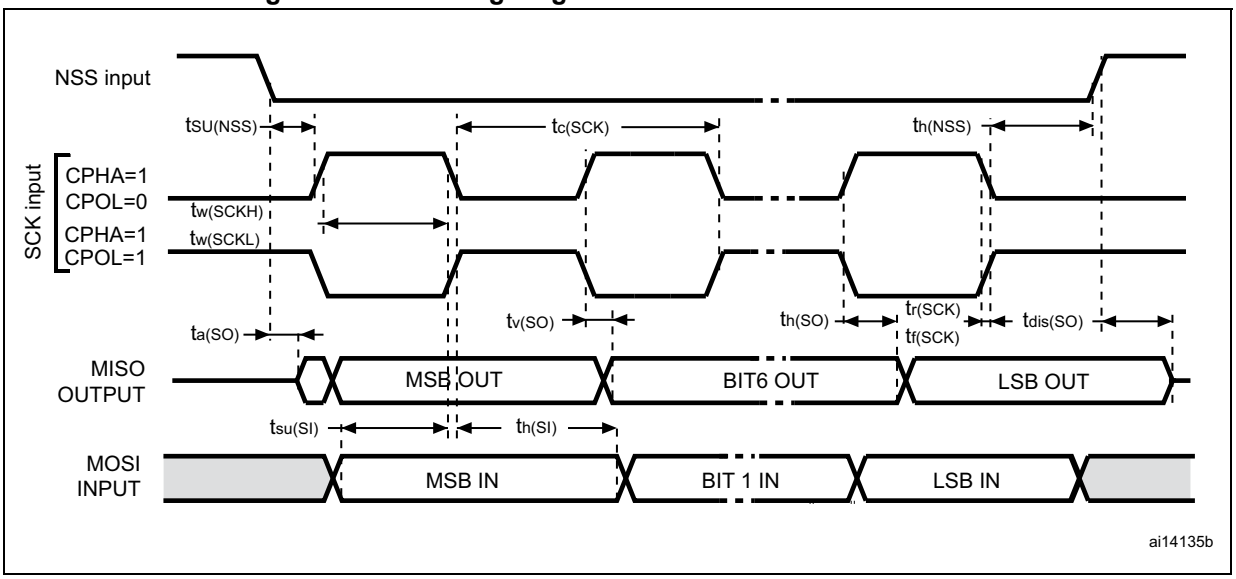
Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website http://www.st.com.

Figure 21. Typical application with a 32.768 kHz crystal



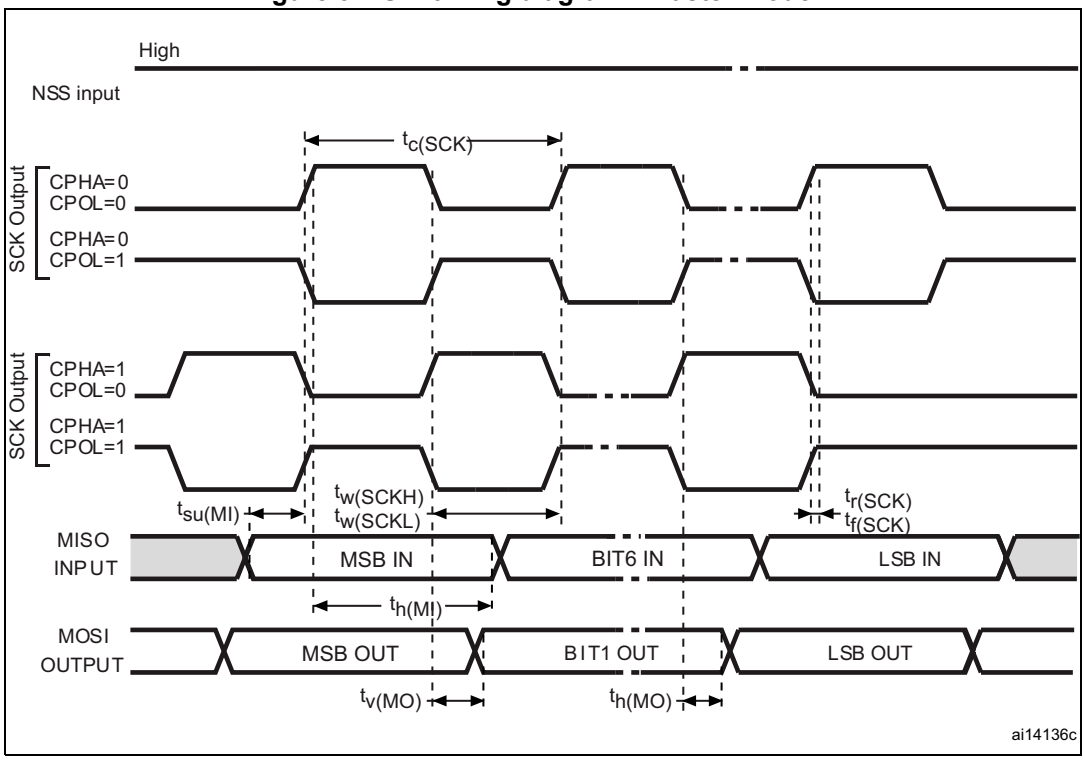
Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Figure 30. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 31. SPI timing diagram - master mode(1)

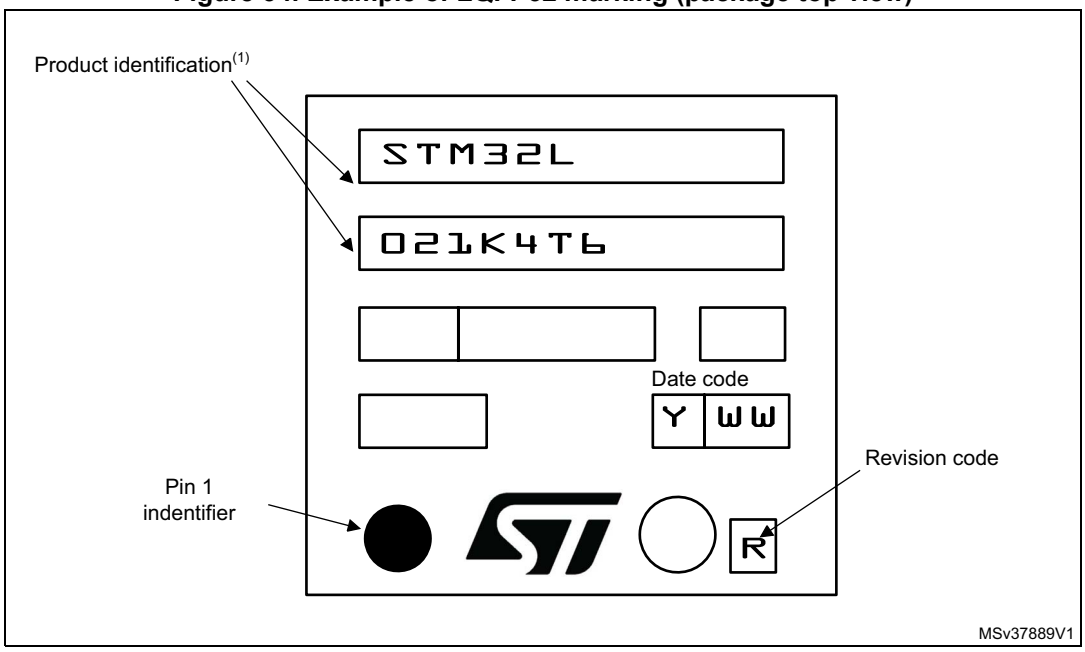


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

LQFP32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

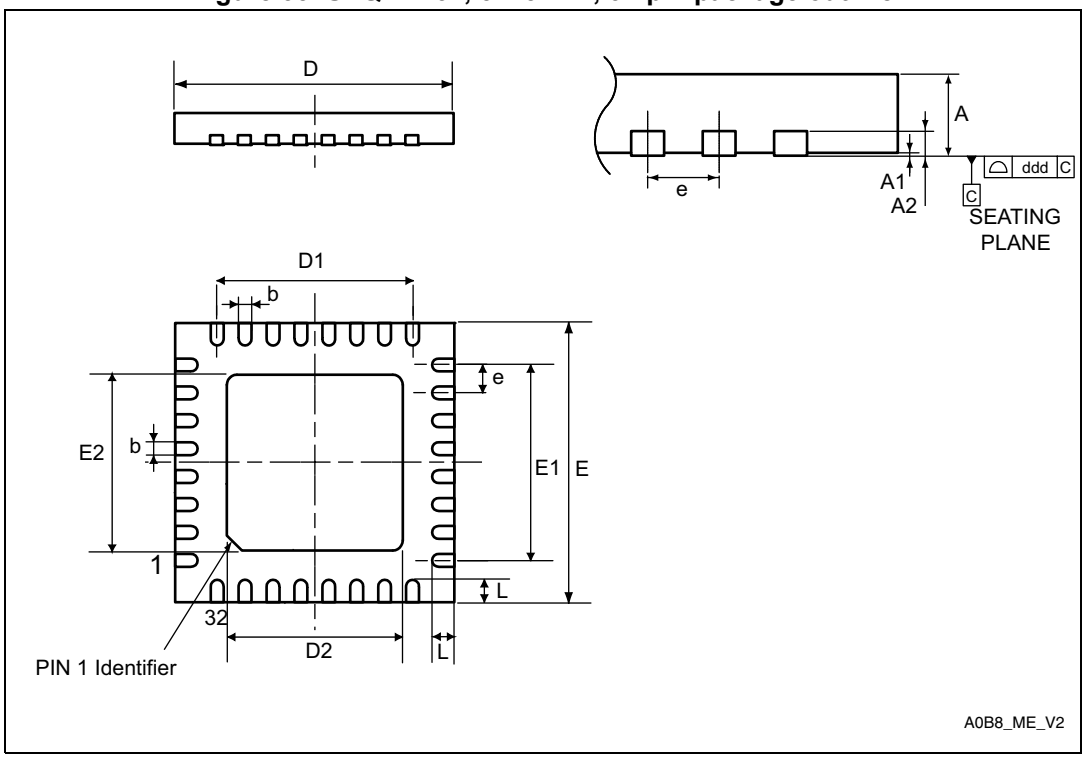
Figure 34. Example of LQFP32 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.2 UFQFPN32 package information

Figure 35. UFQFPN32, 5 x 5 mm, 32-pin package outline



1. Drawing is not to scale.

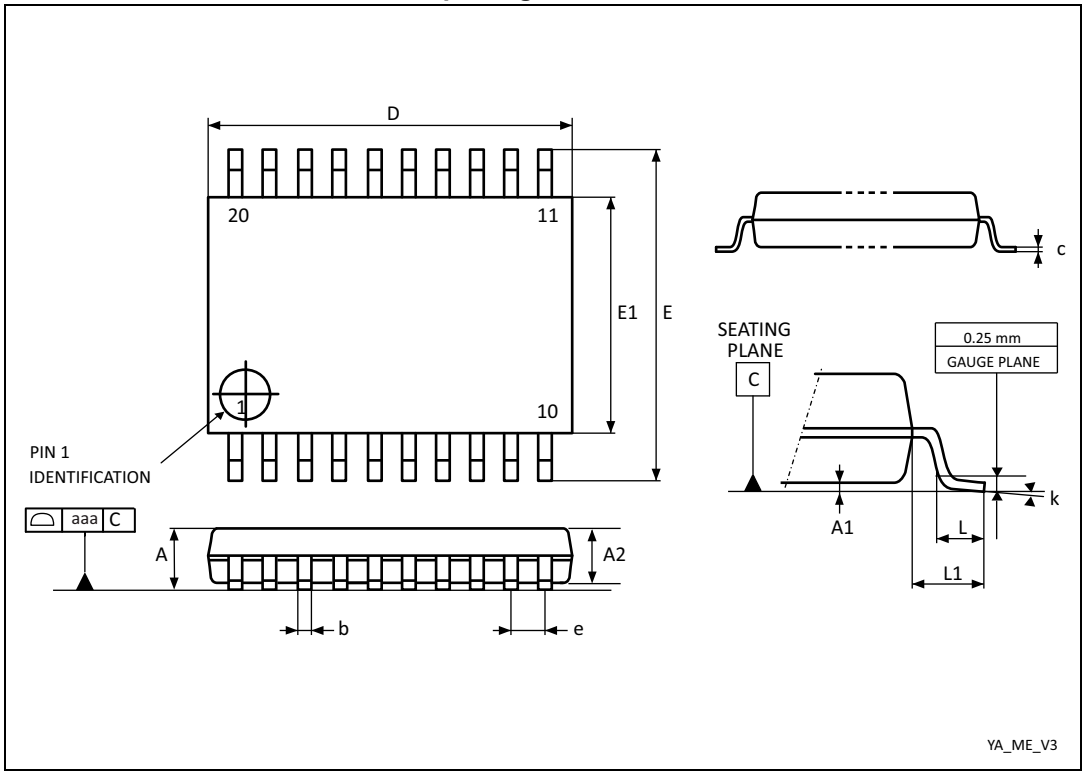
Table 68. UFQFPN32, 5 x 5 mm, 32-pin package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D2	3.200	3.450	3.700	0.1260	0.1358	0.1457
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E2	3.200	3.450	3.700	0.1260	0.1358	0.1457
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.5 TSSOP20 package information

Figure 43.TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

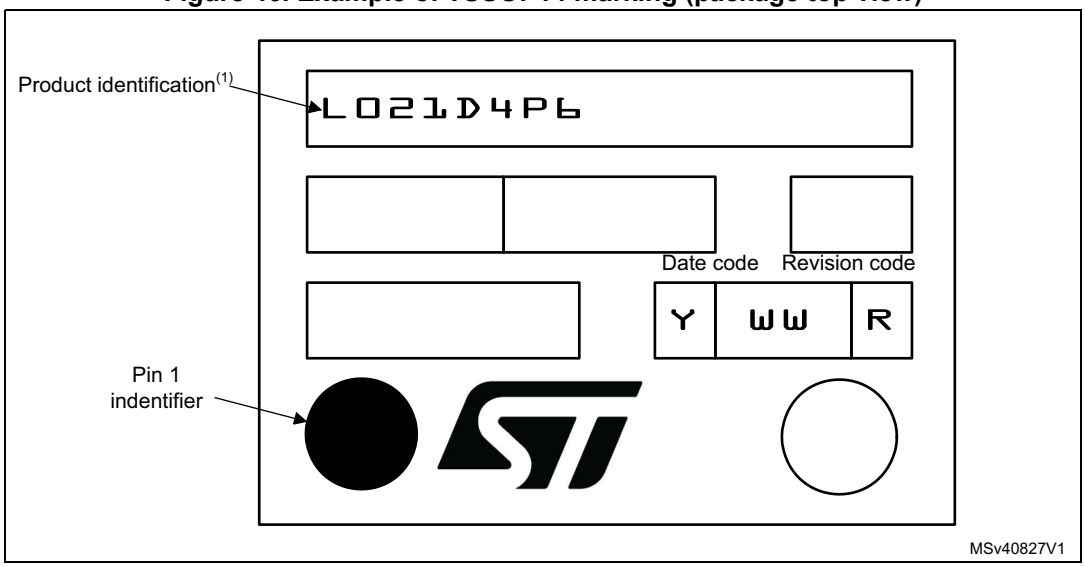
Table 71. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

TSSOP14 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 46. Example of TSSOP14 marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.7 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

9 Revision history

Table 75. Document revision history

Date	Revision	Changes
07-Dec-2015	1	Initial release.
11-Feb-2016	2	*Features*: modified current consumption in run mode, Cortex®-M0+ core frequency range and total number of timers. Updated ADC conversion consumption on cover page. Updated ADC conversion consumption on cover page. Updated UFQFPN28 pinout: *Figure 5: STM32L021x4 UFQFPN28 pinout* and *Table 12: Pin definitions*. Updated *Table 54: RAIN max for fADC = 16 MHz*. Modified TS_CAL2 description in *Table 56: Temperature sensor calibration values*. Added *Section : UFQFPN20 device marking*, *Section : TSSOP14 device marking* and *Section : UFQFPN28 device marking*.
17-Mar-2016	3	Changed minimum comparator supply voltage to 1.65 V on cover page. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.16.3: Low-power universal asynchronous receiver transmitter (LPUART)*. Added number of fast and standard channels in *Section 3.10: Analog-to-digital converter (ADC)*. Updated *Table 15: Current characteristics* to add the total output current for STM32L021GxUx. Changed V_{DDA} minimum value to 1.65 V in *Table 17: General operating conditions*. Updated *Table 25: Current consumption in Sleep mode*, *Table 26: Current consumption in Low-power Run mode*, *Table 27: Current consumption in Low-power Sleep mode* and *Table 29: Typical and maximum current consumptions in Standby mode*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 53: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note *1.* Updated condition for f_{TRIG} measurement. Added note *4.* related to R_{ADC} and removed measurement condition. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated *Table 54: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. – Updated measurement condition in *Table 55: ADC accuracy*. Added *Table 63: USART/LPUART characteristics*.