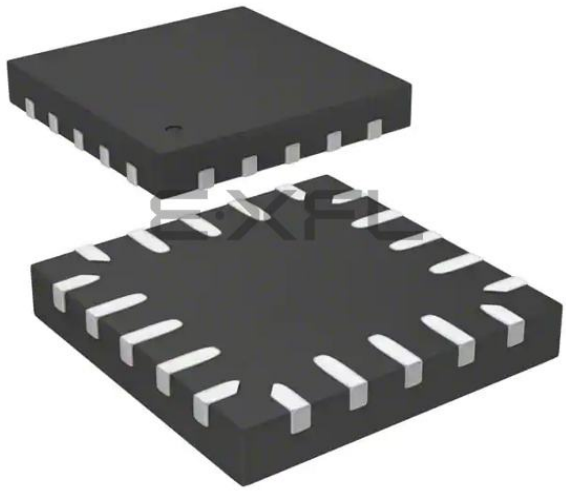

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l021f4u6tr

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 Ultra-low-power series are the best solution for applications such as gas/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power Run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.4.3 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in Run mode (nominal regulation)
- LPR is used in the Low-power run, Low-power sleep and Stop modes
- Power down is used in Standby mode. The regulator output is high impedance, the kernel circuitry is powered down, inducing zero consumption but the contents of the registers and RAM are lost except for the standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE crystal 32 KHz oscillator, RCC_CSR).

3.4.4 Boot modes

At startup, BOOT0 pin and nBOOT0, nBOOT1 and nBOOT_SEL option bits are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1 (PA4, PA7, PA13 and PA14 on TSSOP14 package or PA4, PA5, PA6 and PA7 on other packages) or USART2 (PA2, PA3 and PA9, PA10). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.12 Ultra-low-power comparators and reference voltage

The STM32L021x4 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.13 System configuration controller

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM21 and LPTIM1 timer input captures. It also controls the routing of internal analog signals to the ADC, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

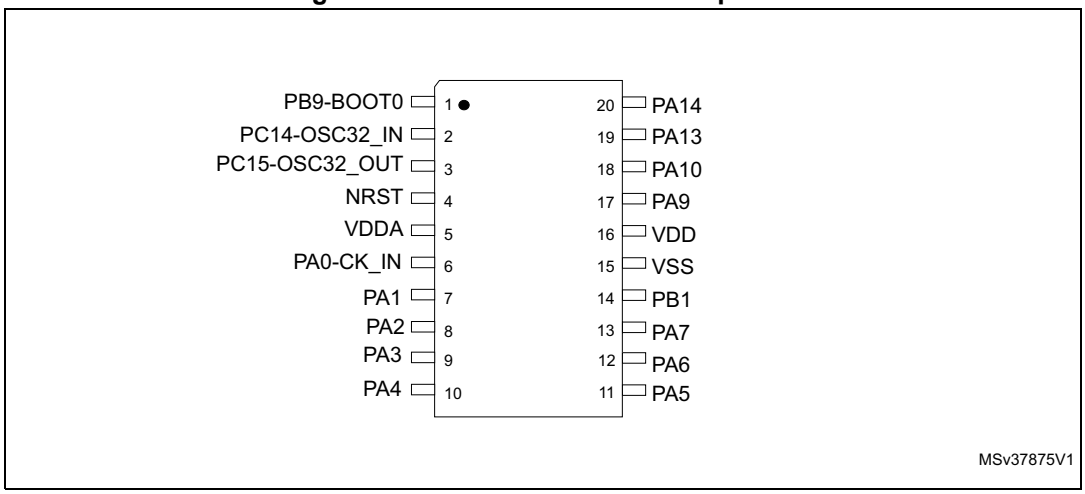
3.14 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES algorithm (compatible with FIPS PUB 197, 2001 Nov 26):

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

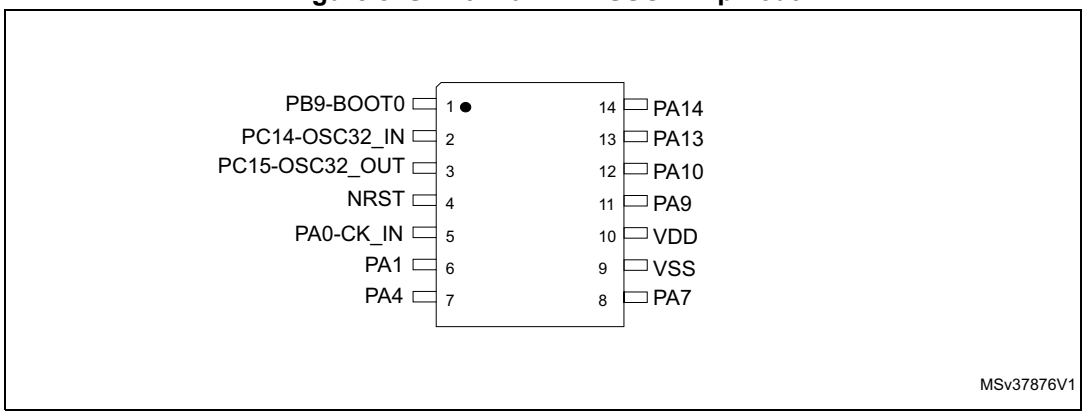
The AES can be served by the DMA controller.

Figure 7. STM32L021x4 TSSOP20 pinout



1. The above figure shows the package top view.

Figure 8. STM32L021x4 TSSOP14 pinout



1. The above figure shows the package top view.

Table 11. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TTa	3.3 V tolerant I/O directly connected to the ADC
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 10*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 11*.

Figure 10. Pin loading conditions

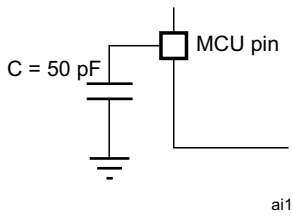
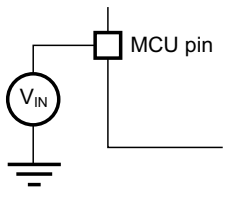


Figure 11. Pin input voltage



6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}	Analog operating voltage (all features)	Must be the same voltage as V_{DD}(1)	1.65	3.6	V
V_{IN}	Input voltage on FT, FTf and RST pins(2)	2.0 V ≤ V_{DD} ≤3.6 V	-0.3	5.5	V
		1.65 V ≤ V_{DD} ≤2.0 V	-0.3	5.2	
	Input voltage on BOOT0 pin	-	0	5.5	
	Input voltage on TC pin	-	-0.3	V_{DD}+0.3	
P_D	Power dissipation at T_A = 85 °C (range 6) or T_A =105 °C (rage 7) (3)	LQFP32 package	-	333	mW
		UFQFPN32 package	-	513	
		UFQFPN28 package	-	206	
		TSSOP20 package	-	270	
		UFQFPN20 package	-	196	
		TSSOP14 package	-	210	
	Power dissipation at T_A = 125 °C (range 3) (3)	LQFP32 package	-	83	
		UFQFPN32 package	-	128	
		UFQFPN28 package	-	52	
		TSSOP20 package	-	67	
		UFQFPN20 package	-	49	
		TSSOP14 package	-	53	

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Temperature range	Maximum power dissipation (range 6)	–40	85	°C
		Maximum power dissipation (range 7)	–40	105	
		Maximum power dissipation (range 3)	–40	125	
T_J	Junction temperature range (range 6)	-40 °C ≤ T_A ≤ 85 °	–40	105	
	Junction temperature range (range 7)	-40 °C ≤ T_A ≤ 105 °C	–40	125	
	Junction temperature range (range 3)	-40 °C ≤ T_A ≤ 125 °C	–40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 16: Thermal characteristics on page 47*).

6.3.2 Embedded reset and power control block characteristics

The parameters given in the following table are derived from the tests performed under the ambient temperature condition summarized in *Table 17*.

Table 18. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}(1)	V_{DD} rise time rate	BOR detector enabled	0	-	∞	µs/V
		BOR detector disabled	0	-	1000	
	V_{DD} fall time rate	BOR detector enabled	20	-	∞	
		BOR detector disabled	0	-	1000	
$T_{RSTTEMPO}$(1)	Reset temporization	V_{DD} rising, BOR enabled	-	2	3.3	ms
		V_{DD} rising, BOR disabled(2)	0.4	0.7	1.6	
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1	1.5	1.65	V
		Rising edge	1.3	1.5	1.65	
V_{BOR0}	Brown-out reset threshold 0	Falling edge	1.67	1.7	1.74	
		Rising edge	1.69	1.76	1.8	
V_{BOR1}	Brown-out reset threshold 1	Falling edge	1.87	1.93	1.97	
		Rising edge	1.96	2.03	2.07	
V_{BOR2}	Brown-out reset threshold 2	Falling edge	2.22	2.30	2.35	
		Rising edge	2.31	2.41	2.44	

Table 26. Current consumption in Low-power Run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	5.7	8.1	µA
				T_A = 85 °C	6.5	9	
				T_A = 105 °C	8	13	
				T_A = 125 °C	11.5	22	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	8.7	11	
				T_A = 85 °C	9.5	12	
				T_A = 105 °C	11	15	
				T_A = 125 °C	15	24	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	17	19	
				T_A = 55 °C	17	19.5	
				T_A = 85 °C	17.5	20	
				T_A = 105 °C	19	22	
				T_A = 125 °C	22.5	31	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	18	22	
				T_A = 85 °C	20	24	
				T_A = 105 °C	22	27	
				T_A = 125 °C	26.5	37	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	22	25	
				T_A = 85 °C	24	27	
				T_A = 105 °C	26	30	
				T_A = 125 °C	30.5	39	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	32	34	
				T_A = 55 °C	32.5	35	
				T_A = 85 °C	34	37	
				T_A = 105 °C	36	39	
				T_A = 125 °C	40	47	

1. Guaranteed by characterization results at 125 °C, not tested in production, unless otherwise specified.

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

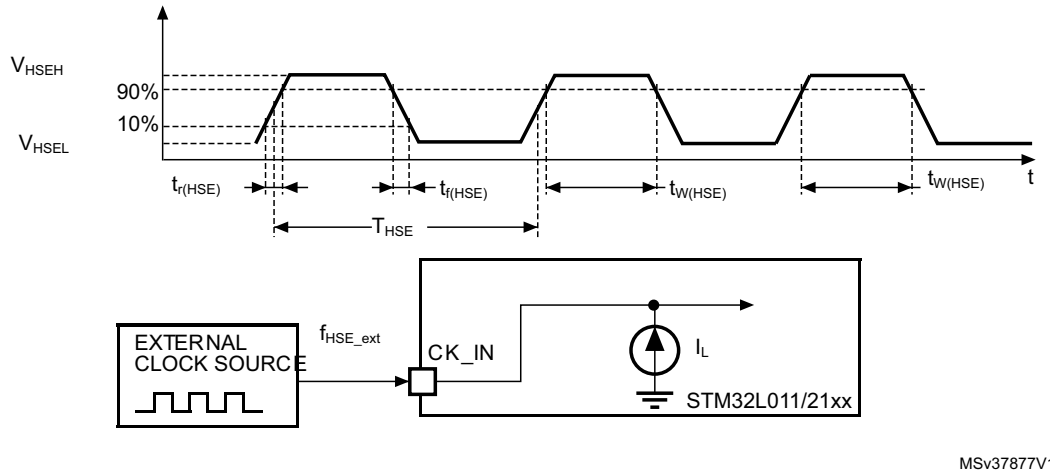
In bypass mode the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.12*. However, the recommended clock input waveform is shown in *Figure 19*.

Table 34. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is ON or PLL is used	1	8	32	MHz
		CSS is OFF, PLL not used	0	8	32	MHz
V_{HSEH}	CK_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	CK_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	CK_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	CK_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	CK_IN input capacitance		-	2.6	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	CK_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 19. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

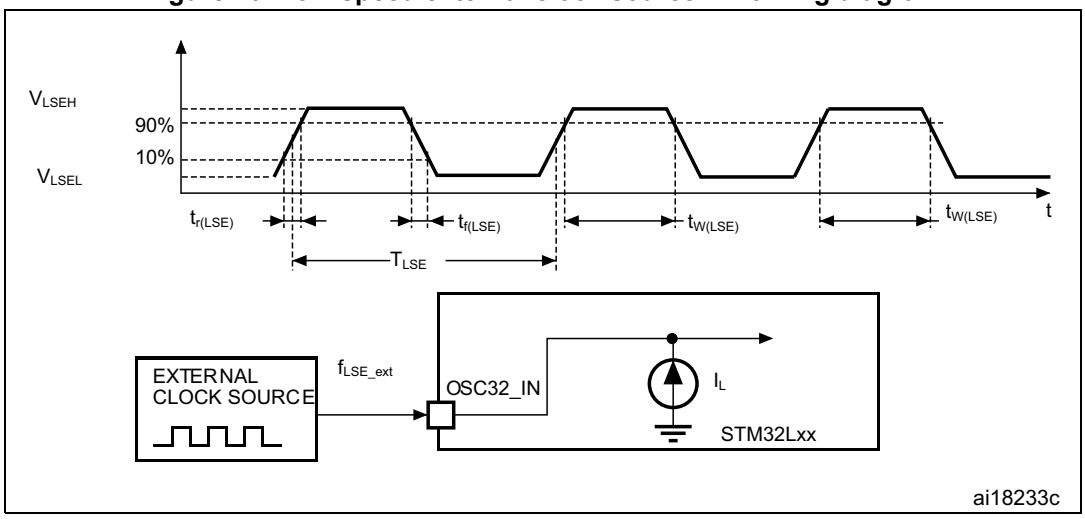
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 17*.

Table 35. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	V
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time	-	465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	10	ns
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 36*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Table 17. All I/Os are CMOS and TTL compliant.

Table 50. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin	CMOS port(2), I_{IO} = +8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		V_{DD}-0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2), I_{IO} =+ 8 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	TTL port(2), I_{IO} = -6 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +15 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	I_{IO} = -15 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL} (1)(4)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V ≤ V_{DD} < 3.6 V	-	0.45	
V_{OH} (3)(4)	Output high level voltage for an I/O pin	I_{IO} = -4 mA 1.65 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.45	-	
V_{OLFM+} (1)(4)	Output low level voltage for an FTf I/O pin in Fm+ mode	I_{IO} = 20 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		I_{IO} = 10 mA 1.65 V ≤ V_{DD} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 15*. The sum of the currents sunk by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 15*. The sum of the currents sourced by all the I/Os (I/O ports and control pins) must always be respected and must not exceed $\Sigma I_{IO(PIN)}$.
4. Guaranteed by characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 25* and *Table 51*, respectively.

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 17*.

Table 51. I/O AC characteristics(1)(2)

OSPEEDRx [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(3)	Unit
00	$f_{max(IO)out}$	Maximum frequency(4)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	320	
01	$f_{max(IO)out}$	Maximum frequency(4)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	0.6	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	65	
10	$F_{max(IO)out}$	Maximum frequency(4)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	13	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	28	
11	$F_{max(IO)out}$	Maximum frequency(4)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	35	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	10	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	6	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	17	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. BOOT0/PB9 maximum input frequency is 10 kHz (1.65 V < V_{DD} < 2.7 V) and 5 MHz (2.7 V < V_{DD} < 3.6 V).
3. Guaranteed by design. Not tested in production.
4. The maximum frequency is defined in *Figure 25*.

Table 54. R_{AIN} max for f_{ADC} = 16 MHz(1)

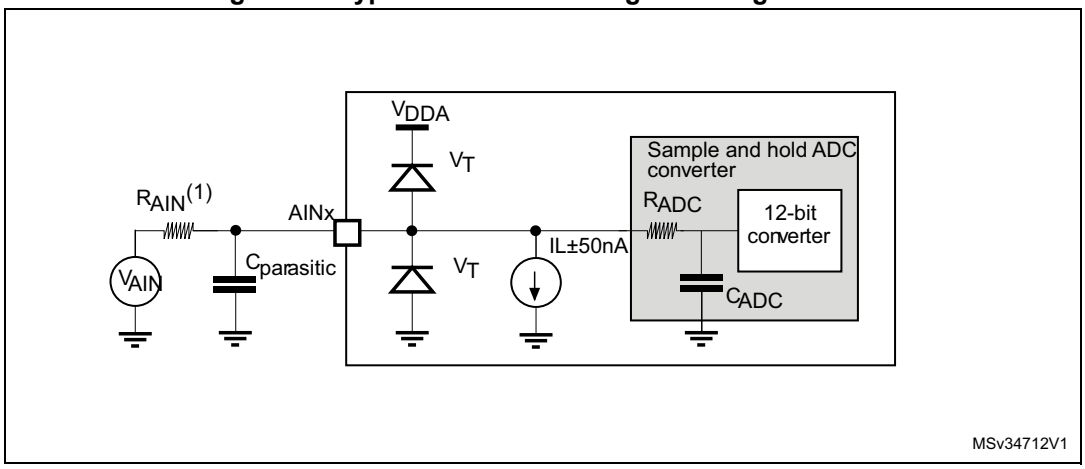
T_s (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > -10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 55. ADC accuracy(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} < 3.6 V, range 1/2/3, except for TSSOP14 package	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(5)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		62	67.8	-	dB
SNR	Signal-to-noise ratio		63	68	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(5)		70	76	-	
THD	Total harmonic distortion		-	-81	-68.5	

Figure 28. Typical connection diagram using the ADC



1. Refer to *Table 53: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.16 Temperature sensor characteristics

Table 56. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C ± 5 °C, V_{DDA}= 3 V ± 10 mV	0x1FF8 007E - 0x1FF8 007F

Table 57. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results, not tested in production.
2. Measured at V_{DD} = 3 V ±10 mV. V30 ADC conversion result is stored in the TS_CAL1 byte.
3. Guaranteed by design, not tested in production.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I²C timing requirements are guaranteed by design when the I²C peripheral is properly configured (refer to the reference manual for details) and when the I2CCLK frequency is greater than the minimum given in *Table 62*. The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I²C SDA and SCL I/Os embed an analog filter (see *Table 61* for the analog filter characteristics).

Table 61. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	100(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

Table 62. I2C frequency in all I2C modes

Symbol	Parameter	Condition		Min	Unit
f_{I2CCLK}	I2C clock frequency	Standard-mode		2	MHz
		Fast-mode		8	
		Fast-mode Plus	Analog filter ON, DNF = 0	18	
			Analog filter OFF, DNF = 1	16	

SPI characteristics

Unless otherwise specified, the parameters given in the following tables are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 17*.

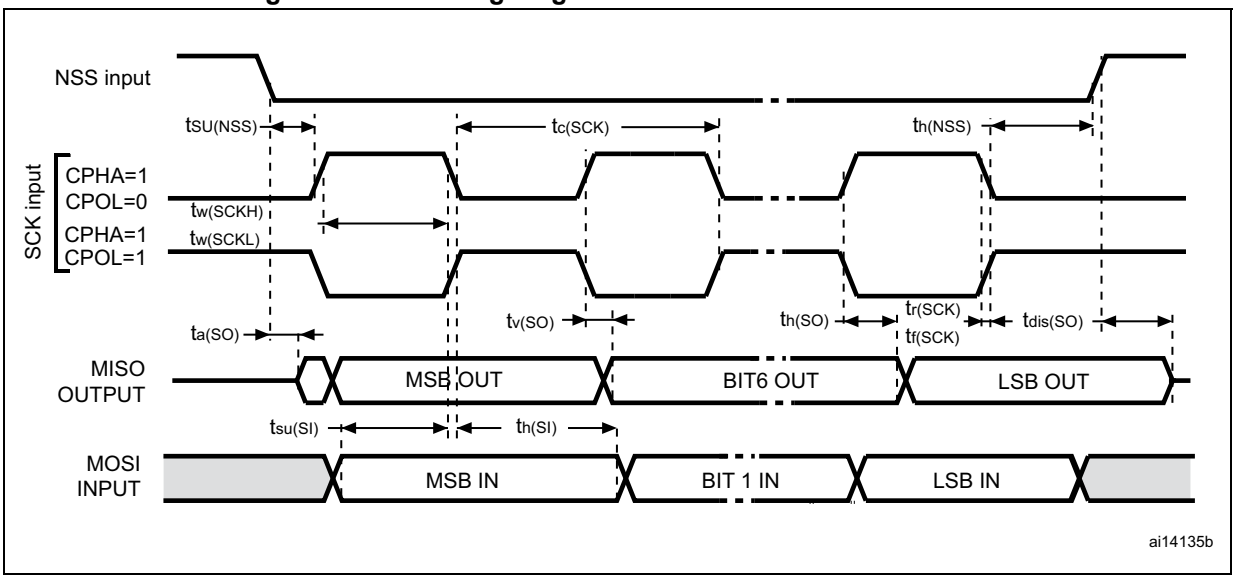
Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 64. SPI characteristics in voltage Range 1 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	16	MHz
		Slave mode receiver			16	
		Slave mode Transmitter 1.71<V_{DD}<3.6V	-	-	12(2)	
		Slave mode Transmitter 2.7<V_{DD}<3.6V	-	-	16(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	3	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	3.5	-	-	
$t_{h(SI)}$		Slave mode	0	-	-	
$t_{a(SO}$	Data output access time	Slave mode	15	-	36	
$t_{dis(SO)}$	Data output disable time	Slave mode	10	-	30	
$t_{v(SO)}$	Data output valid time	Slave mode 1.71<V_{DD}<3.6V	-	14	35	
		Slave mode 2.7<V_{DD}<3.6V	-	14	20	
$t_{v(MO)}$		Master mode	-	4	6	
$t_{h(SO)}$	Data output hold time	Slave mode	10	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

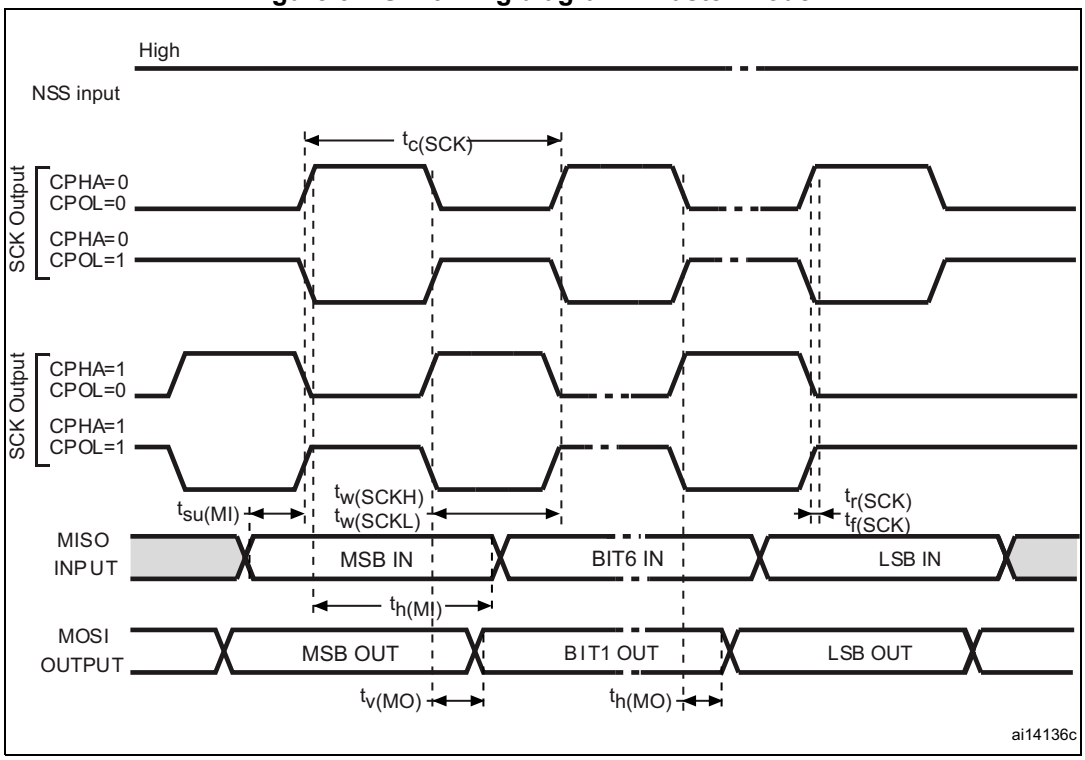
1. Guaranteed by characterization results, not tested in production.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 30. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 31. SPI timing diagram - master mode(1)

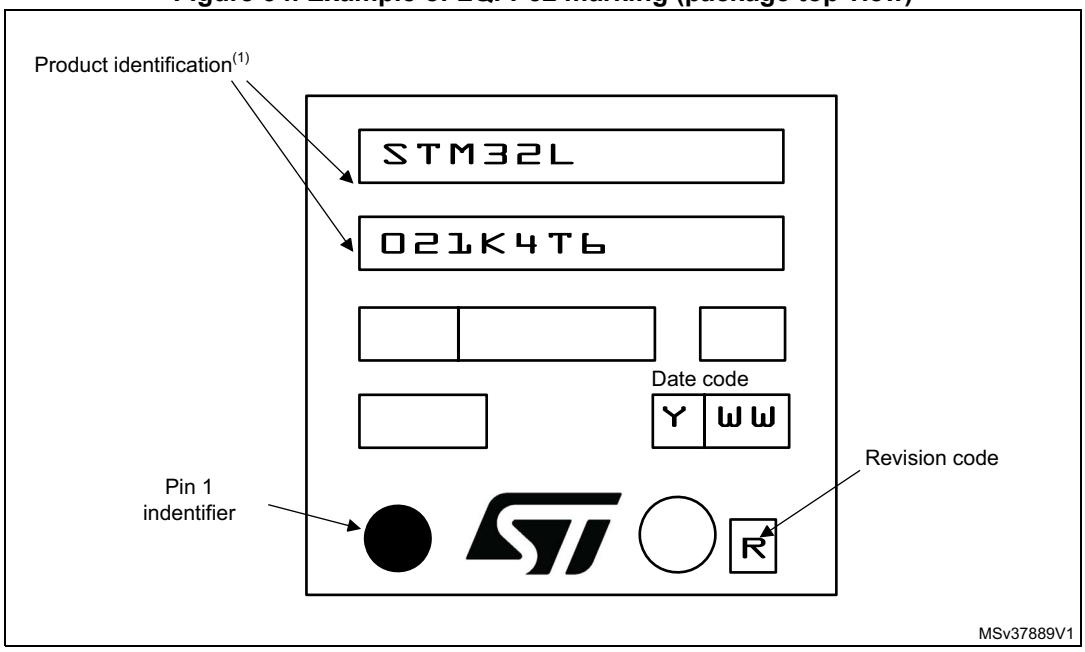


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

LQFP32 device marking

The following figure gives an example of topside marking versus pin 1 position identifier location.

Figure 34. Example of LQFP32 marking (package top view)



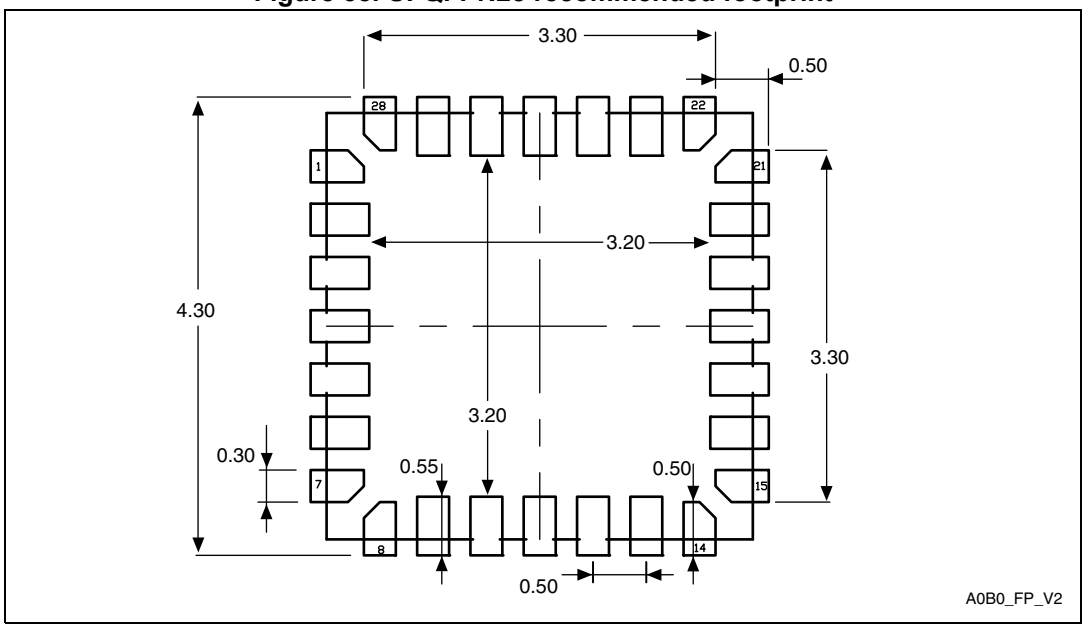
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 69. UFQPN28, 4 x 4 mm, 28-pin package mechanical data(1)

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. UFQFPN28 recommended footprint



1. Dimensions are expressed in millimeters.