



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3370am1gba-gah-ax

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Notes for CMOS Devices

1. Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

V850ES/FF3

Legal Notes

- The information in this document is current as of January 2007. The information is subject to change
 without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or
 data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products
 and/or types are available in every country. Please check with an NEC sales representative for
 availability and additional information.
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such NEC Electronics products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics
 products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated
 entirely. To minimize risks of damage to property or injury (including death) to persons arising from
 defects in NEC Electronics products, customers must incorporate sufficient safety measures in their
 design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

- "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
- "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
- "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact NEC Electronics sales representative in advance to determine NEC Electronics 's willingness to support a given application.

- **Notes: 1.** "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
 - **2.** "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).
 - **3.** SuperFlash[®] is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan. This product uses SuperFlash[®] technology licensed from Silicon Storage Technology, Inc.



For further information, please contact:

NEC Electronics Corporation

1753, Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa 211-8668, Japan Tel: 044-435-5111 http://www.necel.com/

[America]

NEC Electronics America, Inc.

2880 Scott Blvd. Santa Clara, CA 95050-2554, U.S.A. Tel: 408-588-6000 800-366-9782 http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH

Arcadiastrasse 10 40472 Düsseldorf, Germany Tel: 0211-65030 http://www.eu.necel.com/

> Hanover Office Podbielski Strasse 166 B 30177 Hanover Tel: 0 511 33 40 2-0

Munich Office

Werner-Eckert-Strasse 9 81829 München Tel: 0 89 92 10 03-0

Stuttgart Office

Industriestrasse 3 70565 Stuttgart Tel: 0 711 99 01 0-0

United Kingdom Branch

Cygnus House, Sunrise Parkway Linford Wood, Milton Keynes MK14 6NP, U.K.

Tel: 01908-691-133

Succursale Française

9, rue Paul Dautier, B.P. 52180 78142 Velizy-Villacoublay Cédex France Tel: 01-3067-5800

Sucursal en España

Juan Esplandiu, 15 28007 Madrid, Spain Tel: 091-504-2787

Tyskland Filial

Täby Centrum Entrance S (7th floor) 18322 Täby, Sweden Tel: 08 638 72 00

Filiale Italiana

Via Fabio Filzi, 25/A 20124 Milano, Italy Tel: 02-667541

Branch The Netherlands

Steijgerweg 6 5616 HS Eindhoven The Netherlands Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd 7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian District, Beijing 100083, P.R.China TEL: 010-8235-1155 http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.

Room 2509-2510, Bank of China Tower, 200 Yincheng Road Central, Pudong New Area, Shanghai P.R. China P.C:200120 Tel: 021-5888-5400 http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.

12/F., Cityplaza 4, 12 Taikoo Wan Road, Hong Kong Tel: 2886-9318 http://www.hk.necel.com/

Seoul Branch

11F., Samik Lavied'or Bldg., 720-2, Yeoksam-Dong, Kangnam-Ku, Seoul, 135-080, Korea Tel: 02-558-3737

NEC Electronics Taiwan Ltd.

7F, No. 363 Fu Shing North Road Taipei, Taiwan, R. O. C. Tel: 02-8175-9600

NEC Electronics Singapore Pte. Ltd.

238A Thomson Road, #12-08 Novena Square, Singapore 307684 Tel: 6253-8311 http://www.sg.necel.com/

G06.6-1A

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3 device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
μPD70F3370A	64	FE3
μΡD70F3371		
μPD70F3372	80	FF3
μΠD70F3374		
μPD70F3375	500	
uPD70F3376A	100	FG3
μPD70F3377A		
μPD70F3378		
μPD70F3379		
μPD70F3380	144	FJ3
μPD70F3381		
μPD70F3382		
μPD70F3383		
μPD70F3384	176	FK3
μPD70F3385		

This document describes the specification for the V850ES/FF3.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)

- P04, P30-31, P34; P40, P91, P913-915 (FE3)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915 (FJ3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915, P156-157 (FK3)
- 1D: (SHMT3)
 - P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3)
 - P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3)
 - P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3)
 - P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912 (FJ3)
 - P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912, P150-155 (FK3)

1.3 Pin Groups 2x: Pins supplied by EVDD

- 2A: (CMOS)
 - PCM0-1 (FE3)
 - PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3)
- 2D: (SHMT3)
 - PDL0-7 (FE3)
 - PDL0-11 (FF3)

2.3 Operating condition

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f _{VBCLK})	Supply voltage	Operating Condition
		Operation of functions is usable under following conditions:
		 Peripheral clock frequency
	A AN A A A A A A A A A A A A A A A A A	• $f_{XP1} \le 32MHz$
	4.0V≤VDD≤5.5V	• $f_{XP2} \le 32MHz$
		AC characteristics:
		 Refer to chapter '2.7 AC Characteris- tics' for details.
		Operation of functions is usable under following conditions:
		 Peripheral clock frequency
	Noto?	• $f_{XP1} \le 20MHz$
	3.5V≤VDD<4.0V ^{NOLE2}	• $f_{XP2} \le 20MHz$
		AC characteristics:
		 Refer to chapter '2.7 AC Characteris- tics' for details.
4.0≤f _{xx} ≤32MHz Note1		Only operation of the following functions is assured:
		Flash (include programming)
		• RAM
	3.3V≤VDD<3.5V ^{Note2}	IO Buffer
		Port
		• WT
		• WDT
		• INT
		• CLM
		• POC
		• LVI
		• A/D Converter
	3 3V <avree0<5 5v<="" td=""><td>Refer to chapter 2.8 A/D Converter for details</td></avree0<5>	Refer to chapter 2.8 A/D Converter for details
		 stop ADC for AVREF0 < 4.0V
		(ADA0CE bit =0)
32kHz≤f _{XT} ≤35kHz (Crystal)		
12.5kHz⊴f _{XT} ≤27.5kHz ^{Note3} (RC)	3.3V≦VDD<5.5V	-
f _{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V ^{Note2}	-

Notes: 1. For using SSCG please refer to '2.5.5 SSCG Characteristics' for details
2. VDD = EVDD

3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.4 Voltage Regulator Characteristics

Ta = -40 to +85°C, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V))							
Parameter	Symbol	Conditions		TYP.	MAX.	Unit	
Input voltage			3.5		5.5	V	
	VDD	Limited function see '2.3 Operating condition'	3.3			V	
Output voltage	VRO			2.5		V	
Output voltage stabilization time	t _{REG} ^{Note}	After VDD reaches voltage range min. 3.3V To connect C=4.7uF on REGC terminal			1	ms	

Note: In case of non-POC device, be sure to start VDD in the state of RESET=VSS=0V. For POC devices there is no need to control external RESET terminal. For decives with POC function the internal RESET signal will automatically controlled until VRO is stable.



2.5 Clock Generator Circuit

2.5.1 Main System Clock Oscillation Circuit Characteristics

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal / Ceramic resona- tor	Refer to figure below	Oscillator fre- quency (fx) ^{Note1}		4		16	MHz
		Oscillation stabili-	After STOP mode	64 ^{Note4}	Note3		μs
		zation time ^{Note2}	After IDLE2 mode	54 ^{Note4}	Note3		μs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to '2.7 AC Characteristics' for CPU operation clock.

- 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range MIN. 3.3V
- 3. Depends on the setting of the oscillation stabilization time select register (OSTS)
- **4.** Minimum time required to stabilize flash. Time has to be secured by setting the oscillation stabilization time select register (OSTS)



2.5.2 Sub System Clock Oscillation Circuit Characteristics

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
		Oscillator fre-		22	22 769	25	kU=
Crystal resonator	Dofor to Figure 1	quency (fxt) ^{Note1}		32	32.700	35	KΠZ
	Refer to Figure 1	Oscillation stabiliza-				10	
		tion time Note2					5
RC resonator	Refer to Figure 2	Oscillator	R=390K Ω ±5% ^{Note3} ,	25	40	55	
		frequency ^{Note1,4}	C=47pF±10% Note3	25	40	55	КПД
		Oscillation stabiliza-				100	
		tion time Note2				100	μs

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

- 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V
- 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
- 4. RC Oscillation frequency is typ. 40kHz. This clock is divided by 2 internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

4	T 40 4- 10500	0-47-5	VDD = EVDD = 0.04	AV/DEEA = A A A = E EV/	1/00 - 51/00 - 41/00 - 01/1
1	$12 = -40 \text{ to } +85^{\circ}$		V(1)) = F(1) = 3.3 TO 5.5V	$\Delta V R = 0 = 3.3 to 5.5 V$	VSS = FVSS = AVSS = 0V
1	10 40 10 00 0	, • • ui			, 100 - L100 - A100 - 01)

()))))))))))))))))))	,	,	,		• •	
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output	f _{RL}	240kHz Internal-OSC	204	240	276	kHz
frequency	f _{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation		240kHz Internal-OSC		10	36	μs
stabilization time		8MHz Internal-OSC	51	92	256	μs

2.5.4 PLL Characteristics

	T 40 4- 10E0C		- EV(DD - 0.04) = EV(DD - 0.04)	1/00 - 5/00 - 4/00 - 0/0
	$12 = -401 \text{ to } + 85^{\circ}$: (:=4 /IIE VIII	= + v (1) = 3 + 10 + 5v	
۰.	10	, o- - ./ui , voc		

· · ·	,			,		
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input fraguanay	fx		4		16	MHz
input irequency	f _{PLLI}	Note1	3		6	MHz
Output frequency	fxx	≤256KB product	12		32	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X , $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

2.5.5 SSCG Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	f _{XX}	≤256KB product	12		32	MHz
Lock time	t _{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector	Percent modulation		Maximum average operating fre- quency		
SFC [[0.4]	TYP	MAX	\leq 256KB product		
000B	± 0.5%	± 2.0%	31.4		
001B	± 1.0%	± 2.5%	31.2		
010B	± 2.0%	± 4.0%	30.7		N/LI-7
011B	± 3.0%	± 6.0%	30.1		
100B	± 4.0%	± 8.0%	29.4		
101B	± 5.0%	± 10.0%	28.8		

2.6 DC Characteristics

2.6.1 Input/Output Level

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Sym- bol	Cor	Conditions		TYP.	MAX.	Uni t
	VIH1	Pin G	Group 1B	0.7·EVDD		EVDD	V
		Pin G	Froup 1D	0.8.EVDD		EVDD	V
High level	VIEZ	Pin G	Froup 2D	0.8.EVDD		EVDD	V
input voltage	VIH3	Pin Group 2A		0.7·EVDD		EVDD	V
	VIH4	Pin	Group 4	0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
	VIL1	Pin G	Group 1B	EVSS		0.3·EVDD	V
		Pin G	Froup 1D	EVSS		0.4·EVDD	V
Low level	VILZ	Pin Group 2D		EVSS		0.4·EVDD	V
input voltage	VIL3	Pin G	Pin Group 2A			0.3·EVDD	V
	VIL4	Pin	Pin Group 4			0.3-AVREF0	V
	VIL5	Pin	Pin Group 6			0.2·EVDD	V
	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
Input hystoresis		Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
input hysteresis	VII 132	Pin Group 2D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High lovel	VOH1	Pin Group	IOH=-1.0mA	EVDD-1.0		EVDD	V
		1x, 2x	IOH=-100uA	EVDD-0.5		EVDD	V
Note2	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
		Din Croup 1v	IOH=-100uA	AVREF0-0.5		AVREF0	V
Low level output		2x	IOL=1.0mA	0		04	v
voltage ^{Note2}	1021	P914, 915	IOL=3.0mA	Ŭ		0.1	
, i i i i i i i i i i i i i i i i i i i	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	V	1=0V	10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI	VI=VDD		30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. DRST terminal only. (Control register is OCDM)

- 2. Total IOH/IOL max is 20mA/-20mA each power supply line (EVDD and AVREF0). AVREF0 IOH/IOL current is excluding ADC0 current IAREF0.
- 3. Typical value. Not tested and guaranteed



Mode	Symbol		Cc	ondition		TYP.	MAX.	Unit
					f _{xx} =5MHz f _x =5MHz	1.4	2.2	mA
		Peripheral (TAA, UARTD) run-		PLL: OFF 4MHz≤f _{xx} ≤16MHz	f _{xx} =12MHz f _x =12MHz	2.0	3.1	mA
		n	ning		f _{xx} =16MHz f _x =16MHz	2.4	3.6	mA
IDLE1			fxx=8MHz, 8MHz In	ternal-OSC ^{Note3}	1.5	2.3	mA	
mode	1003				f _{xx} =5MHz f _x =5MHz	1.2		mA
	All peripherals stopped	PLL: OFF 4MHz≤f _{xx} ≤16MHz	f _{xx} =12MHz f _x =12MHz	1.4		mA		
				f _{xx} =16MHz f _x =16MHz	1.6		mA	
				fxx=8MHz, 8MHz In	ternal-OSC ^{Note3}	1.1		mA
			f _{xx} =5MHz f _x =5MHz			0.4	0.7	mA
IDLE2	IDD4		PLL: OFF 4MHz≤f _{xx} ≤16M	f _{xx} =12MHz f _x =12MHz	0.7	1.0	mA	
mode			Noter	f _{xx} =16MHz f _x =16MHz	0.8	1.2	mA	
			fxx=8MHz, 8MHz Internal-OSC Note3					mA
SUB			Crystal resonat	or (fxt = 32,768kHz)		80	400	μA
operating	IDD5		RC resonator	r (fxt=20kHz) ^{Note6}		80	400	μA
mode ^{Note5}		2	240 kHz Internal-C	SC (SubOSC stoppe	d)	220	1000	μA
SubIDLE			Crystal resonat	or (fxt = 32,768kHz)		20	190	μA
mode	IDD6	RC resonator (fxt=20kHz) Note6					220	μA
Note3,5			240kHz Internal-O	SC (SubOSC stopped	(t	25	180	μA
STOP		POC stop	24	0kHz Internal-OSC st	op	7.5	80	μA
mode	IDD7		240	240kHz Internal-OSC working			95	μA
Note3,4		POC work	24	UKHz Internal-OSC st	ор	10.5	85	μA
,		ł	240	240kHz Internal-OSC working			100	μA

(b) Calculation formulas

(Ta = -40 to +85°C, C=4.7uF,

VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = $0V^{Note1}$)

Mode	Symbol		Condition			MAX. Note9	Unit
			Peripheral: f _{xx}	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.98·f _{xx} +7.1	1.18·f _{xx} +13.6	mA
		All peripherals running	PRSI option: 0	PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.98·f _{xx} +5.5	1.18·f _{xx} +10.6	mA
Operating mode IDD1 _{Note2,8}		Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.90·f _{xx} +6.0	1.08·f _{xx} +12.2	mA	
	All peripherals stopped	Peripheral: ff _{xx-}	PLL: ON 12MHz⊴f _{xx} ≤32MHz	0.81·f _{xx} +6.2		mA	
		PRSI option: 0	PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.83·f _{xx} +5.7		mA	
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.79·f _{xx} +6.2		mA
		All peripherals running	Peripheral: ff _{xx-} PRSI option: 0	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.67·f _{xx} +3.0	0.90*f _{xx} +5.4	mA
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.70·f _{xx} +1.9	1.00*f _{xx} +4.0	mA
HALT	נחחו		Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.55·f _{xx} +2.8	0.64*f _{xx} +7.0	mA
Note8	IDD2		Peripheral: f _{xx}	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.46·f _{xx} +2.8		mA
		All peripherals stopped	PRSI option: 0	PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.44·f _{xx} +1.6		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz⊴f _{xx} ≤32MHz	0.46·f _{xx} +1.8		mA
IDLE1	.E1 IDD3 Peripheral (TA		A, UARTD) run- ng	PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.092·f _{xx} +0.90	0.128·f _{xx} + 1.35	mA
moue		All peripher	rals stopped	Note7	0.035·f _{xx} +1.01		mΑ
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f _{xx} ≤16MHz ^{Note7}			0.037·f _{xx} +0.21	0.049·f _{xx} + 0.43	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).

AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pulldown resistor) are not included.

- 2. The code flash and the data flash are in read mode. When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:
 - Self-programming mode:
 - + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
 - + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
 - Data flash programming mode:
 - + 7-(0.18*fxx/4+3.0) [mA]
- 3. Main OSC is stopped.
- **4.** Do not use SubOSC.
- 5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
- 6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
- 7. 8MHz Internal-OSC is stopped
- 8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
- **9.** The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.



3.5.2 Sub System Clock Oscillation Circuit Characteristics

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator Refer to Figure 2	Oscillator frequency ^{Note1,4}	R=390KΩ ±5% ^{Note3} , C=47pF±10% ^{Note3}	25	40	55	kHz	
		Oscillation stabiliza- tion time Note2				100	μs

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

- 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V
- **3.** In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
- **4.** RC Oscillation frequency is typ. 40kHz. This clock is divided by 2 internally. In case of RC Oscillator, internal system clock frequency(fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.



3.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.4 PLL Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.5 SSCG Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.6.3 Power supply current (A1-grade)

3.6.3.1 FF3 128KB $\mu\text{PD70F3372},$ FF3 256KB $\mu\text{PD70F3373}$

(a) Absolute values (Ta = -40 to +110°C, C=4.7uF,

VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1})

Mode	Symbol		Condition					Unit
	-			PLL: ON	f _{xx} =20MHz f _x =5MHz	27	37	mA
			Dariphoral: f	12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	39	51	mA
		All peripherals running	Peripheral. 1 _{xx} PRSI option: 0	PLL: OFF 4MHz <f <16mhz<="" td=""><td>f_{xx}=8MHz 8MHz Internal- OSC ^{Note3}</td><td>13</td><td>20</td><td>mA</td></f>	f _{xx} =8MHz 8MHz Internal- OSC ^{Note3}	13	20	mA
					f _{xx} =16MHz f _x =16MHz	21	30	mA
Operating	1חחו		Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	35	47	mA
Note2,8	ושטו			PLL: ON	f _{xx} =20MHz f _x =5MHz	22		mA
			Perinheral: f	12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	32		mA
	All peripherals stopped	Peripheral: 1 _{xx} PRSI option: 0	PLL: OFF 4MHz <f<16mhz< td=""><td>f_{xx}=8MHz 8MHz Internal- OSC ^{Note3}</td><td>12</td><td></td><td>mA</td></f<16mhz<>	f _{xx} =8MHz 8MHz Internal- OSC ^{Note3}	12		mA	
					f _{xx} =16MHz f _x =16MHz	19		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	31		mA
			PLL: ON	f _{xx} =20MHz f _x =5MHz	16	23	mA	
		All peripherals running	Peripheral: f _{xx} PRSI option: 0	12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	24	34	mA
				PLL: OFF 4MHz≤f _{vv} ≤16MHz	f _{xx} =8MHz 8MHz Internal- OSC _{Note3}	8	12	mA
					f _{xx} =16MHz f _x =16MHz	13	20	mA
HALT mode	IDD2		Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	20	27	mA
Note8				PLL: ON	f _{xx} =20MHz f _x =5MHz	12		mA
			Perinheral: f	12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	18		mA
		All peripherals stopped	PRSI option: 0	PLL: OFF	f _{xx} =8MHz 8MHz Internal- OSC ^{Note3}	5		mA
					f _{xx} =16MHz f _x =16MHz	9		mA
				Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	f _{xx} =32MHz f _x =16MHz	17	



3.7 AC Characteristics

AC test Input measurement points (VDD, AVREF0, EVDD)



AC test output measurement points



Load conditions



Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

3.7.1 CLKOUT Output Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.2 RESET, Interrupt, ADTRG Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.3 Key Return Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.4 Timer Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.5 CSI Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.6 UART Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.7 IIC Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.7.8 CAN Timing

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.8 A/D Converter

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.9 POC

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.10 LVI

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.11 RAM Retention Flag

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.12 Data Retention Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

<u>(</u> ,		,,					
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Operation frequency	fCPU		4		32	MHz	
Supply voltage	VDD		3.3		5.5	V	
		Code Flash	1000				
Number of rewrites	CWRTT	Data Elash	1000			count	
	CWRT2	Data Flash	10000				
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V	
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V	
Programming temperature	tPRG		-40		+110	°C	
		Code Flash			⊿ –Note1		
Data retention		Data Flash			15.000		
		Data Flash			5 ^{Note2}		

Notes: 1. Under the condition of CWRT12. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase \rightarrow write set of operations, or any programming operation is counted as one rewrite. Example: P: Program(write) E: Erase Product is shipped $\rightarrow P \rightarrow E \rightarrow P \rightarrow E \rightarrow P$: Rewrite count: 3 Product is shipped $\rightarrow E \rightarrow P \rightarrow E \rightarrow P \rightarrow E \rightarrow P$: Rewrite count: 3

(b) Serial Writing Operation Characteristics Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.



4.5.2 Sub System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A1)-Grade except Ta=-40 to +125°C.

4.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.5.4 PLL Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
i alametei	Oymbol	Contaitionio			100 0 1.	Onic
Input fraguisnov	fx		4		16	MHz
input inequency	f _{PLLI}	Note	3		6	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X , $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

4.5.5 SSCG Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
Lock time	t _{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector	Percent modulation		Maximum average operating fre- quency		
SFC [[0.4]	TYP	MAX	≤256KB product		
000B	± 0.5%	± 2.0%	23.5		
001B	± 1.0%	± 2.5%	23.4		
010B	± 2.0%	± 4.0%	23.0		
011B	± 3.0%	± 6.0%	22.6		
100B	± 4.0%	± 8.0%	22.1		
101B	± 5.0%	± 10.0%	21.6		

V850ES/FF3



Mode	Symbol		Condition		TYP.	MAX.	Unit
IDLE2 mode IDD4					1.1	mA	
		PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7	f _{xx} =12MHz f _x =12MHz	0.7	1.5	mA	
			f _{xx} =16MHz f _x =16MHz	0.8	1.7	mA	
			fxx=8MHz, 8MHz Internal-OSC Note3				
SUB			RC resonator (fxt=20kHz) Note6				μA
operating mode ^{Note5}	IDD5	240 kHz Internal-OSC (SubOSC stopped)				1450	μA
SubIDLE			RC resonator (fxt=20kHz) Note6	or (fxt=20kHz) ^{Note6}			μA
Mode Note3,5	mode IDD6 Note3,5	240kHz Internal-OSC (SubOSC stopped)				630	μA
STOD		POC stop	240kHz Internal-OSC sto	ор	7.5	530	μΑ
mode	דחחו	100300	240kHz Internal-OSC working			545	μA
Note3.4	1001	POC work	240kHz Internal-OSC stop			535	μA
NOICO, T		1 CC WORK	240kHz Internal-OSC working			550	μA

V850ES/FF3

NEC

5. Package

5.1 Package Dimension

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



its true position at maximum material condition.

© NEC Electronics Corporation 2005

6. Change History

The following revision list shows all major changes of the different datasheet versions.

Version	Chapter	Comment
V1.0		Initial release
	2.13	Removed 'Target Specification' for (A)- and (A1)-Grade Devices in the Flash Pro- gramming specifications.
V1.1	0.10	Changed specification of 'Number of rewrites' from MAX. to MIN.
	2.8 4.8	Remove Caution (Described in User's Manual)
		Changed document status from 'Preliminary Datasheet' to 'Datasheet'.
V1.2	4.13	Removed 'Target Specification' for (A2)-Grade Devices in the Flash Programming specifications.

NEC

Facsimile Message

FAX

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

Address

Tel.

From:

Name

Company

Thank you for your kind support.

North America NEC Electronics America Inc. Corporate Communications Dept. Fax: 1-800-729-9288 1-408-588-6130	Hong Kong, Philippines, Oceania NEC Electronics Hong Kong Ltd. Fax: +852-2886-9022/9044	Asian Nations except Philippines NEC Electronics Singapore Pte. Ltd. Fax: +65-6250-3583	
Europe NEC Electronics (Europe) GmbH Market Communication Dept. Fax: +49(0)-211-6503-1344	Korea NEC Electronics Hong Kong Ltd. Seoul Branch Fax: 02-528-4411	Japan NEC Semiconductor Technical Hotline Fax: +81- 44-435-9608	
	Taiwan NEC Electronics Taiwan Ltd. Fax: 02-2719-5951		

I would like to report the following error/make the following suggestion:

Document title: ___

Document number: ____

_____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity				
Technical Accuracy				
Organization				