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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3.3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3370m2gba-gah-ax

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2.3 Operating condition

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition

4.0≤f_{xx}≤32MHz Note1	4.0V≤VDD≤5.5V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • f_{XP1} ≤ 32MHz
		  • f_{XP2} ≤ 32MHz
		• AC characteristics:
		  • Refer to chapter '2.7 AC Characteristics' for details.

	3.5V≤VDD<4.0V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • f_{XP1} ≤ 20MHz
		  • f_{XP2} ≤ 20MHz
		• AC characteristics:
		  • Refer to chapter '2.7 AC Characteristics' for details.

	3.3V≤VDD<3.5V Note2	Only operation of the following functions is assured: • CPU • Flash (include programming) • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI

	3.3V≤AVREF0≤5.5V	• A/D Converter
		  • Refer to chapter '2.8 A/D Converter' for details.
		  • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0)

32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note2	-
12.5kHz≤f_{XT}≤27.5kHz Note3 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note2	-

Notes: 1. For using SSCG please refer to '2.5.5 SSCG Characteristics' for details

2. VDD = EVDD

3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.5.4 PLL Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note1	3		6	MHz
Output frequency	fxx	≤256KB product	12		32	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

2.5.5 SSCG Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	f_{XX}	≤256KB product	12		32	MHz
Lock time	t_{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector SFC1[6:4]	Percent modulation		Maximum average operating frequency		Unit
	TYP	MAX	≤256KB product		
000B	± 0.5%	± 2.0%	31.4		MHz
001B	± 1.0%	± 2.5%	31.2		
010B	± 2.0%	± 4.0%	30.7		
011B	± 3.0%	± 6.0%	30.1		
100B	± 4.0%	± 8.0%	29.4		
101B	± 5.0%	± 10.0%	28.8		

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	1.4	2.2	mA
				f_{xx}=12MHz f_X=12MHz	2.0	3.1	mA
				f_{xx}=16MHz f_X=16MHz	2.4	3.6	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.5	2.3	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	1.2		mA
				f_{xx}=12MHz f_X=12MHz	1.4		mA
				f_{xx}=16MHz f_X=16MHz	1.6		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.1		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_X=5MHz	0.4	0.7	mA
				f_{xx}=12MHz f_X=12MHz	0.7	1.0	mA
				f_{xx}=16MHz f_X=16MHz	0.8	1.2	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			80	400	μA
		RC resonator (fxt=20kHz) Note6			80	400	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1000	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	μA
		RC resonator (fxt=20kHz) Note6			40	220	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	80	μA
			240kHz Internal-OSC working		15.5	95	μA
		POC work	240kHz Internal-OSC stop		10.5	85	μA
			240kHz Internal-OSC working		18.5	100	μA

(b) Calculation formulas

(Ta = -40 to +85°C, C=4.7uF,
VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note9]	MAX. [Note9]	Unit
Operating mode [Note2,8]	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	0.98·f_{xx}+7.1	1.18·f_{xx}+13.6	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.98·f_{xx}+5.5	1.18·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.90·f_{xx}+6.0	1.08·f_{xx}+12.2	mA
		All peripherals stopped	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	0.81·f_{xx}+6.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.83·f_{xx}+5.7		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.79·f_{xx}+6.2		mA
HALT mode [Note8]	IDD2	All peripherals running	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.67·f_{xx}+3.0	0.90*f_{xx}+5.4	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.70·f_{xx}+1.9	1.00*f_{xx}+4.0	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.55·f_{xx}+2.8	0.64*f_{xx}+7.0	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+2.8		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz [Note7]	0.092·f_{xx}+0.90	0.128·f_{xx}+ 1.35	mA
		All peripherals stopped			0.035·f_{xx}+1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz [Note7]			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.43	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
- Data flash programming mode:
  + 7-(0.18*fxx/4+3.0) [mA]

3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7.5 CSI Timing

(a) Master mode

(Ta = -40 to +85°C, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

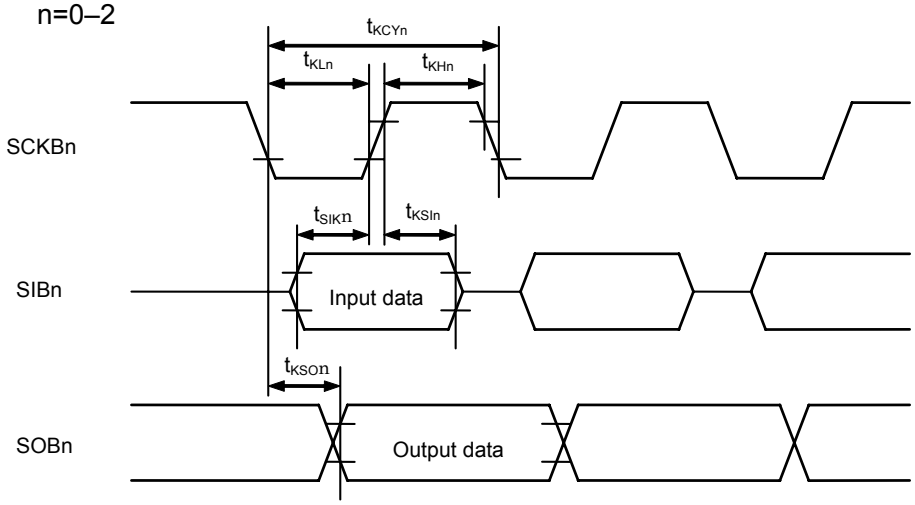
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–2



2.7.6 UART Timing

(Ta = -40 to +85°C, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

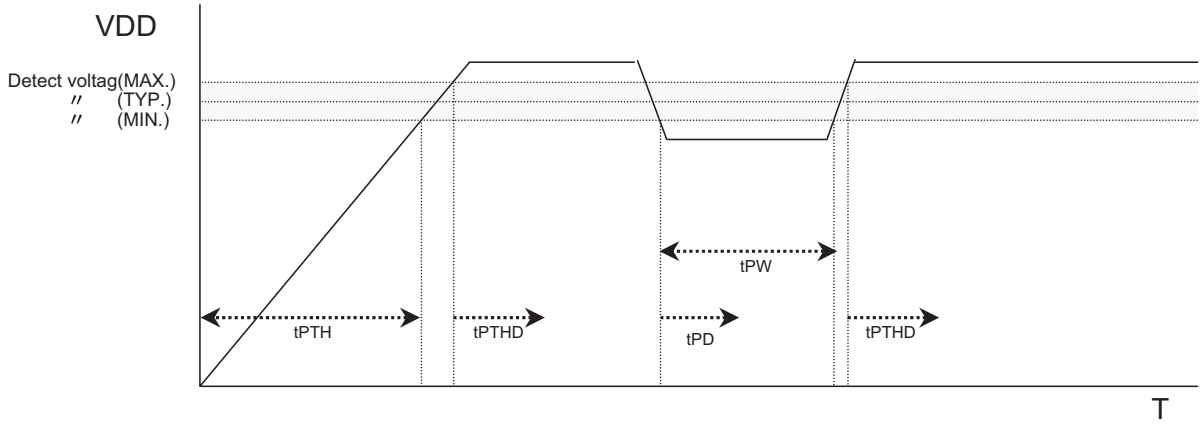
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.9 POC

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 Note1	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 Note2	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

Notes: 1. From detect voltage to release reset signal
2. From detect voltage to occurrence of reset signal



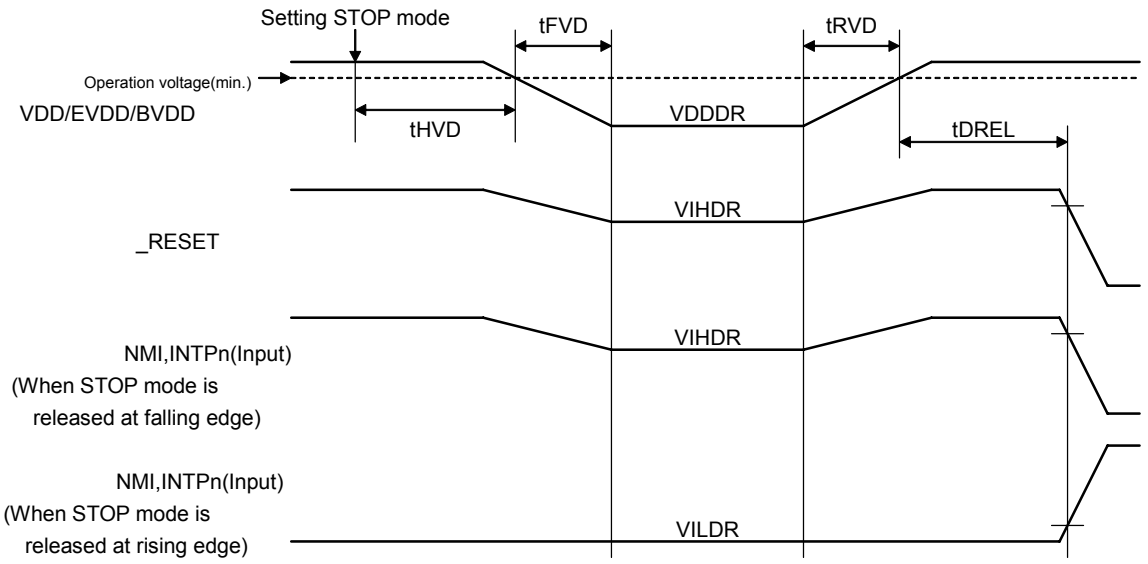
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3 User's Manual.

2.12 Data Retention Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V) (

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	VDDDR	STOP mode (All function is stopped)	1.9		5.5	V
Data retention power supply current	IDDDR	VDDDR=2.0V(All function is stopped)		6.5	70	μA
Supply voltage rise time	tRVD		1			μs
Supply voltage fall time	tFVD		1			μs
Supply voltage hold time	tHVD	After STOP mode	0			ms
STOP release signal input time	tDREL	After VDD reaches operating voltage range MIN. 3.3V	0			ms
Data retention high-level input voltage	VIHDR	All input port	0.9VDDDR		VDDDR	V
Data retention low-level input voltage	VILDR	All input port	0		0.1VDDDR	V

Remark: When STOP mode is entered/released operation voltage range must be controlled.



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU		4		32	MHz
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+85	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

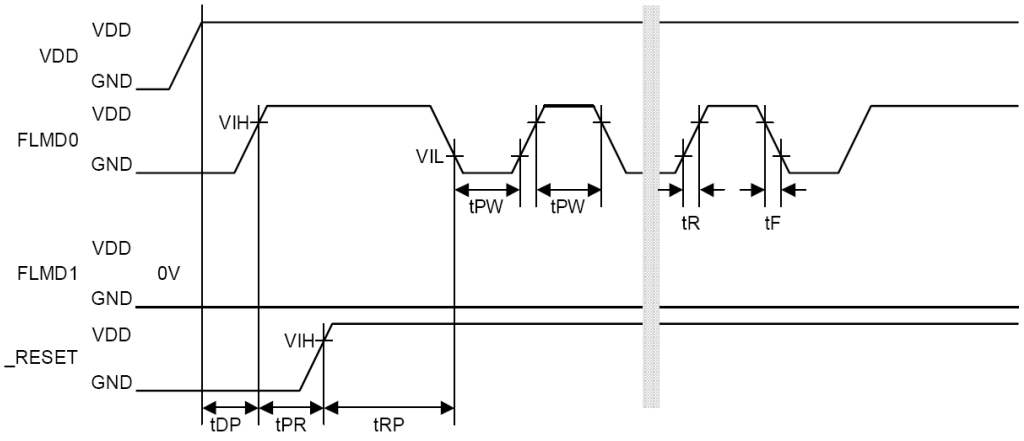
Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			μs
FLMD0 high level width / low level width	tPW		10		100	μs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns



3.6 DC Characteristics

3.6.1 Input/Output Level

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 2D		0.8·EVDD		EVDD	V
	VIH3	Pin Group 2A		0.7·EVDD		EVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 2D		EVSS		0.4·EVDD	V
	VIL3	Pin Group 2A		EVSS		0.3·EVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 2D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x, 2x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
Low level output voltage Note2	VOL1	Pin Group 1x, 2x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA for the power supply line EVDD.
Total IOH/IOL max is 10mA/-10mA for the power supply line AVREF0.
AVREF0 IOH/IOL current is excluding ADC0 current IAREF0.

3. Typical value. Not tested and guaranteed

4.5.2 Sub System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A1)-Grade except Ta=-40 to +125°C.

4.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.5.4 PLL Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note	3		6	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

4.5.5 SSCG Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
Lock time	t_{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector SFC1[6:4]	Percent modulation		Maximum average operating frequency		Unit
	TYP	MAX	≤256KB product		
000B	± 0.5%	± 2.0%	23.5		MHz
001B	± 1.0%	± 2.5%	23.4		
010B	± 2.0%	± 4.0%	23.0		
011B	± 3.0%	± 6.0%	22.6		
100B	± 4.0%	± 8.0%	22.1		
101B	± 5.0%	± 10.0%	21.6		

4.6.3 Power supply current (A2-grade)

4.6.3.1 FF3 128KB μPD70F3372, FF3 256KB μPD70F3373

(a) Absolute values

(Ta = -40 to +125°C, C=4.7uF,
VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	f_{xx}=20MHz f_x=5MHz	27	37	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	13	20	mA
					f_{xx}=16MHz f_x=16MHz	21	30	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	f_{xx}=20MHz f_x=5MHz	22		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	12		mA
					f_{xx}=16MHz f_x=16MHz	19		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	f_{xx}=20MHz f_x=5MHz	16	23	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8	12	mA
					f_{xx}=16MHz f_x=16MHz	13	20	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	f_{xx}=20MHz f_x=5MHz	12		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5		mA
					f_{xx}=16MHz f_x=16MHz	9		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4	2.8	mA
					f_{xx}=12MHz f_x=12MHz	2.0	3.7	mA
					f_{xx}=16MHz f_x=16MHz	2.4	4.2	mA
				fxx=8MHz, 8MHz Internal-OSC Note3		1.5	2.9	mA
		All peripherals stopped		PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.2		mA
					f_{xx}=12MHz f_x=12MHz	1.4		mA
					f_{xx}=16MHz f_x=16MHz	1.6		mA
				fxx=8MHz, 8MHz Internal-OSC Note3		1.1		mA

Mode	Symbol	Condition		TYP.	MAX.	Unit
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	0.4	1.1	mA
			f_{xx}=12MHz f_X=12MHz	0.7	1.5	mA
			f_{xx}=16MHz f_X=16MHz	0.8	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3		0.2	1.0	mA
SUB operating mode Note5	IDD5	RC resonator (fxt=20kHz) Note6		80	850	μA
		240 kHz Internal-OSC (SubOSC stopped)		220	1450	μA
SubIDLE mode Note3,5	IDD6	RC resonator (fxt=20kHz) Note6		40	670	μA
		240kHz Internal-OSC (SubOSC stopped)		25	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop	7.5	530	μA
			240kHz Internal-OSC working	15.5	545	μA
		POC work	240kHz Internal-OSC stop	10.5	535	μA
			240kHz Internal-OSC working	18.5	550	μA

4.8 A/D Converter

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.35	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error[Note1]	ZSE				±0.35	%FSR
Full-scale error[Note1]	FSE				±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5	LSB
Differential non-liniearity error[Note2]	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF0	V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19	pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55	kΩ
AVREF0 current	IAREF0	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF	HEX
		AVSS conversion	000		003	HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.
2. Excluding quantization error (±1/2 LSB)
3. Not tested in production.
4. Does not include input/output capacitance CIO

4.9 POC

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.10 LVI

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.11 RAM Retention Flag

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.12 Data Retention Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU		4		32	MHz
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+125	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

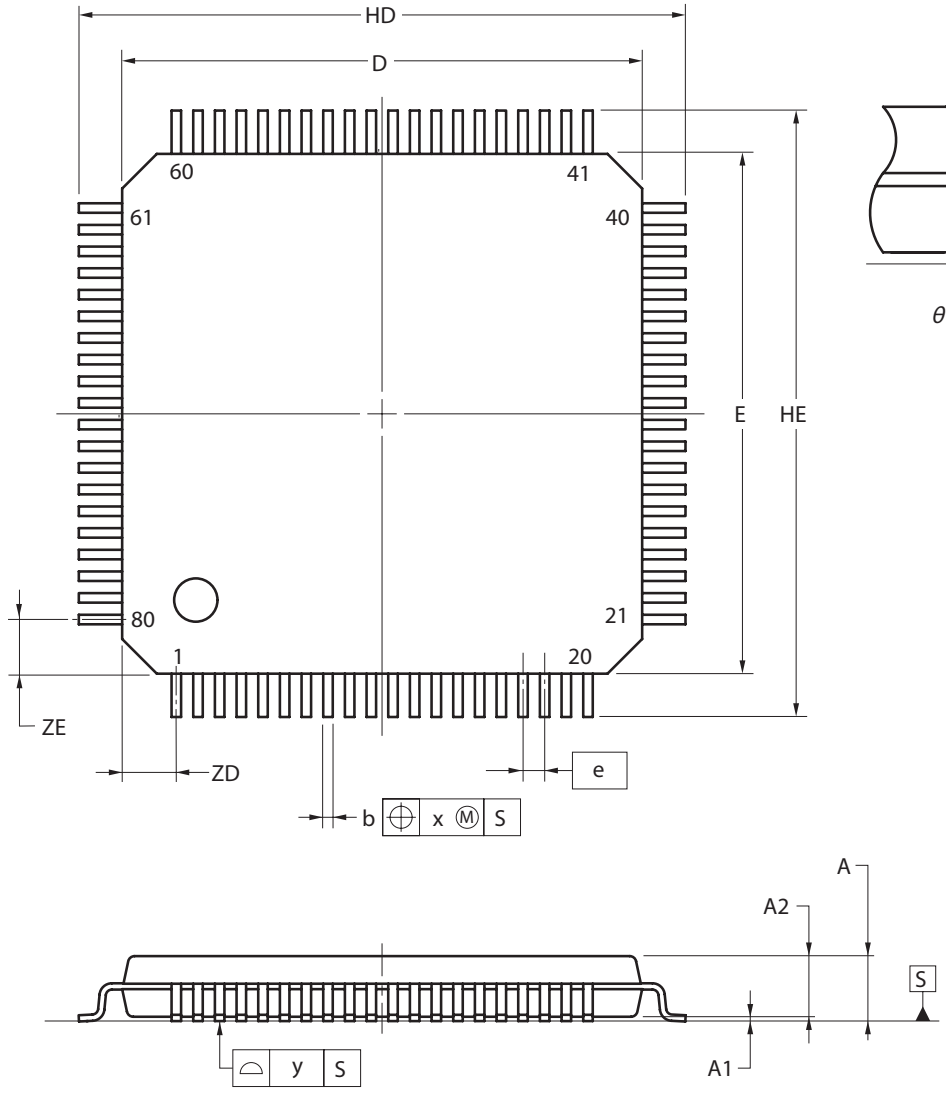
(b) Serial Writing Operation Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

5. Package

5.1 Package Dimension

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



(UNIT:mm)

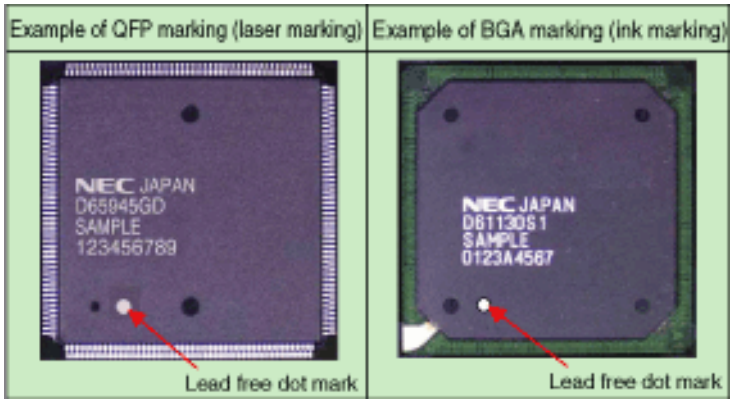
ITEM	DIMENSIONS
D	12.00 ±0.20
E	12.00 ±0.20
HD	14.00 ±0.20
HE	14.00 ±0.20
A	1.60 MAX.
A1	0.10 ±0.05
A2	1.40 ±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

5.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.
Example:



[MEMO]