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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, CSI, EBI/EMI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3378m1gja-gae-ax

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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G06.6-1A

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2. Electrical Specifications of (A)-Grade

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Absolute Maximum Ratings (TA = 25 °C)					
Parameter	Symbol	Conditions		Rating	Units
Supply voltage	VDD	VDD=EVDD,		-0.5 to +6.5	V
	EVDD	VDD=EVDD		-0.5 to +6.5	V
	AVREF0			-0.5 to +6.5	V
	VSS	VSS=EVSS=AVSS		-0.5 to +0.5	V
	EVSS	VSS=EVSS=AVSS		-0.5 to +0.5	V
	AVSS	VSS=EVSS=AVSS		-0.5 to +0.5	V
Input voltage	VI1	Pin Group 1x, 2x, 6		-0.5 to EVDD+0.5 Note1	V
	VI3	Pin Group 7		-0.5 to VRO+0.5 Note1	V
Analog input voltage	VIAN	Pin Group 4		-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x, 2x	1 pin	-4	mA
			Total	-50	mA
		Pin Group 4	1 pin	-4	mA
			Total	-20 ^{Note2}	mA
Low level output current	IOL	Pin Group 1x, 2x	1 pin	4	mA
			Total	50	mA
		Pin Group 4	1 pin	4	mA
			Total	20 ^{Note2}	mA
Operating ambient temperature	Ta	Normal operating mode		-40 to +85	°C
		Flash programming mode		-40 to +85	
Storage temperature	Tstg			-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f _{VBLK})	Supply voltage	Operating Condition
$4.0 \leq f_{xx} \leq 32\text{MHz}$ Note1	$4.0\text{V} \leq \text{VDD} \leq 5.5\text{V}$ Note2	Operation of functions is usable under following conditions: - Peripheral clock frequency $f_{XP1} \leq 32\text{MHz}$ $f_{XP2} \leq 32\text{MHz}$ - AC characteristics: - Refer to chapter '2.7 AC Characteristics' for details.
	$3.5\text{V} \leq \text{VDD} < 4.0\text{V}$ Note2	Operation of functions is usable under following conditions: - Peripheral clock frequency $f_{XP1} \leq 20\text{MHz}$ $f_{XP2} \leq 20\text{MHz}$ - AC characteristics: - Refer to chapter '2.7 AC Characteristics' for details.
	$3.3\text{V} \leq \text{VDD} < 3.5\text{V}$ Note2	Only operation of the following functions is assured: - CPU - Flash (include programming) - RAM - IO Buffer - Port - WT - WDT - INT - CLM - POC - LVI
	$3.3\text{V} \leq \text{AVREF0} \leq 5.5\text{V}$	- A/D Converter - Refer to chapter '2.8 A/D Converter' for details. - stop ADC for AVREF0 < 4.0V (ADA0CE bit =0)
$32\text{kHz} \leq f_{XT} \leq 35\text{kHz}$ (Crystal)	$3.3\text{V} \leq \text{VDD} < 5.5\text{V}$ Note2	-
$12.5\text{kHz} \leq f_{XT} \leq 27.5\text{kHz}$ Note3 (RC)		
f _{RL} (240kHz Internal-OSC)	$3.3\text{V} \leq \text{VDD} < 5.5\text{V}$ Note2	-

Notes: 1. For using SSCG please refer to '2.5.5 SSCG Characteristics' for details

2. VDD = EVDD

3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.6.2 PIN leakage current

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.		TYP.	MAX.	Unit
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	uA
			Other pins ^{Note1}			0.5	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	
			Other pins ^{Note1}			-0.5	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	
			Other pins			0.5	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	
			Other pins			-0.5	

Notes: 1. The input leakage current of FLMD0 is as follows:

High level input leakage current : 2.0uA

Low level input leakage current : -2.0uA

2.6.3 Power supply current (A-grade)

2.6.3.1 FF3 128KB μ PD70F3372, FF3 256KB μ PD70F3373

(a) Absolute values

(Ta = -40 to +85°C, C=4.7 μ F,VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1})

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =20MHz f _x =5MHz	27	37	mA
					f _{xx} =32MHz f _x =16MHz	39	51	mA
			PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz		f _{xx} =8MHz 8MHz Internal-OSC ^{Note3}	13	20	mA
					f _{xx} =16MHz f _x =16MHz	21	30	mA
		All peripherals stopped	Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =32MHz f _x =16MHz	35	47	mA
			Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =20MHz f _x =5MHz	22		mA
					f _{xx} =32MHz f _x =16MHz	32		mA
				PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	f _{xx} =8MHz 8MHz Internal-OSC ^{Note3}	12		mA
					f _{xx} =16MHz f _x =16MHz	19		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =32MHz f _x =16MHz	31		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =20MHz f _x =5MHz	16	23	mA
					f _{xx} =32MHz f _x =16MHz	24	34	mA
			PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz		f _{xx} =8MHz 8MHz Internal-OSC ^{Note3}	8	12	mA
					f _{xx} =16MHz f _x =16MHz	13	20	mA
		All peripherals stopped	Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =32MHz f _x =16MHz	20	27	mA
			Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =20MHz f _x =5MHz	12		mA
					f _{xx} =32MHz f _x =16MHz	18		mA
				PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	f _{xx} =8MHz 8MHz Internal-OSC ^{Note3}	5		mA
					f _{xx} =16MHz f _x =16MHz	9		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	f _{xx} =32MHz f _x =16MHz	17		mA

(b) Calculation formulas

(Ta = -40 to +85°C, C=4.7uF,

VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1)})

Mode	Symbol	Condition			TYP. ^{Note9}	MAX. ^{Note9}	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.98·f _{xx} +7.1	1.18·f _{xx} +13.6	mA
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.98·f _{xx} +5.5	1.18·f _{xx} +10.6	mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.90·f _{xx} +6.0	1.08·f _{xx} +12.2	mA
		All peripherals stopped	Peripheral: ff _{xx} - PRSI option: 0	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.81·f _{xx} +6.2		mA
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.83·f _{xx} +5.7		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤32MHz	0.79·f _{xx} +6.2		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff _{xx} - PRSI option: 0	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.67·f _{xx} +3.0	0.90·f _{xx} +5.4	mA
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.70·f _{xx} +1.9	1.00·f _{xx} +4.0	mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.55·f _{xx} +2.8	0.64·f _{xx} +7.0	mA
		All peripherals stopped	Peripheral: f _{xx} PRSI option: 0	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.46·f _{xx} +2.8		mA
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.44·f _{xx} +1.6		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz≤f _{xx} ≤32MHz	0.46·f _{xx} +1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) run- ning		PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7	0.092·f _{xx} +0.90	0.128·f _{xx} + 1.35	mA
		All peripherals stopped			0.035·f _{xx} +1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f _{xx} ≤16MHz ^{Note7}			0.037·f _{xx} +0.21	0.049·f _{xx} + 0.43	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).

AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.

When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

• Self-programming mode:

+ In case of PLL OFF: 7-(0.33·f_{xx}+0.1) [mA]+ In case of PLL ON: 7-(0.18·f_{xx}+3.0) [mA]

• Data flash programming mode:

+ 7-(0.18·f_{xx}/4+3.0) [mA]**3.** Main OSC is stopped.**4.** Do not use SubOSC.**5.** POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.**6.** RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.**7.** 8MHz Internal-OSC is stopped**8.** When the SSCG is running, the current value adds typ +2.5mA, max +4mA.**9.** The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.8 A/D Converter

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error ^{Note1}		4.0V≤AVREF0<5.5V		±0.15	±0.3	%FSR
Conversion time	tCONV		3.10		16	μs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2			μs
Recovery time for power down mode	tDPU		1			μs
Zero-scale error ^{Note1}	ZSE				±0.3	%FSR
Full-scale error ^{Note1}	FSE				±0.3	%FSR
Integral non-linearity error ^{Note2}	INL				±2.5	LSB
Differential non-linearity error ^{Note2}	DNL				±1.5	LSB
Analog input voltage	VIAN		AVSS		AVREF0	V
Analog input equivalent circuit capacitance ^{Note3,4}	CINA				6.19	pF
Analog input equivalent circuit resistance ^{Note3}	RINA				2.55	kΩ
AVREF0 current	IAREF0	A/D operating		4	7	mA
		A/D operation stop		1	10	uA
Conversion result when using Diagnostic function		AVREF0 conversion	3FC		3FF	HEX
		AVSS conversion	000		003	HEX

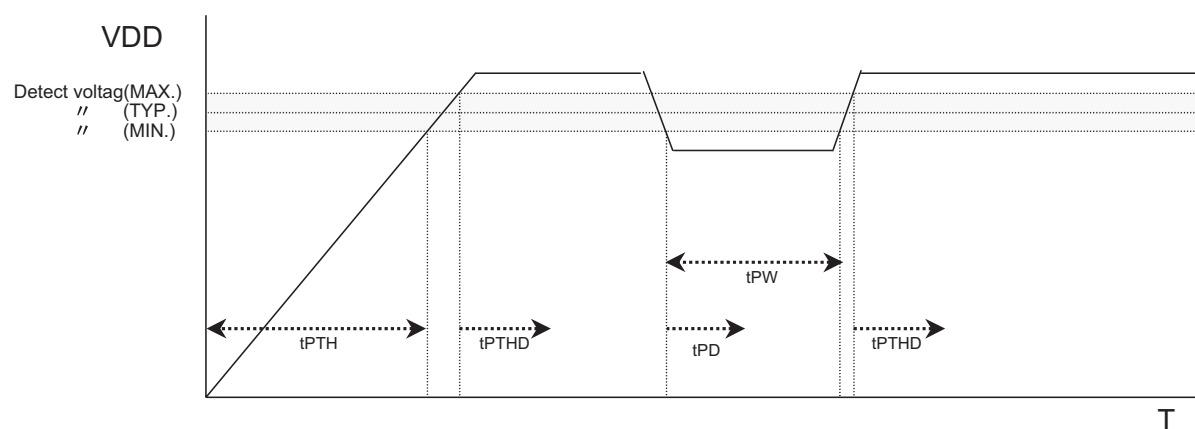
- Notes:**
1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.
 2. Excluding quantization error (±1/2 LSB)
 3. Not tested in production.
 4. Does not include input/output capacitance CIO

2.9 POC

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 ^{Note1}	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 ^{Note2}	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

- Notes:** 1. From detect voltage to release reset signal
 2. From detect voltage to occurrence of reset signal



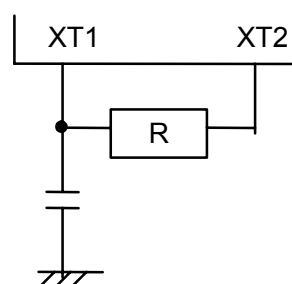
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3 User's Manual.

3.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequency ^{Note1,4}	R=390KΩ ±5% ^{Note3} , C=47pF±10% ^{Note3}	25	40	55	kHz
		Oscillation stabilization time ^{Note2}				100	μs

- Notes:**
1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.
 2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V
 3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.
 4. RC Oscillation frequency is typ. 40kHz. This clock is divided by 2 internally. In case of RC Oscillator, internal system clock frequency(fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.



3.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.4 PLL Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.5 SSCG Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.6.2 PIN leakage current

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.		TYP.	MAX.	Unit
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.4	uA
			Other pins ^{Note1}			0.8	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.4	
			Other pins ^{Note1}			-0.8	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.4	
			Other pins			0.8	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.4	
			Other pins			-0.8	

Notes: 1. The input leakage current of FLMD0 is as follows:

High level input leakage current : 4.0uA

Low level input leakage current : -4.0uA

Mode	Symbol	Condition			TYP.	MAX.	Unit	
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7	f _{xx} =5MHz f _x =5MHz	1.4	2.5	mA
					f _{xx} =12MHz f _x =12MHz	2.0	3.4	mA
					f _{xx} =16MHz f _x =16MHz	2.4	3.9	mA
				fxx=8MHz, 8MHz Internal-OSC ^{Note3}		1.5	2.6	mA
		All peripherals stopped		PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7	f _{xx} =5MHz f _x =5MHz	1.2		mA
					f _{xx} =12MHz f _x =12MHz	1.4		mA
					f _{xx} =16MHz f _x =16MHz	1.6		mA
					fxx=8MHz, 8MHz Internal-OSC ^{Note3}		1.1	
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7			f _{xx} =5MHz f _x =5MHz	0.4	0.9	mA
					f _{xx} =12MHz f _x =12MHz	0.7	1.2	mA
					f _{xx} =16MHz f _x =16MHz	0.8	1.4	mA
		fxx=8MHz, 8MHz Internal-OSC ^{Note3}			0.2	0.7	mA	
SUB operating mode ^{Note5}	IDD5	RC resonator (fxt=20kHz) ^{Note6}			80	600	μA	
		240 kHz Internal-OSC (SubOSC stopped)			220	1200	μA	
SubIDLE mode ^{Note3,}	IDD6	RC resonator (fxt=20kHz) ^{Note6}			40	420	μA	
		240kHz Internal-OSC (SubOSC stopped)			25	380	μA	
STOP mode ^{Note3,4}	IDD7	POC stop	240kHz Internal-OSC stop			7.5	280	μA
			240kHz Internal-OSC working			15.5	295	μA
		POC work	240kHz Internal-OSC stop			10.5	285	μA
			240kHz Internal-OSC working			18.5	300	μA

(b) Calculation formulas

(Ta = -40 to +110°C, C=4.7uF,

VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1)})

Mode	Symbol	Condition			TYP. ^{Note9}	MAX. ^{Note3}	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f _{xx}	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	0.98·f _{xx} +7.1	1.18·f _{xx} +13.6	mA
			PRSI option: 0	PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	0.98·f _{xx} +5.5	1.18·f _{xx} +10.6	mA
			Peripheral: f _{xx} /2	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	0.90·f _{xx} +6.0	1.08·f _{xx} +12.2	mA
		All peripherals stopped	Peripheral: f _{xx}	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	0.81·f _{xx} +6.2		mA
			PRSI option: 0	PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	0.83·f _{xx} +5.7		mA
			Peripheral: f _{xx} /2	PLL: ON 12MHz ≤ f _{xx} ≤ 32MHz	0.79·f _{xx} +6.2		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f _{xx}	PLL: ON 16MHz ≤ f _{xx} ≤ 32MHz	0.67·f _{xx} +3.0	0.90·f _{xx} +5.4	mA
			PRSI option: 0	PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	0.70·f _{xx} +1.9	1.00·f _{xx} +4.0	mA
			Peripheral: f _{xx} /2	PLL: ON 16MHz ≤ f _{xx} ≤ 32MHz	0.55·f _{xx} +2.8	0.64·f _{xx} +7.0	mA
		All peripherals stopped	Peripheral: f _{xx}	PLL: ON 16MHz ≤ f _{xx} ≤ 32MHz	0.46·f _{xx} +2.8		mA
			PRSI option: 0	PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	0.44·f _{xx} +1.6		mA
			Peripheral: f _{xx} /2	PLL: ON 16MHz ≤ f _{xx} ≤ 32MHz	0.46·f _{xx} +1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz	0.092·f _{xx} +0.90	0.128·f _{xx} +1.82	mA
		All peripherals stopped		Note7	0.035·f _{xx} +1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤ f _{xx} ≤ 16MHz Note7			0.037·f _{xx} +0.21	0.049·f _{xx} +0.63	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).

AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.

When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:

+ In case of PLL OFF: 7-(0.33·f_{xx}+0.1) [mA]+ In case of PLL ON: 7-(0.18·f_{xx}+3.0) [mA]

- Data flash programming mode:

+ 7-(0.18·f_{xx}/4+3.0) [mA]**3.** Main OSC is stopped.**4.** Do not use SubOSC.**5.** POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.**6.** RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.**7.** 8MHz Internal-OSC is stopped**8.** When the SSCG is running, the current value adds typ +2.5mA, max +4mA.**9.** The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

(b) Calculation formulas

(Ta = -40 to +125°C, C=4.7uF,

VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V^{Note1)})

Mode	Symbol	Condition			TYP. ^{Note9}	MAX. ^{Note9}	Unit	
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f _{xx} PRSI option: 0	PLL: ON 12MHz≤f _{xx} ≤24MHz	0.98·f _{xx} +7.1	1.18·f _{xx} +13.6	mA	
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.98·f _{xx} +5.5	1.18·f _{xx} +10.6	mA	
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤24MHz	0.90·f _{xx} +6.0	1.08·f _{xx} +12.2	mA	
		All peripherals stopped		Peripheral: f _{xx} - PRSI option: 0	PLL: ON 12MHz≤f _{xx} ≤24MHz	0.81·f _{xx} +6.2		mA
					PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.83·f _{xx} +5.7		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 12MHz≤f _{xx} ≤24MHz	0.79·f _{xx} +6.2		mA	
HALT mode Note8	IDD2	All peripherals running	Peripheral: f _{xx} - PRSI option: 0	PLL: ON 16MHz≤f _{xx} ≤24MHz	0.67·f _{xx} +3.0	0.90·f _{xx} +5.4	mA	
				PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.70·f _{xx} +1.9	1.00·f _{xx} +4.0	mA	
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz≤f _{xx} ≤24MHz	0.55·f _{xx} +2.8	0.64·f _{xx} +7.0	mA	
		All peripherals stopped		Peripheral: f _{xx} PRSI option: 0	PLL: ON 16MHz≤f _{xx} ≤24MHz	0.46·f _{xx} +2.8		mA
					PLL: OFF 4MHz≤f _{xx} ≤16MHz	0.44·f _{xx} +1.6		mA
			Peripheral: f _{xx} /2 PRSI option: 1	PLL: ON 16MHz≤f _{xx} ≤24MHz	0.46·f _{xx} +1.8		mA	
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f _{xx} ≤16MHz Note7	0.092·f _{xx} +0.90	0.128·f _{xx} + 2.12	mA	
		All peripherals stopped			0.035·f _{xx} +1.01		mA	
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f _{xx} ≤16MHz ^{Note7}				0.037·f _{xx} +0.21	0.049·f _{xx} + 0.88	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).

AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.

When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
 - + In case of PLL OFF: 7-(0.33·f_{xx}+0.1) [mA]
 - + In case of PLL ON: 7-(0.18·f_{xx}+3.0) [mA]
- Data flash programming mode:
 - + 7-(0.18·f_{xx}+4+3.0) [mA]

3. Main OSC is stopped.

4. Do not use SubOSC.

5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.

6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.

7. 8MHz Internal-OSC is stopped

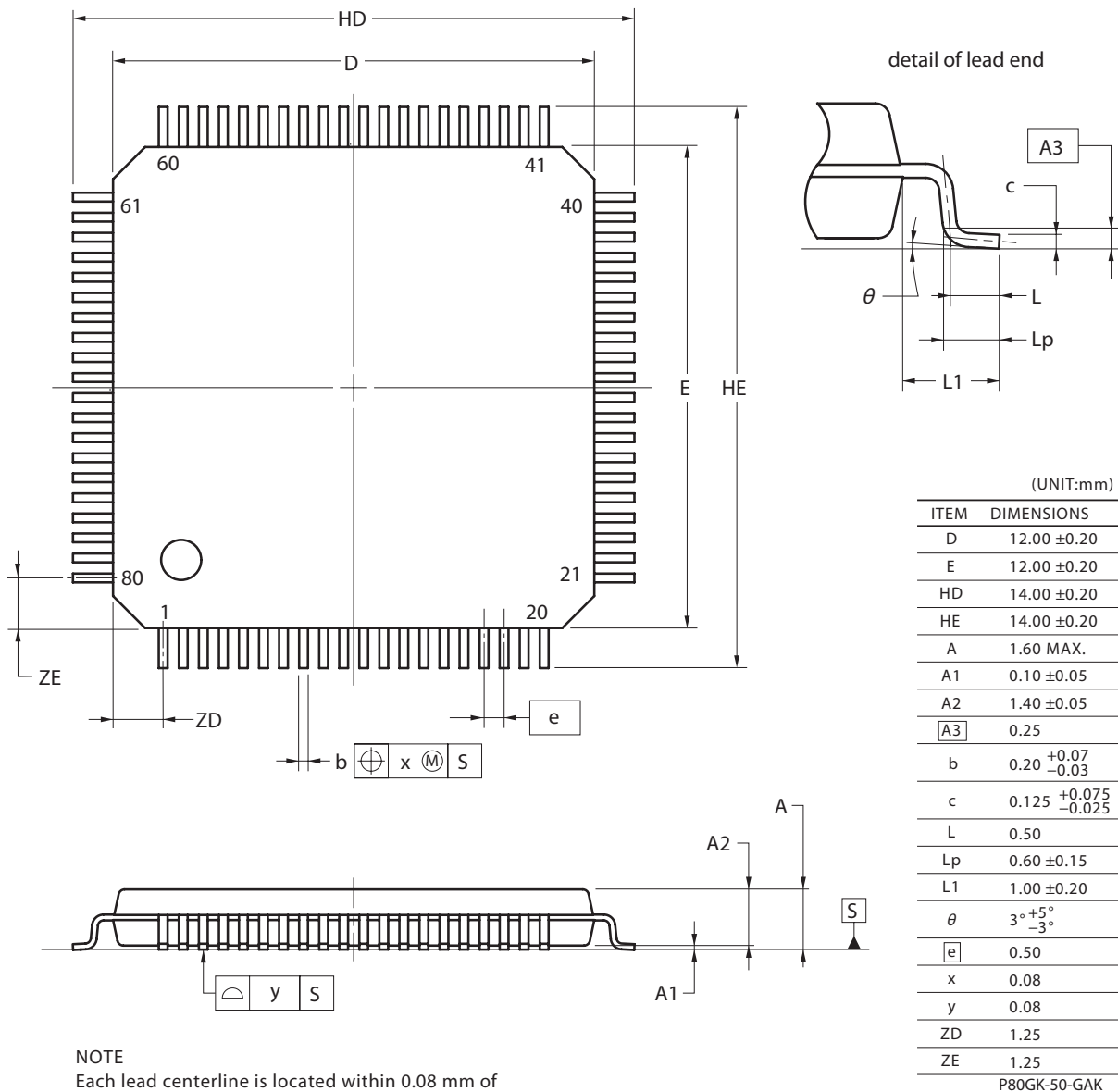
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.

9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

5. Package

5.1 Package Dimension

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



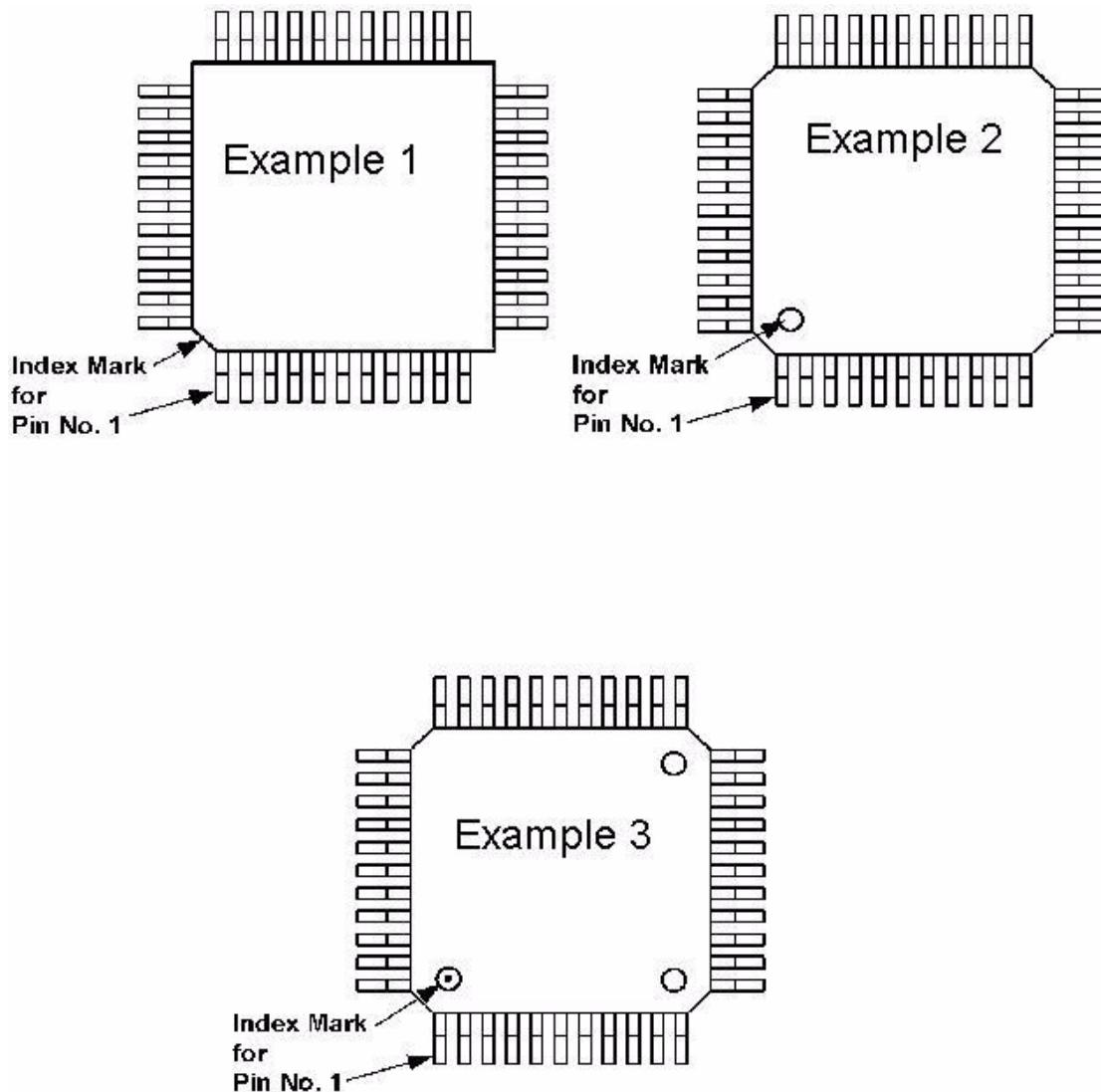
NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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5.2 Product Marking

5.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 5.2.2 "Identification of Lead-Free Products" on page 53.

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