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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk21dn512avlk5

Part identification

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = -40 to 105 • C = -40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz • 18 = 180 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

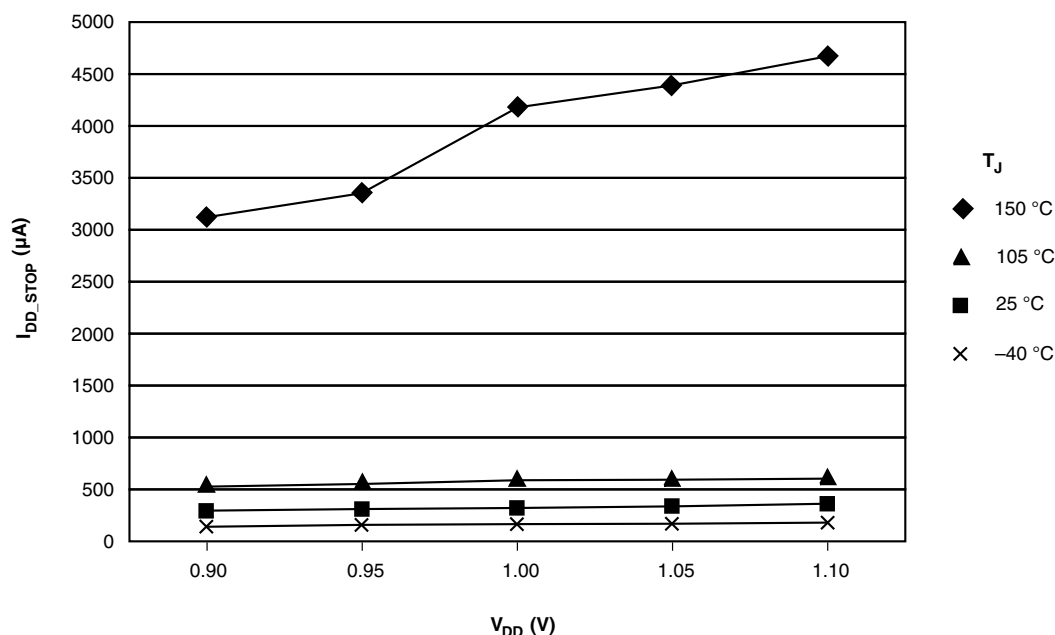
MK21DX128VLK5

2.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3		V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V_{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

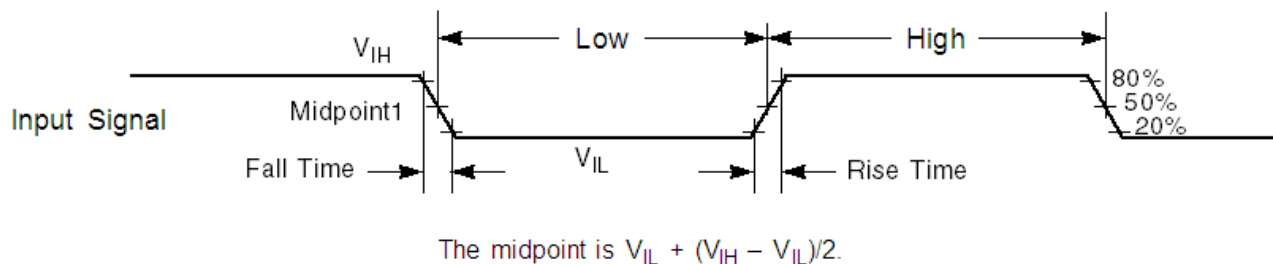


Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{CIO}	I/O pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-3	—	mA	1
		—	+3		

Table continues on the next page...

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — high drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{ mA}$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{ mA}$	—	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin)				
	• @ full temperature range	—	1.0	μA	1
	• @ 25 °C	—	0.1	μA	
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I _{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R _{PU}	Internal pullup resistors	22	50	kΩ	2
R _{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at V_{input} = V_{SS}
3. Measured at V_{input} = V_{DD}

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$	— — — —	13 7 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) • Slew disabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$ • Slew enabled • $1.71 \leq V_{DD} \leq 2.7V$ • $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.

3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	35	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	29	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	19	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8	°C/W	5

Table continues on the next page...

Peripheral operating requirements and behaviors

Board type	Symbol	Description	80 LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 JTAG electricals

Table 12. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns

Table continues on the next page...

Table 15. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}^5	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. $V_{DD}=3.3$ V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that—it remains within the limits of DCO input clock frequency when divided by FRDIV.
3. Proper PC board layout procedures must be followed to achieve specifications.

- Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	$M\Omega$
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

- When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications

Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

- Proper PC board layout procedures must be followed to achieve specifications.
- This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
- The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 19. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp\text{gm}4}$	Longword Program high-voltage time	—	7.5	18	μs	
$t_{h\text{versscr}}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{h\text{versblk}256\text{k}}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 20. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{rd}1\text{blk}64\text{k}}$	Read 1s Block execution time • 64 KB data flash	—	—	0.9	ms	
$t_{\text{rd}1\text{blk}256\text{k}}$	• 256 KB program flash	—	—	1.7	ms	
$t_{\text{rd}1\text{sec}2\text{k}}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
$t_{\text{rd}r\text{src}}$	Read Resource execution time	—	—	30	μs	1
$t_{\text{pgm}4}$	Program Longword execution time	—	65	145	μs	
$t_{\text{ersblk}64\text{k}}$	Erase Flash Block execution time • 64 KB data flash	—	58	580	ms	2
$t_{\text{ersblk}256\text{k}}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{\text{pgmsec}512}$	Program Section execution time • 512 bytes flash	—	2.4	—	ms	
$t_{\text{pgmsec}1\text{k}}$	• 1 KB flash	—	4.7	—	ms	
$t_{\text{pgmsec}2\text{k}}$	• 2 KB flash	—	9.3	—	ms	
$t_{\text{rd}1\text{all}}$	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
t_{pgmonce}	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	250	2000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1

Table continues on the next page...

Table 24. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C_{rate}	ADC conversion rate	≤ 13 -bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had $< 8 \Omega$ analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

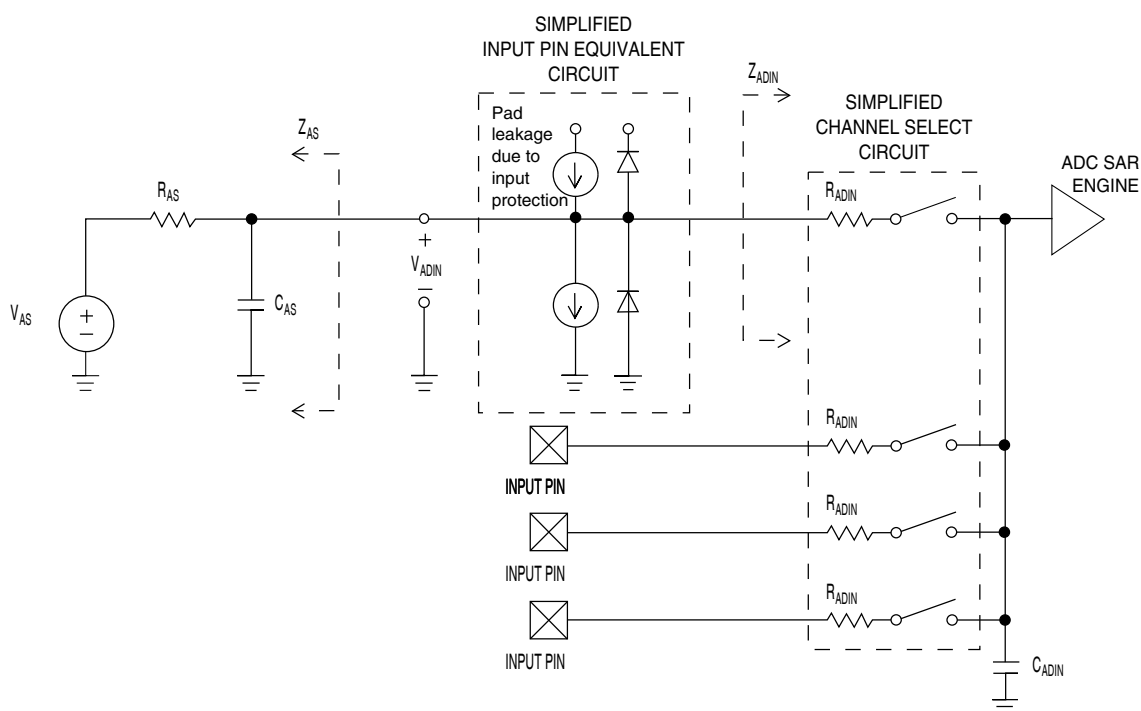


Figure 9. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 25. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	16-bit modes ≤13-bit modes	— —	-1 to 0 —	— ±0.5	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9 12.2 11.4	14.5 13.8 13.9 13.1	— — — —	bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7

Table continues on the next page...

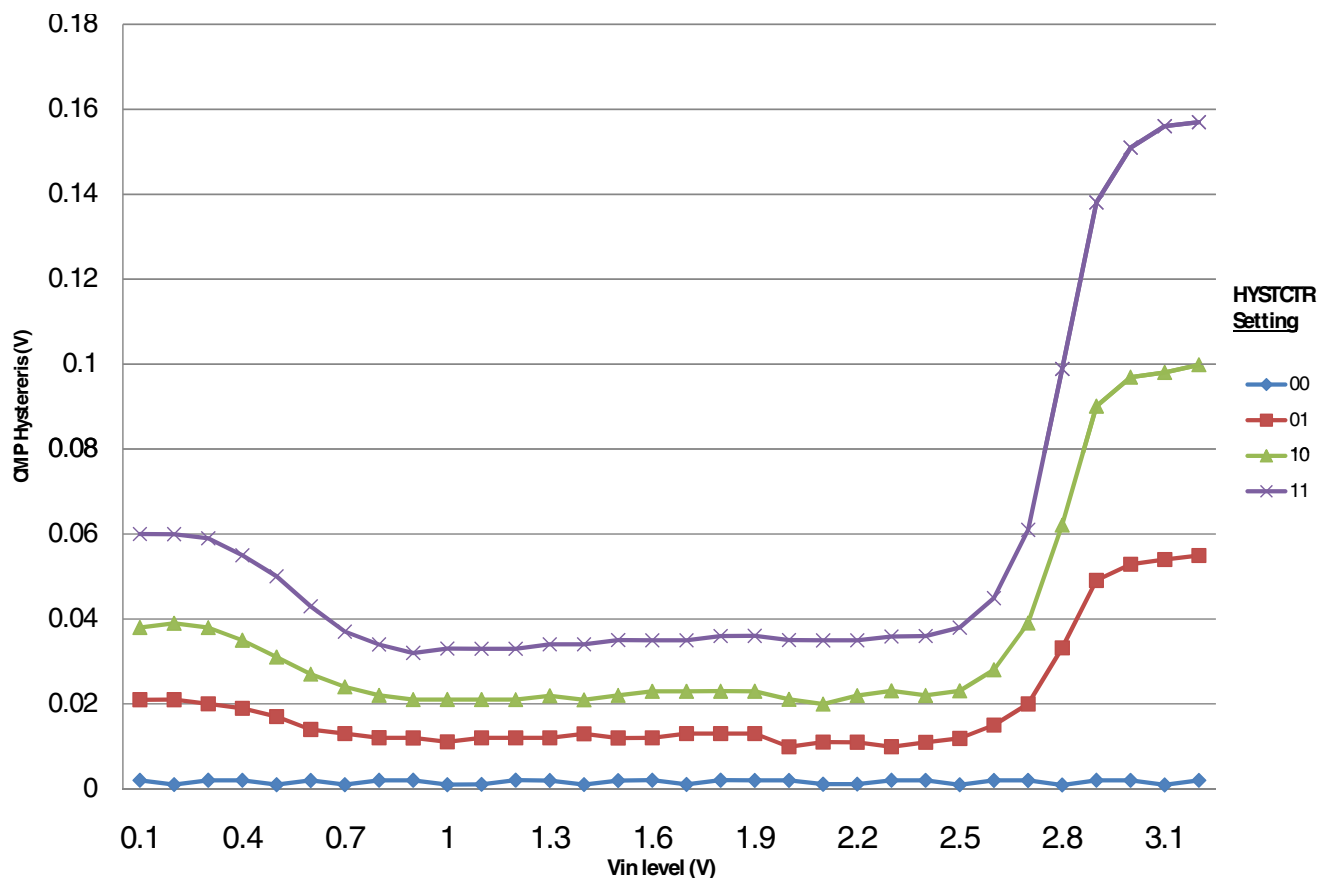


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.7 Timers

See [General switching specifications](#).

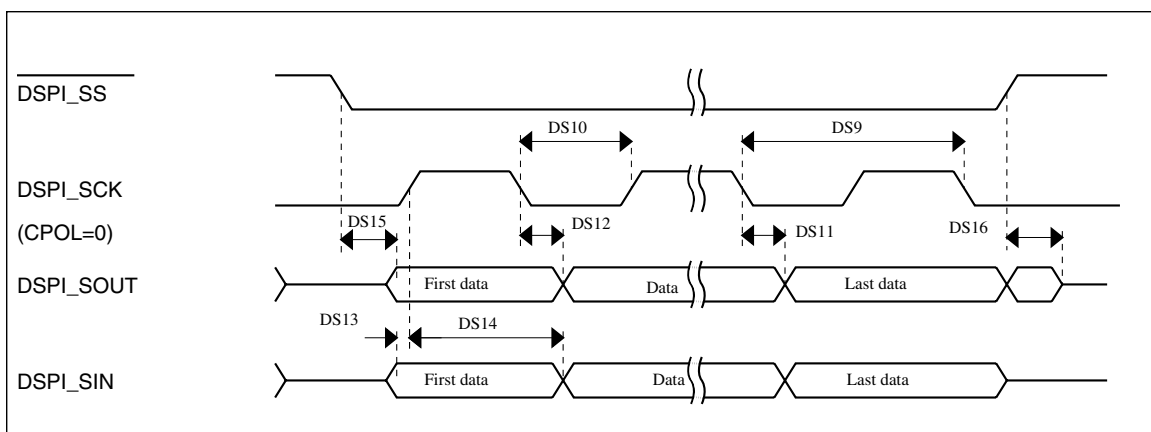
6.8 Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org.

Table 30. Slave mode DSPI timing (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns


Figure 15. DSPI classic SPI timing — slave mode

6.8.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 31. Master mode DSPI timing (full voltage range)

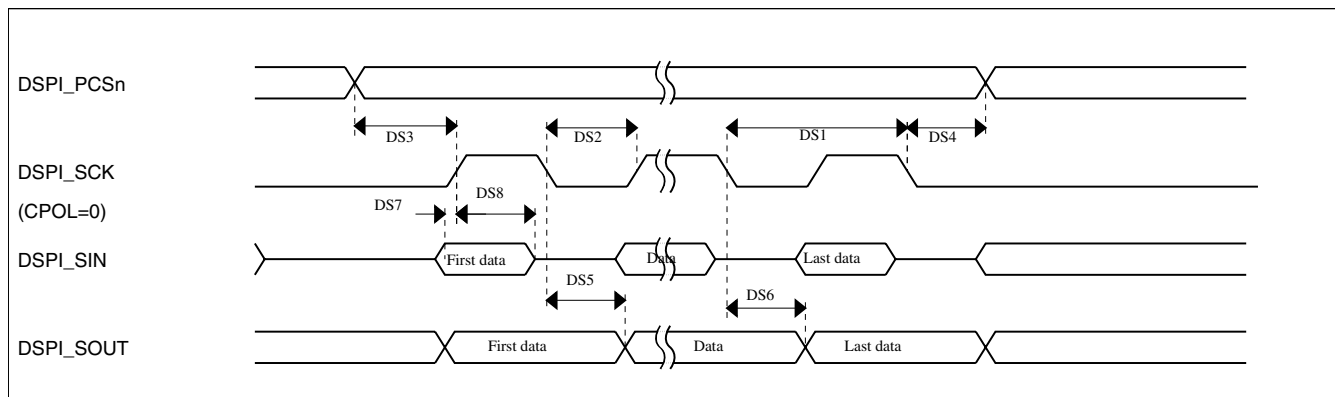
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2

Table continues on the next page...

Table 31. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].


Figure 16. DSPI classic SPI timing — master mode
Table 32. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

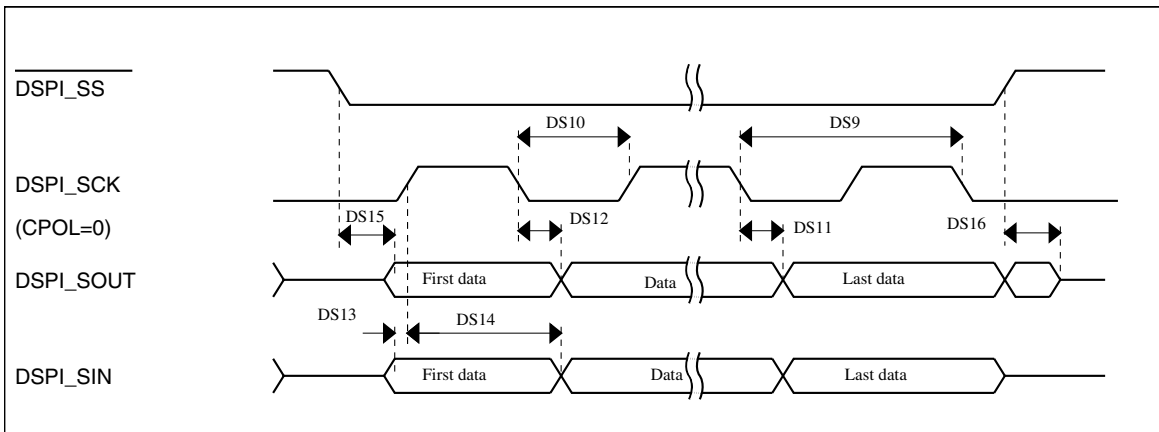


Figure 17. DSPI classic SPI timing — slave mode

6.8.6 I²C switching specifications

See [General switching specifications](#).

6.8.7 UART switching specifications

See [General switching specifications](#).

6.8.8 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 33. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns

Table continues on the next page...

Table 33. I2S/SAI master mode timing (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

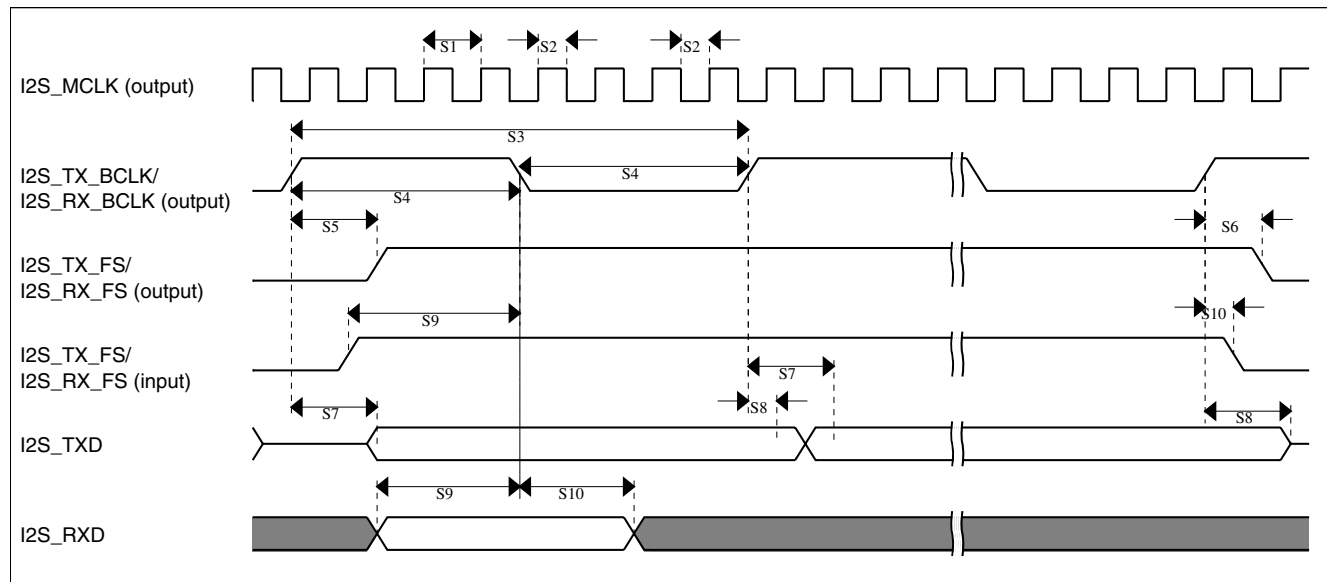


Figure 18. I2S/SAI timing — master modes

Table 34. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

K12, K21, and K22 devices and are not present on K10 and K20 devices.

- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

80 LQFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
2	ADC0_SE11	ADC0_SE11	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	I2C1_SCL	SPI1_SIN	
3	ADC0_DP1	ADC0_DP1	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
4	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	
5	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX		TRACE_D0			
6	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
7	VDD	VDD								
8	VSS	VSS								
9	USB0_DP	USB0_DP								
10	USB0_DM	USB0_DM								
11	VOUT33	VOUT33								
12	VREGIN	VREGIN								
13	ADC0_DP0	ADC0_DP0								
14	ADC0_DM0	ADC0_DM0								
15	ADC0_DP3	ADC0_DP3								
16	ADC0_DM3	ADC0_DM3								
17	VDDA	VDDA								
18	VREFH	VREFH								
19	VREFL	VREFL								

80 LQFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
52	DISABLED		PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	FTM_CLKIN1	
53	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK				
54	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS				
55	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1		
56	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
57	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
58	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
59	VSS	VSS								
60	VDD	VDD								
61	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
62	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	FTM0_CH2	
63	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
64	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS				
65	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
66	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_BCLK		FTM2_FLT0		
67	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS				
68	DISABLED		PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1				
69	DISABLED		PTC12							
70	DISABLED		PTC13							
71	DISABLED		PTC16		UART3_RX					
72	DISABLED		PTC17		UART3_TX					
73	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b					
74	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
75	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	I2C0_SCL				
76	DISABLED		PTD3	SPI0_SIN	UART2_TX	I2C0_SDA				
77	ADC0_SE21	ADC0_SE21	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
78	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b		
79	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
80	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		