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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 20x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-FQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk21dx256vlk5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



reminology and guidelines

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- Operating ratings apply during operation of the chip.
- Handling ratings apply when the chip is not powered.







3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	٥C
V _{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.



4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

- 1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
- 2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.
- 3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current		155	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3		V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
V _{USB0_DP}	USB0_DP input voltage	-0.3	3.63	V
V _{USB0_DM}	USB0_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General



5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + $(V_{IH} - V_{IL})/2$.

Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
V _{BAT}	RTC battery supply voltage	1.71	3.6	V	
V _{IH}	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	_	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	—	$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I _{ICIO}	I/O pin DC injection current — single pin				1
	 V_{IN} < V_{SS}-0.3V (Negative current injection) 			mA	
	 V_{IN} > V_{DD}+0.3V (Positive current injection) 	-3	—		
		—	+3		

Table continues on the next page ...



General

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.			μs	1
	 1.71 V/(V_{DD} slew rate) ≤ 300 μs 	—	300		
	 1.71 V/(V_{DD} slew rate) > 300 µs 	—	1.7 V / (V _{DD} slew rate)		
	VLLS0 → RUN	—	135	μs	
	• VLLS1 → RUN		135	μs	
	• VLLS2 \rightarrow RUN	—	85	μs	
	 VLLS3 → RUN 	_	85	μs	
	• LLS → RUN	_	6	μs	
	 VLPS → RUN 		5.2	μs	
	• STOP \rightarrow RUN	_	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	—	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8 V	_	12.98	14	mA	
	• @ 3.0 V	—	12.93	13.8	mA	

Table continues on the next page...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8 V		17.04	10.3	mΔ	
	• @ 3.0 V		17.04	10.0		
	• @ 25°C		17.01	18.9	mA	
	• @ 125°C		19.8	21.3	mA	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled		7.95	9.5	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled		5.88	7.4	mA	5
I _{DD_STOP}	Stop mode current at 3.0 V	_	320	436	μA	
	• @ -40 to 25°C • @ 50°C		360	489		
	• @ 70°C		410	620		
	• @ 105°C		610	1100		
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled		754		μΑ	6
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled		1.1		mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V	_	437	_	μA	8
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V		7.33	24.2	μΑ	
	• @ -40 to 25°C • @ 50°C		14	32		
	• @ 70°C		28	48		
			110	280		
I _{DD_LLS}	Low leakage stop mode current at 3.0 V • @ -40 to 25°C	_	3.14	4.8	μΑ	
	• @ 50°C		6.48	28.3		
	• @ 70°C • @ 105°C		13.85	44.6		
			55.53	71.3		
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V	_	2.19	3.4	μΑ	
	• @ -40 to 25°C • @ 50°C		4.35	4.35		
	• @ 70°C		8.92	24.6		
	• @ 105°C		35.33	45.3		
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V		1.77	3.1	μΑ	
	• @ -40 to 25°C • @ 50°C		2.81	13.8		
	• @ 70°C		5.20	22.3		
			19.88	34.2		

Table 6.	Power	consumption	operating	behaviors	(continued)
		•••••••••••••••••••••••••••••••••••••••	•p•i.a.iiig		(

Table continues on the next page...



Symbol	Description	Min.	Max.	Unit	Notes
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f _{I2S_MCLK}	I2S master clock	_	12.5	MHz	
f _{I2S_BCLK}	I2S bit clock		4	MHz	

Table 9. Device clock specifications (continued)

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	_	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	_	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	_	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength)				4
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	13	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	7	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	24	ns	

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.

6.3.1 MCG specifications Table 14. MCG specifications

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f _{ints_ft}	Internal reference factory trimmed at	frequency (slow clock) — nominal VDD and 25 °C	_	32.768	—	kHz	
f _{ints_t}	Internal reference trimmed	frequency (slow clock) — user	31.25		39.0625	kHz	
Δ _{fdco_res_t}	Resolution of trimr frequency at fixed using SCTRIM and	ned average DCO output voltage and temperature — d SCFTRIM	_	± 0.3	± 0.6	%f _{dco}	1
$\Delta f_{dco_res_t}$	Resolution of trimr frequency at fixed using SCTRIM onl	ned average DCO output voltage and temperature — y	_	± 0.2	± 0.5	%f _{dco}	1
Δf _{dco_t}	Total deviation of t frequency over vo	trimmed average DCO output Itage and temperature	—	+0.5/-0.7	± 2	%f _{dco}	1, 2
∆f _{dco_t}	Total deviation of t frequency over fixe range of 0–70°C	trimmed average DCO output ed voltage and temperature	_	± 0.3	±1	%f _{dco}	1, 2
f _{intf_ft}	Internal reference factory trimmed at	frequency (fast clock) — nominal VDD and 25°C	_	4	—	MHz	
f _{intf_t}	Internal reference trimmed at nomina	frequency (fast clock) — user al VDD and 25 °C	3	_	5	MHz	
f _{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f _{ints_t}	_	_	kHz	
f _{loc_high}	Loss of external cl RANGE = 01, 10,	ock minimum frequency — or 11	(16/5) x f _{ints_t}	_	_	kHz	
		FI	ĹĹ				
f _{fll_ref}	FLL reference free	luency range	31.25	_	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll ref}	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	-
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll ref}	80	83.89	100	MHz	-
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00)		23.99		MHz	5, 6
		Mid range (DRS=01) 1464 × f _{fll_ref}		47.97		MHz	
		Mid-high range (DRS=10) 2197 × f _{fll ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	_	95.98	_	MHz	

Table continues on the next page ...



4. Crystal startup time is defined as the time between oscillator being enabled and OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	—	3.6	V
R _F	Internal feedback resistor		100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32		5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation	_	0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications Table 18. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t _{start}	Crystal start-up time	—	1000	—	ms	1
V _{ec_extal32}	Externally provided input clock amplitude	700	—	V _{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The
oscillator remains enabled and XTAL32 must be left unconnected.

3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Swap Control execution time					
t _{swapx01}	control code 0x01	_	200	_	μs	
t _{swapx02}	control code 0x02	_	70	150	μs	
t _{swapx04}	control code 0x04	_	70	150	μs	
t _{swapx08}	control code 0x08		—	30	μs	
	Program Partition for EEPROM execution time					
t _{pgmpart64k}	• 64 KB FlexNVM	_	138	_	ms	
	Set FlexRAM Function execution time:					
t _{setramff}	Control Code 0xFF	_	70	_	μs	
t _{setram32k}	32 KB EEPROM backup	_	0.8	1.2	ms	
t _{setram64k}	64 KB EEPROM backup		1.3	1.9	ms	
	Byte-write to FlexRAM	for EEPROM	l operation	Į	1	1
t _{eewr8bers}	Byte-write to erased FlexRAM location execution time	_	175	260	μs	3
	Byte-write to FlexRAM execution time:					
t _{eewr8b32k}	32 KB EEPROM backup	_	385	1800	μs	
t _{eewr8b64k}	64 KB EEPROM backup		475	2000	μs	
	Word-write to FlexRAM	for EEPRON	A operation		1	
t _{eewr16bers}	Word-write to erased FlexRAM location execution time	_	175	260	μs	
	Word-write to FlexRAM execution time:					
t _{eewr16b32k}	32 KB EEPROM backup	_	385	1800	μs	
t _{eewr16b64k}	64 KB EEPROM backup		475	2000	μs	
	Longword-write to FlexRA	M for EEPR	OM operation	ו		
t _{eewr32bers}	Longword-write to erased FlexRAM location execution time		360	540	μs	
	Longword-write to FlexRAM execution time:					
t _{eewr32b32k}	32 KB EEPROM backup	_	630	2050	μs	
t _{eewr32b64k}	64 KB EEPROM backup	_	810	2250	μs	

Table 20. Flash command timing specifications (continued)

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.



6.4.1.3 Flash high voltage current behaviors Table 21. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
	Prograi	n Flash				
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2
	Data	Flash				
t _{nvmretd10k}	Data retention after up to 10 K cycles	5	50	—	years	
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	—	years	
n _{nvmcycd}	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM a	s EEPROM	•	•	•	
t _{nvmretee100}	Data retention up to 100% of write endurance	5	50	—	years	
t _{nvmretee10}	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
n _{nvmwree16}	 EEPROM backup to FlexRAM ratio = 16 	35 K	175 K	_	writes	
n _{nvmwree128}	 EEPROM backup to FlexRAM ratio = 128 	315 K	1.6 M	_	writes	
n _{nvmwree512}	 EEPROM backup to FlexRAM ratio = 512 	1.27 M	6.4 M	_	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	_	writes	

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40 °C \leq T_i \leq °C.

3. Write endurance represents the number of writes to each FlexRAM location at -40 °C ≤Tj ≤ °C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.



Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging	20.000		818.330	Ksps	
		Continuous conversions enabled, subsequent conversion time					
C _{rate}	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37.037		461.467	Ksps	
		Continuous conversions enabled, subsequent conversion time					

Table 24. 16-bit ADC operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 9. ADC input impedance equivalency diagram





Typical ADC 16-bit Differential ENOB vs ADC Clock 100Hz, 90% FS Sine Input





Typical ADC 16-bit Single-Ended ENOB vs ADC Clock 100Hz, 90% FS Sine Input

Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode



6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t _{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t _{SCK} /2) – 2	(t _{SCK} /2) + 2	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2		ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

 Table 29. Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 14. DSPI classic SPI timing — master mode

Table 30. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t _{BUS}	_	ns

Table continues on the next page...



Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCS <i>n</i> invalid delay	(t _{BUS} x 2) – 4	_	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	_	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0		ns	

 Table 31.
 Master mode DSPI timing (full voltage range) (continued)

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 16. DSPI classic SPI timing — master mode

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	_	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t _{BUS}		ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2		ns
DS14	DSPI_SCK to DSPI_SIN input hold	7		ns
DS15	DSPI_SS active to DSPI_SOUT driven		19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		19	ns







6.8.6 I²C switching specifications

See General switching specifications.

6.8.7 UART switching specifications

See General switching specifications.

6.8.8 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	_	15	ns

Table 33. I2S/SAI master mode timing

Table continues on the next page...





Figure 20. I2S/SAI timing — master modes

Table 36. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	-	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	_	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





Figure 21. I2S/SAI timing — slave modes

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number				
80-pin LQFP	98ASS23174W				

8 Pinout

8.1 K21 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

• The analog input signals ADC0_SE10, ADC0_SE11, ADC0_DP1, and ADC0_DM1 are available only for K11,

K12, K21, and K22 devices and are not present on K10 and K20 devices.

- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0_CH2 signal on PTC5/LLWU_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0_SCL signal on PTD2/LLWU_P13 and I2C0_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

80 LQFP	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
2	ADC0_SE11	ADC0_SE11	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	12C1_SCL	SPI1_SIN	
3	ADC0_DP1	ADC0_DP1	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
4	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	
5	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX		TRACE_D0			
6	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
7	VDD	VDD								
8	VSS	VSS								
9	USB0_DP	USB0_DP								
10	USB0_DM	USB0_DM								
11	VOUT33	VOUT33								
12	VREGIN	VREGIN								
13	ADC0_DP0	ADC0_DP0								
14	ADC0_DM0	ADC0_DM0								
15	ADC0_DP3	ADC0_DP3								
16	ADC0_DM3	ADC0_DM3								
17	VDDA	VDDA								
18	VREFH	VREFH								
19	VREFL	VREFL								



rmout

80 LQFP	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
52	DISABLED		PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	FTM_CLKIN1	
53	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK				
54	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS				
55	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1		
56	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
57	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
58	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
59	VSS	VSS								
60	VDD	VDD								
61	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
62	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	FTM0_CH2	
63	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
64	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS				
65	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
66	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_BCLK		FTM2_FLT0		
67	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS				
68	DISABLED		PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1				
69	DISABLED		PTC12							
70	DISABLED		PTC13							
71	DISABLED		PTC16		UART3_RX					
72	DISABLED		PTC17		UART3_TX					
73	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b					
74	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
75	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	12C0_SCL				
76	DISABLED		PTD3	SPI0_SIN	UART2_TX	I2C0_SDA				
77	ADC0_SE21	ADC0_SE21	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
78	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b		
79	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
80	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		