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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, LCD, POR, WDT
Number of I/O	42
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc11d14fbd100-302

3. Applications

- Industrial applications (e.g. thermostats)
- White goods
- Human interface
- Sensors

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC11D14FBD100/302	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash	Total SRAM	Power profiles	UART RS-485	I^2C/ Fast+	SPI	ADC channels	Package
LPC11D14FBD100/302	32 kB	8 kB	yes	1	1	2	8	LQFP100

5. Block diagram

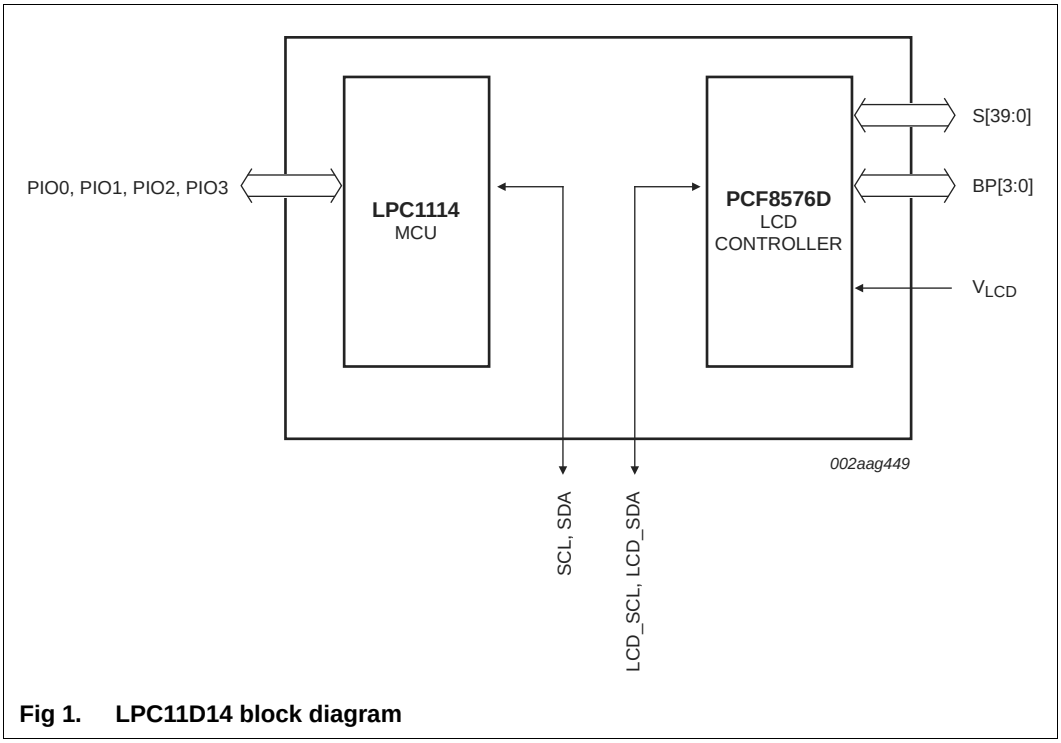


Fig 1. LPC11D14 block diagram

Table 3. LPC11D14 pin description table (LQFP100 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	99[3]	no	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	100[3]	no	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	1[3]	no	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	12[3]	no	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	20[3]	no	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	84[5]	no	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	96[5]	no	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0 to PIO2_11			I/O		**Port 2 —** Port 2 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 2 pins depends on the function selected through the IOCONFIG register block.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	5[3]	no	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
			I/O	-	**SSEL1 —** Slave Select for SPI1.
PIO2_1/$\overline{\text{DSR}}$/SCK1	16[3]	no	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
			I/O	-	**SCK1 —** Serial clock for SPI1.
PIO2_2/$\overline{\text{DCD}}$/MISO1	80[3]	no	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
			I/O	-	**MISO1 —** Master In Slave Out for SPI1.
PIO2_3/$\overline{\text{RI}}$/MOSI1	92[3]	no	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
			I/O	-	**MOSI1 —** Master Out Slave In for SPI1.
PIO2_4	22[3]	no	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin.
PIO2_5	23[3]	no	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin.
PIO2_6	4[3]	no	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
PIO2_7	14[3]	no	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
PIO2_8	15[3]	no	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
PIO2_9	27[3]	no	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.

Table 3. LPC11D14 pin description table (LQFP100 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO2_10	28[3]	no	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0	85[3]	no	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SPI0.
PIO3_0 to PIO3_5			I/O		**Port 3 —** Port 3 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 3 pins depends on the function selected through the IOCONFIG register block. Pins PIO3_6 to PIO3_11 are not available.
PIO3_0/$\overline{\text{DTR}}$	90[3]	no	I/O	I; PU	**PIO3_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_1/$\overline{\text{DSR}}$	91[3]	no	I/O	I; PU	**PIO3_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
PIO3_2/$\overline{\text{DCD}}$	97[3]	no	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
PIO3_3/$\overline{\text{RI}}$	2[3]	no	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
PIO3_4	21[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin.
PIO3_5	24[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin.
V_{DD}	11; 98	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	9[6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	10[6]	-	O	-	Output from the oscillator amplifier.
V_{SS}	8; 95	-	I	-	Ground.
LCD display pins					
S0	46	-	O	V_{LCD}[7]	LCD segment output.
S1	47	-	O	V_{LCD}[7]	LCD segment output.
S2	48	-	O	V_{LCD}[7]	LCD segment output.
S3	49	-	O	V_{LCD}[7]	LCD segment output.
S4	50	-	O	V_{LCD}[7]	LCD segment output.
S5	51	-	O	V_{LCD}[7]	LCD segment output.
S6	52	-	O	V_{LCD}[7]	LCD segment output.
S7	53	-	O	V_{LCD}[7]	LCD segment output.
S8	54	-	O	V_{LCD}[7]	LCD segment output.
S9	55	-	O	V_{LCD}[7]	LCD segment output.
S10	56	-	O	V_{LCD}[7]	LCD segment output.
S11	57	-	O	V_{LCD}[7]	LCD segment output.
S12	58	-	O	V_{LCD}[7]	LCD segment output.
S13	59	-	O	V_{LCD}[7]	LCD segment output.
S14	60	-	O	V_{LCD}[7]	LCD segment output.
S15	61	-	O	V_{LCD}[7]	LCD segment output.
S16	62	-	O	V_{LCD}[7]	LCD segment output.

Table 3. LPC11D14 pin description table (LQFP100 package) *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
S17	63	-	O	V_{LCD}[7]	LCD segment output.
S18	64	-	O	V_{LCD}[7]	LCD segment output.
S19	65	-	O	V_{LCD}[7]	LCD segment output.
S20	66	-	O	V_{LCD}[7]	LCD segment output.
S21	67	-	O	V_{LCD}[7]	LCD segment output.
S22	68	-	O	V_{LCD}[7]	LCD segment output.
S23	69	-	O	V_{LCD}[7]	LCD segment output.
S24	70	-	O	V_{LCD}[7]	LCD segment output.
S25	71	-	O	V_{LCD}[7]	LCD segment output.
S26	72	-	O	V_{LCD}[7]	LCD segment output.
S27	73	-	O	V_{LCD}[7]	LCD segment output.
S28	74	-	O	V_{LCD}[7]	LCD segment output.
S29	75	-	O	V_{LCD}[7]	LCD segment output.
S30	76	-	O	V_{LCD}[7]	LCD segment output.
S31	77	-	O	V_{LCD}[7]	LCD segment output.
S32	78	-	O	V_{LCD}[7]	LCD segment output.
S33	79	-	O	V_{LCD}[7]	LCD segment output.
S34	29	-	O	V_{LCD}[7]	LCD segment output.
S35	30	-	O	V_{LCD}[7]	LCD segment output.
S36	31	-	O	V_{LCD}[7]	LCD segment output.
S37	32	-	O	V_{LCD}[7]	LCD segment output.
S38	33	-	O	V_{LCD}[7]	LCD segment output.
S39	34	-	O	V_{LCD}[7]	LCD segment output.
BP0	42	-	O	V_{LCD}[7]	LCD backplane output.
BP1	44	-	O	V_{LCD}[7]	LCD backplane output.
BP2	43	-	O	V_{LCD}[7]	LCD backplane output.
BP3	45	-	O	V_{LCD}[7]	LCD backplane output.
LCD_SDA	35	-	I/O	[7]	I^2C-bus serial data input/output.
LCD_SCL	36	-	I/O	[7]	I^2C-bus serial clock input.
$\overline{SYNC}$	37	-	I/O	[7]	Cascade synchronization input/output.
CLK	38	-	I/O	[7]	External clock input/output.
$V_{DD(LCD)}$	39	-	-	-	1.8 V to 5.5 V power supply: Power supply voltage for the PCF8576D.
$V_{SS(LCD)}$	40	-	-	-	LCD ground. The PCF8576 input signals A0, A1, A2, SA0, and OSC are internally hard-wired to $V_{SS(LCD)}$.
V_{LCD}	41	-	-	-	LCD power supply; LCD voltage.
n.c.	3	-	-	-	Not connected.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level (V_{DD} = 3.3 V)); IA = inactive, no pull-up/down enabled.

[2] $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant.

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

[7] See Section 7.2.3.

9. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)			1.8	3.3	3.6	V
Power consumption in low-current mode[10]							
I_{DD}	supply current	Active mode; code `while(1){}` executed from flash					
		system clock = 12 MHz; V_{DD} = 3.3 V	[2][3][4][5][6]	-	2	-	mA
		system clock = 50 MHz; V_{DD} = 3.3 V	[2][3][5][6][7]	-	7	-	mA
		Sleep mode; system clock = 12 MHz; V_{DD} = 3.3 V	[2][3][4][5][6]	-	1	-	mA
		Deep-sleep mode; V_{DD} = 3.3 V	[2][3][8]	-	2	-	μA
		Deep power-down mode; V_{DD} = 3.3 V	[2][9]	-	220	-	nA
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[11][12][13]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −4 mA		V_{DD} − 0.4	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −3 mA		V_{DD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		−4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		−3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[14]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[14]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V; 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	μA
		$V_{DD} < V_I$ < 5 V		0	0	0	μA
High-drive output pin (PIO0_7)							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[11][12][13]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OH} = −20 mA		$V_{DD} - 0.4$	-	-	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OH} = −12 mA		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	2.5 V ≤ V_{DD} ≤ 3.6 V; I_{OL} = 4 mA		-	-	0.4	V
		1.8 V ≤ V_{DD} < 2.5 V; I_{OL} = 3 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V; 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		12	-	-	mA

Table 6. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V 2.5 V ≤ V_{DD} ≤ 3.6 V		4	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = V_{DD}	[14]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V 2.0 V ≤ V_{DD} ≤ 3.6 V		−15	−50	−85	μA
		1.8 V ≤ V_{DD} < 2.0 V		−10	−50	−85	μA
		V_{DD} < V_I < 5 V		0	0	0	μA
I^2C-bus pins (PIO0_4 and PIO0_5)							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins 2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		3	-	-	
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		1.8 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[15]	-	2	4	μA
		V_I = 5 V		-	10	22	μA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	1.8	1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	1.8	1.95	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] T_{amb} = 25 °C.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART and SPI0/1 disabled in system configuration block.

[7] IRC disabled; system oscillator enabled; system PLL enabled.

[8] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.

[9] WAKEUP pin pulled HIGH externally.

[10] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[11] Including voltage on outputs in 3-state mode.

[12] V_{DD} supply voltage must be present.

[13] 3-state outputs go into 3-state mode in Deep power-down mode.

[14] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[15] To V_{SS}.

Table 7. ADC static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	-	± 1.5	LSB
E_O	offset error		[4]	-	-	± 3.5	LSB
E_G	gain error		[5]	-	-	0.6	%
E_T	absolute error		[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ
R_i	input resistance		[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

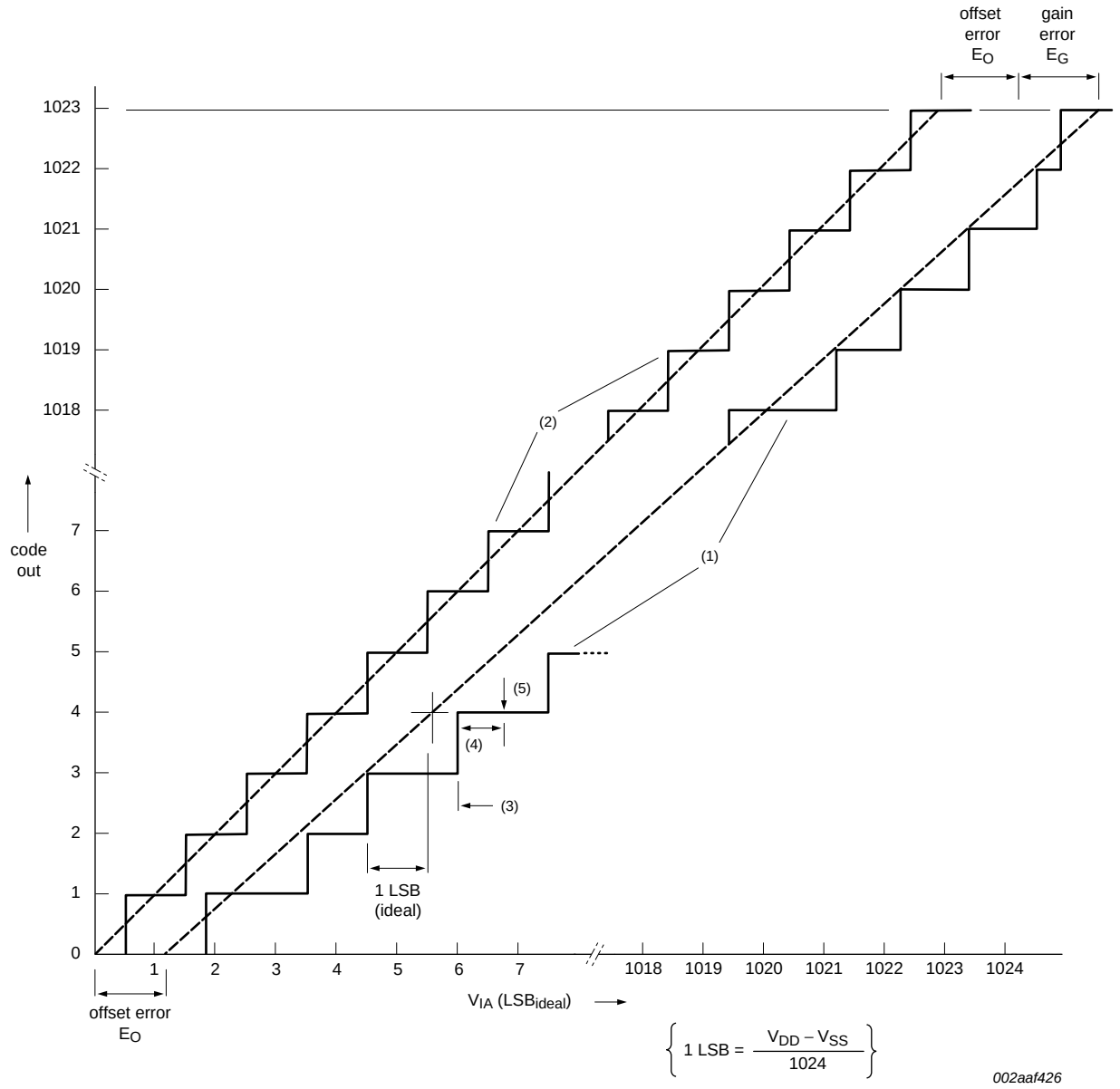
[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 5.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 1 / (f_s \times C_{ia})$.



(1) Example of an actual transfer curve.

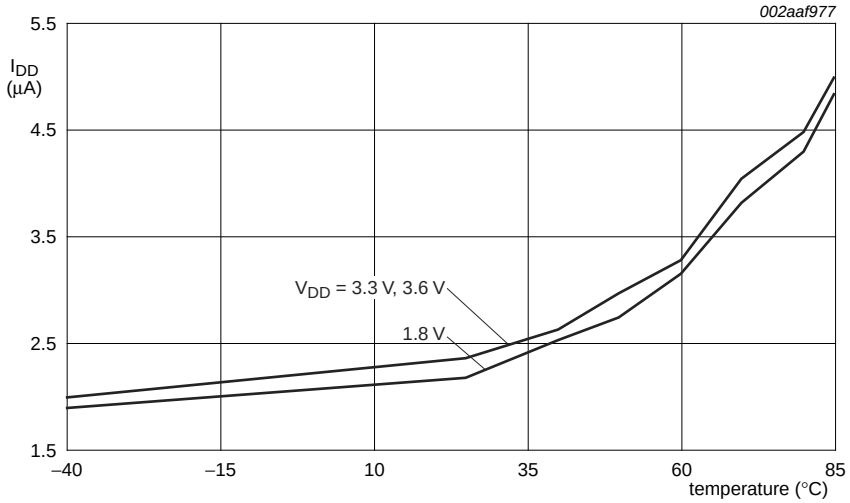
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics



Conditions: BOD disabled; all oscillators and analog blocks disabled in the PDSLEEPCFG register (PDSLEEPCFG = 0x0000 18FF).

Fig 9. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

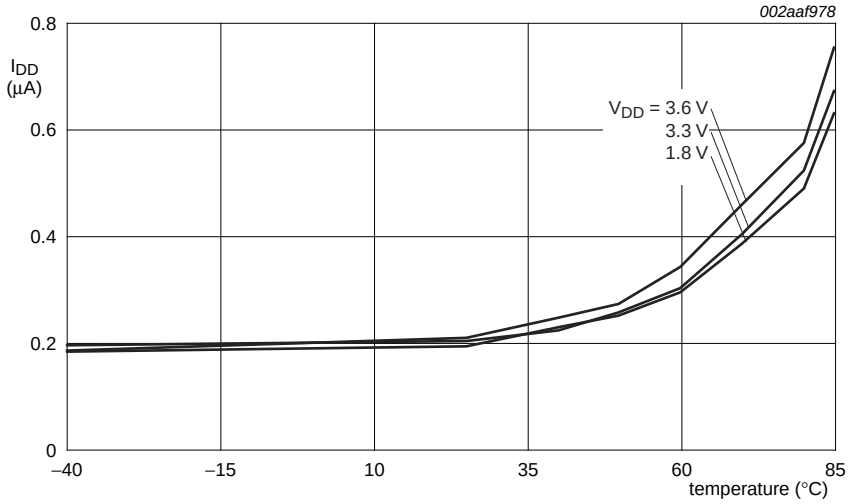


Fig 10. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

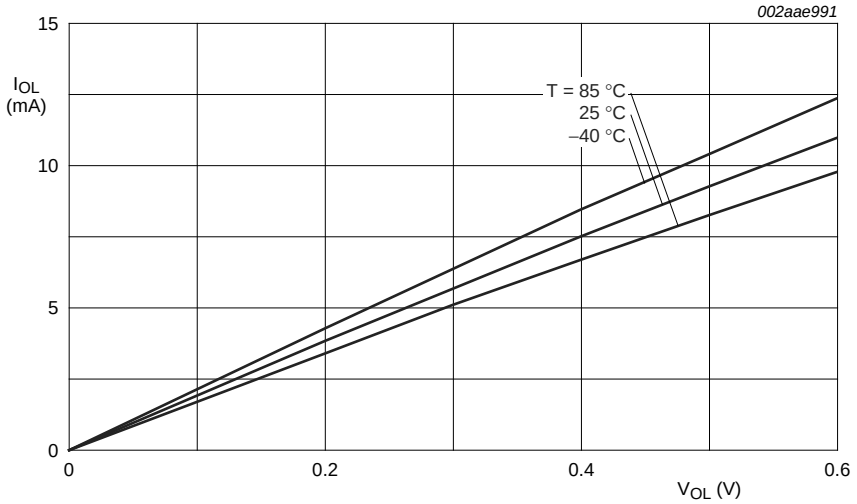
9.3 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz and 48 MHz.

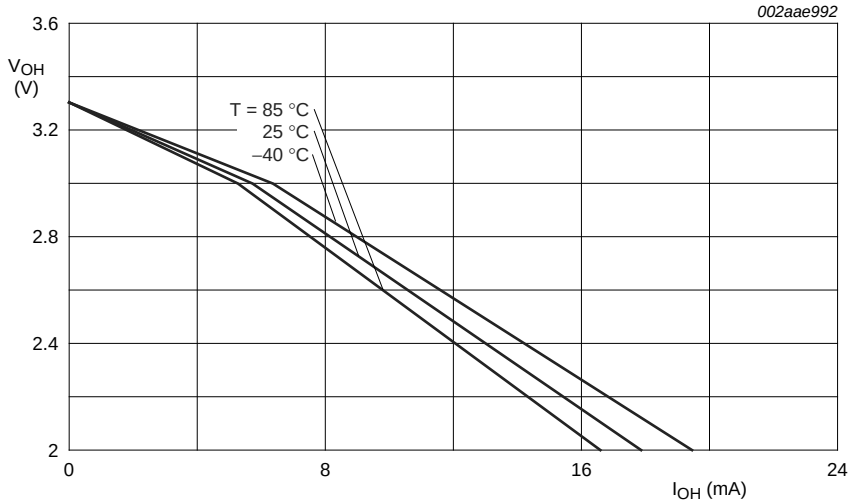
Table 9. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	48 MHz	
IRC	0.27	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.22	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.004	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.051	-	-	Independent of main clock frequency.
Main PLL	-	0.21	-	
ADC	-	0.08	0.29	
CLKOUT	-	0.12	0.47	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.02	0.06	
CT16B1	-	0.02	0.06	
CT32B0	-	0.02	0.07	
CT32B1	-	0.02	0.06	
GPIO	-	0.23	0.88	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.03	0.10	
I2C	-	0.04	0.13	
ROM	-	0.04	0.15	
SPI0	-	0.12	0.45	
SPI1	-	0.12	0.45	
UART	-	0.22	0.82	
WDT	-	0.02	0.06	Main clock selected as clock source for the WDT.



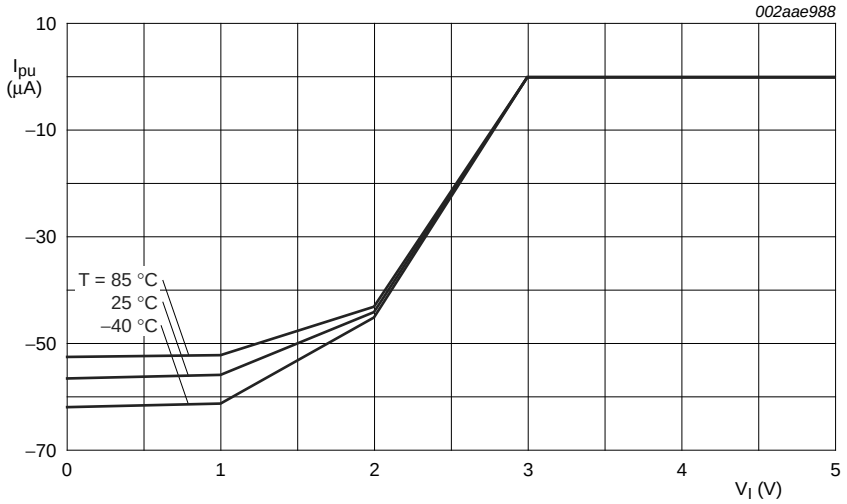
Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 13. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



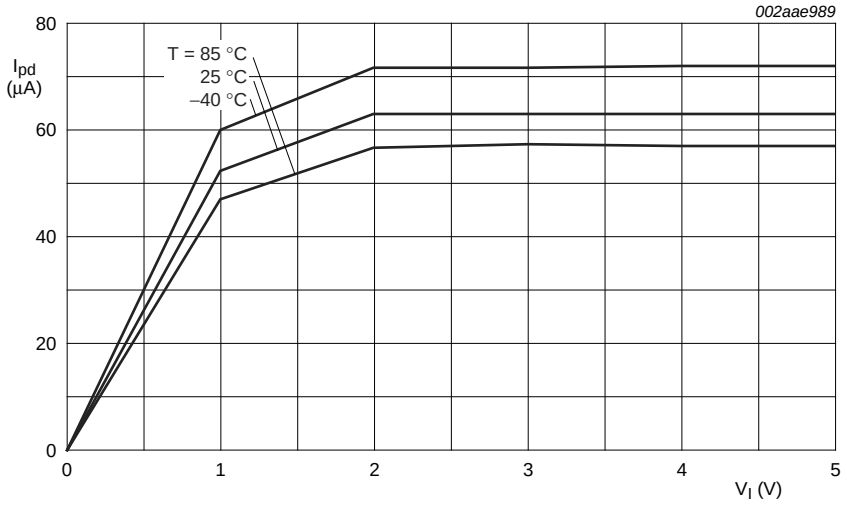
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 14. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 15. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 16. Typical pull-down current I_{pd} versus input voltage V_I

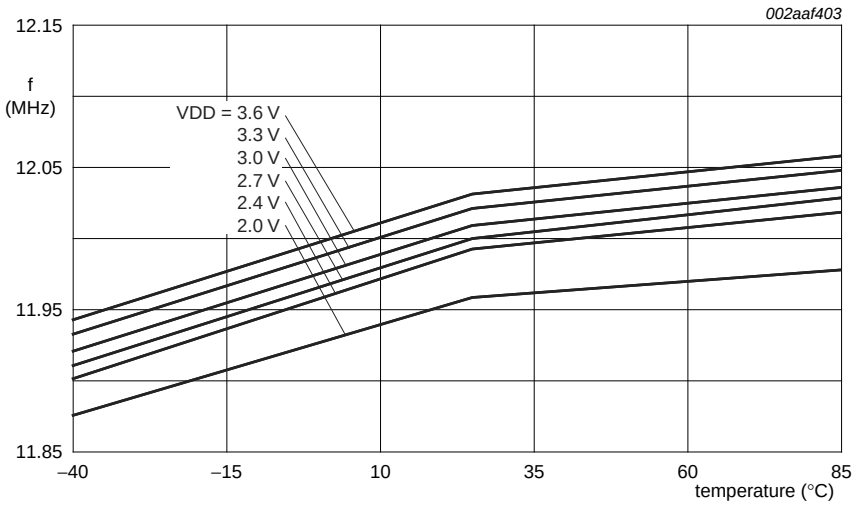
10.4 Internal oscillators

Table 13. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = −40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 19. Internal RC oscillator frequency versus temperature

Table 14. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +85 °C) is ±40 %.

[3] See the *LPC111x user manual*.

11. Application information

11.1 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 7:

- The ADC input trace must be short and as close as possible to the LPC11D14 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV (RMS) is needed.

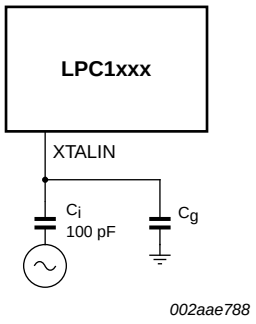


Fig 23. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 23), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 24 and in Table 18 and Table 19. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 24 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer (see Table 18).

order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

11.4 Standard I/O pad configuration

Figure 25 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

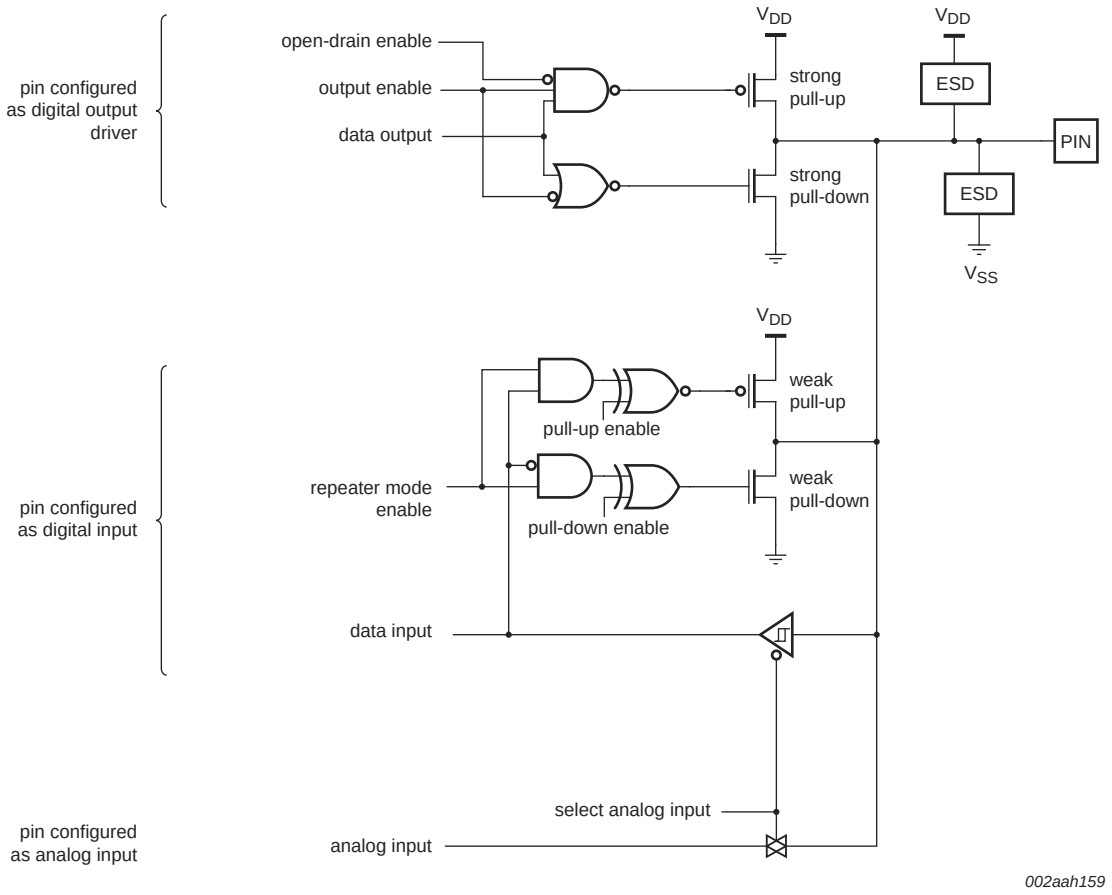


Fig 25. Standard I/O pad configuration

11.5 Reset pad configuration

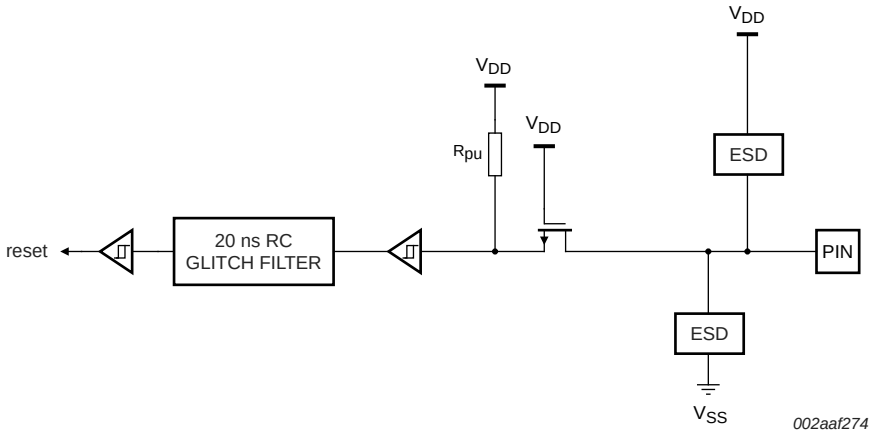


Fig 26. Reset pad configuration

11.6 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC 61967-2 standard using the TEM-cell method are shown for the LPC1114FBD48/302 in Table 20.

Table 20. ElectroMagnetic Compatibility (EMC) for part LPC1114FBD48/302 (TEM-cell method)

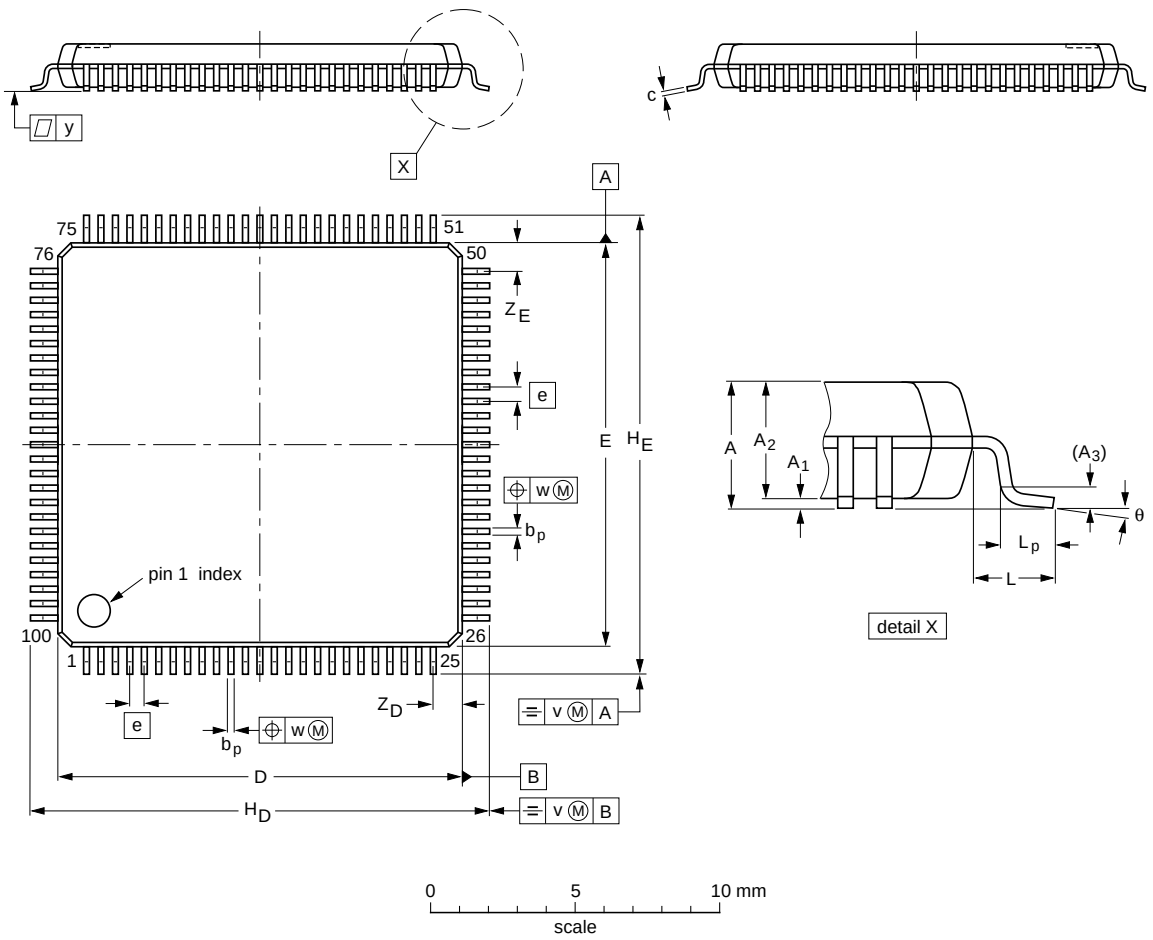
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	48 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz - 30 MHz	–7	–5	–7	dBμV
	30 MHz - 150 MHz	–2	1	10	dBμV
	150 MHz - 1 GHz	4	8	16	dBμV
IEC level[1]	-	O	N	M	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz - 30 MHz	–7	–7	–7	dBμV
	30 MHz - 150 MHz	–2	1	8	dBμV
	150 MHz - 1 GHz	4	7	14	dBμV
IEC level[1]	-	O	N	M	-

[1] IEC levels refer to Appendix D in the IEC 61967-2 Specification.

12. Package outline

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 27. Package outline (LQFP100)

16. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC11D14 v.2	20120723	Product data sheet	-	LPC11D14 v.1
Modifications:	• Figure 3 updated. • Internal oscillator description updated (Section 7.2.5). • Description of the $V_{SS(LCD)}$ pin updated in Table 3. • Data sheet status changed to Product data sheet. • Remove table note “The peak current is limited to 25 times the corresponding maximum current” in Table 5. • For parameters I_{OL}, V_{OL}, I_{OH}, V_{OH}, changed conditions to 1.8 V ≤ V_{DD} < 2.5 V and 2.5 V ≤ V_{DD} ≤ 3.6 V in Table 6. • Figure 25 updated for parts with configurable open-drain mode. • WDOSc frequency range corrected.			
LPC11D14 v.1	20110928	Preliminary data sheet	-	-