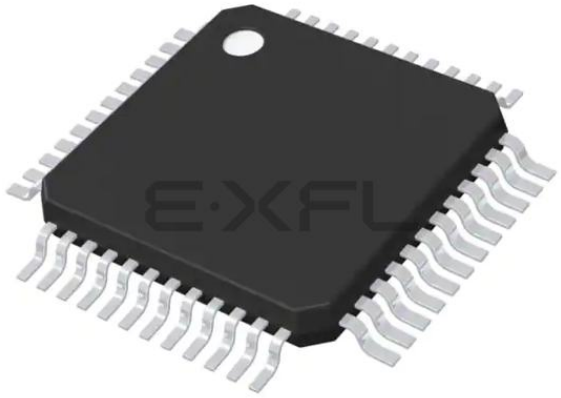
# Infineon Technologies - SAF-XC886-8FFI 3V3 AC Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.75K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | PG-TQFP-48 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc886-8ffi-3v3-ac |

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINT0
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Six ports
  - Up to 48 pins as digital I/O
  - 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- Software libraries to support floating point and MDU calculations
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Capture/compare unit for PWM signal generation (CCU6)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 12-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Packages:
  - PG-TQFP-48
  - PG-TQFP-64
- Temperature range $T_A$:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

**Table 2 Device Profile** (cont'd)

| Sales Type | Device Type | Program Memory (Kbytes) | Power Supply (V) | Temp-erature (°C) | Quality Profile |
|---|---|---|---|---|---|
| SAK-XC886*/888*-8FFA 3V3 | Flash | 32 | 3.3 | -40 to 125 | Automotive |
| SAK-XC886*/888*-6FFA 3V3 | Flash | 24 | 3.3 | -40 to 125 | Automotive |
| SAF-XC886*/888*-8FFA 3V3 | Flash | 32 | 3.3 | -40 to 85 | Automotive |
| SAF-XC886*/888*-6FFA 3V3 | Flash | 24 | 3.3 | -40 to 85 | Automotive |
| SAF-XC886*/888*-8FFI 3V3 | Flash | 32 | 3.3 | -40 to 85 | Industrial |
| SAF-XC886*/888*-6FFI 3V3 | Flash | 24 | 3.3 | -40 to 85 | Industrial |

*Note: The asterisk (*) above denotes the device configuration letters from **Table 1**. Corresponding ROM derivatives will be available on request.*

*Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.*

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC886/888 throughout this document.

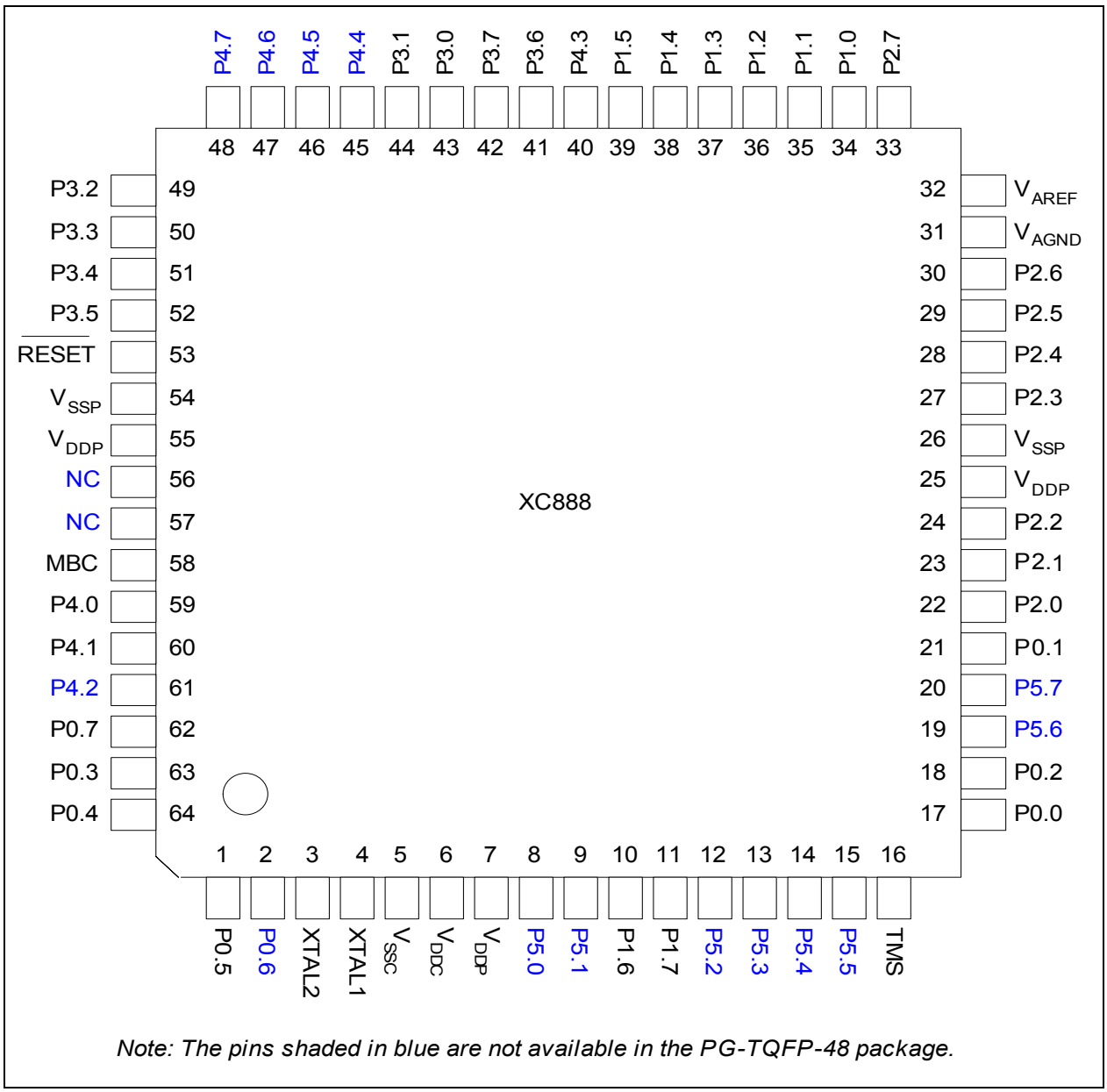
### Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC886/888, please refer to your responsible sales representative or your local distributor.

*Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.*




*Note: The pins shaded in blue are not available in the PG-TQFP-48 package.*

**Figure 5 XC888 Pin Configuration, PG-TQFP-64 Package** (top view)

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function |
|---|---|---|---|---|
| **P3** | | I/O | | **Port 3**<br>Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN. |
| P3.0 | 35/43 | | Hi-Z | CCPOS1_2 CCU6 Hall Input 1<br>CC60_0 Input/Output of Capture/Compare channel 0<br>RXDO1_1 UART1 Transmit Data Output |
| P3.1 | 36/44 | | Hi-Z | CCPOS0_2 CCU6 Hall Input 0<br>CC61_2 Input/Output of Capture/Compare channel 1<br>COUT60_0 Output of Capture/Compare channel 0<br>TXD1_1 UART1 Transmit Data Output/Clock Output |
| P3.2 | 37/49 | | Hi-Z | CCPOS2_2 CCU6 Hall Input 2<br>RXDC1_1 MultiCAN Node 1 Receiver Input<br>RXD1_1 UART1 Receive Data Input<br>CC61_0 Input/Output of Capture/Compare channel 1 |
| P3.3 | 38/50 | | Hi-Z | COUT61_0 Output of Capture/Compare channel 1<br>TXDC1_1 MultiCAN Node 1 Transmitter Output |
| P3.4 | 39/51 | | Hi-Z | CC62_0 Input/Output of Capture/Compare channel 2<br>RXDC0_1 MultiCAN Node 0 Receiver Input<br>T2EX1_0 Timer 21 External Trigger Input |
| P3.5 | 40/52 | | Hi-Z | COUT62_0 Output of Capture/Compare channel 2<br>EXF21_0 Timer 21 External Flag Output<br>TXDC0_1 MultiCAN Node 0 Transmitter Output |
| P3.6 | 33/41 | | PD | $\overline{\text{CTRAP\_0}}$ CCU6 Trap Input |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function | |
|---|---|---|---|---|---|
| **P5** | | I/O | | **Port 5**<br>Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1 and JTAG. | |
| P5.0 | –/8 | | PU | EXINT1_1 | External Interrupt Input 1 |
| P5.1 | –/9 | | PU | EXINT2_1 | External Interrupt Input 2 |
| P5.2 | –/12 | | PU | RXD_2 | UART Receive Data Input |
| P5.3 | –/13 | | PU | TXD_2 | UART Transmit Data Output/Clock Output |
| P5.4 | –/14 | | PU | RXDO_2 | UART Transmit Data Output |
| P5.5 | –/15 | | PU | TDO_2<br>TXD1_2 | JTAG Serial Data Output<br>UART1 Transmit Data Output/ Clock Output |
| P5.6 | –/19 | | PU | TCK_2<br>RXDO1_2 | JTAG Clock Input<br>UART1 Transmit Data Output |
| P5.7 | –/20 | | PU | TDI_2<br>RXD1_2 | JTAG Serial Data Input<br>UART1 Receive Data Input |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function |
|---|---|---|---|---|
| $V_{DDP}$ | 7, 17, 43/ 7, 25, 55 | – | – | **I/O Port Supply (3.3 or 5.0 V)** Also used by EVR and analog modules. All pins must be connected. |
| $V_{SSP}$ | 18, 42/26, 54 | – | – | **I/O Port Ground** All pins must be connected. |
| $V_{DDC}$ | 6/6 | – | – | **Core Supply Monitor (2.5 V)** |
| $V_{SSC}$ | 5/5 | – | – | **Core Supply Ground** |
| $V_{AREF}$ | 24/32 | – | – | **ADC Reference Voltage** |
| $V_{AGND}$ | 23/31 | – | – | **ADC Reference Ground** |
| **XTAL1** | 4/4 | I | Hi-Z | **External Oscillator Input (backup for on-chip OSC, normally NC)** |
| **XTAL2** | 3/3 | O | Hi-Z | **External Oscillator Output (backup for on-chip OSC, normally NC)** |
| **TMS** | 10/16 | I | PD | **Test Mode Select** |
| **RESET** | 41/53 | I | PU | **Reset Input** |
| **MBC**[1)] | 44/58 | I | PU | **Monitor & BootStrap Loader Control** |
| **NC** | –/56, 57 | – | – | **No Connection** |

1) An external pull-up device in the range of 4.7 kΩ to 100 kΩ. is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

### 3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range $80_H$ to $FF_H$. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

#### 3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range $80_H$ to $FF_H$, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

**SYSCON0**
**System Control Register 0** **Reset Value: $04_H$**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | **0** | | **IMODE** | **0** | **1** | **0** | **RMAP** |
| | r | | rw | r | r | r | rw |

| Field | Bits | Type | Description |
|---|---|---|---|
| **RMAP** | 0 | rw | **Interrupt Node XINTR0 Enable**<br>0 The access to the standard SFR area is enabled<br>1 The access to the mapped SFR area is enabled |
| **1** | 2 | r | **Reserved**<br>Returns 1 if read; should be written with 1. |
| **0** | [7:5], 3,1 | r | **Reserved**<br>Returns 0 if read; should be written with 0. |

*Note: The RMAP bit should be cleared/set by ANL or ORL instructions.*

### 3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC886/888 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 9**.

**Table 7 CORDIC Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $A0_H$ | **CD_STATC** **Reset: $00_H$** CORDIC Status and Data Control Register | Bit Field | KEEPZ | KEEPY | KEEPX | DMAP | INT_EN | EOC | ERROR | BSY |
| | | Type | rw | rw | rw | rw | rw | rwh | rh | rh |
| $A1_H$ | **CD_CON** **Reset: $00_H$** CORDIC Control Register | Bit Field | MPS | | X_USIGN | ST_MODE | ROTVEC | MODE | | ST |
| | | Type | rw | | rw | rw | rw | rw | | rwh |

### 3.2.4.4 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

**Table 8 SCU Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 or 1 | | | | | | | | | | |
| $8F_H$ | **SYSCON0** **Reset: $04_H$** System Control Register 0 | Bit Field | 0 | | | IMODE | 0 | 1 | 0 | RMAP |
| | | Type | r | | | rw | r | r | r | rw |
| RMAP = 0 | | | | | | | | | | |
| $BF_H$ | **SCU_PAGE** **Reset: $00_H$** Page Register | Bit Field | OP | | STNR | | 0 | PAGE | | |
| | | Type | w | | w | | r | rw | | |
| RMAP = 0, PAGE 0 | | | | | | | | | | |
| $B3_H$ | **MODPISEL** **Reset: $00_H$** Peripheral Input Select Register | Bit Field | 0 | URRISH | JTAGTDIS | JTAGTCKS | EXINT2IS | EXINT1IS | EXINT0IS | URRIS |
| | | Type | r | rw | rw | rw | rw | rw | rw | rw |
| $B4_H$ | **IRCON0** **Reset: $00_H$** Interrupt Request Register 0 | Bit Field | 0 | EXINT6 | EXINT5 | EXINT4 | EXINT3 | EXINT2 | EXINT1 | EXINT0 |
| | | Type | r | rwh | rwh | rwh | rwh | rwh | rwh | rwh |
| $B5_H$ | **IRCON1** **Reset: $00_H$** Interrupt Request Register 1 | Bit Field | 0 | CANSRC2 | CANSRC1 | ADCSR1 | ADCSR0 | RIR | TIR | EIR |
| | | Type | r | rwh | rwh | rwh | rwh | rwh | rwh | rwh |
| $B6_H$ | **IRCON2** **Reset: $00_H$** Interrupt Request Register 2 | Bit Field | 0 | | | CANSRC3 | 0 | | | CANSRC0 |
| | | Type | r | | | rwh | r | | | rwh |
| $B7_H$ | **EXICON0** **Reset: $F0_H$** External Interrupt Control Register 0 | Bit Field | EXINT3 | | EXINT2 | | EXINT1 | | EXINT0 | |
| | | Type | rw | | rw | | rw | | rw | |
| $BA_H$ | **EXICON1** **Reset: $3F_H$** External Interrupt Control Register 1 | Bit Field | 0 | | EXINT6 | | EXINT5 | | EXINT4 | |
| | | Type | r | | rw | | rw | | rw | |
| $BB_H$ | **NMICON** **Reset: $00_H$** NMI Control Register | Bit Field | 0 | NMIECC | NMIVDDP | NMIVDD | NMIOCDS | NMIFLASH | NMIPLL | NMIWDT |
| | | Type | r | rw | rw | rw | rw | rw | rw | rw |

**Table 10 Port Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0, PAGE 1 | | | | | | | | | | |
| **$80_H$** | **P0_PUDSEL Reset: $FF_H$** P0 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $86_H$ | **P0_PUDEN Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$90_H$** | **P1_PUDSEL Reset: $FF_H$** P1 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $91_H$ | **P1_PUDEN Reset: $FF_H$** P1 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $92_H$ | **P5_PUDSEL Reset: $FF_H$** P5 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $93_H$ | **P5_PUDEN Reset: $FF_H$** P5 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$A0_H$** | **P2_PUDSEL Reset: $FF_H$** P2 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $A1_H$ | **P2_PUDEN Reset: $00_H$** P2 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$B0_H$** | **P3_PUDSEL Reset: $BF_H$** P3 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $B1_H$ | **P3_PUDEN Reset: $40_H$** P3 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$C8_H$** | **P4_PUDSEL Reset: $FF_H$** P4 Pull-Up/Pull-Down Select Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $C9_H$ | **P4_PUDEN Reset: $04_H$** P4 Pull-Up/Pull-Down Enable Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| RMAP = 0, PAGE 2 | | | | | | | | | | |
| **$80_H$** | **P0_ALTSEL0 Reset: $00_H$** P0 Alternate Select 0 Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $86_H$ | **P0_ALTSEL1 Reset: $00_H$** P0 Alternate Select 1 Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| **$90_H$** | **P1_ALTSEL0 Reset: $00_H$** P1 Alternate Select 0 Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $91_H$ | **P1_ALTSEL1 Reset: $00_H$** P1 Alternate Select 1 Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |
| $92_H$ | **P5_ALTSEL0 Reset: $00_H$** P5 Alternate Select 0 Register | Bit Field | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| | | Type | rw | rw | rw | rw | rw | rw | rw | rw |

### 3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 16 SSC Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 | | | | | | | | | | |
| $A9_H$ | **SSC_PISEL** **Reset: $00_H$** Port Input Select Register | Bit Field | 0 | | | | | CIS | SIS | MIS |
| | | Type | r | | | | | rw | rw | rw |
| $AA_H$ | **SSC_CONL** **Reset: $00_H$** Control Register Low Programming Mode | Bit Field | LB | PO | PH | HB | BM | | | |
| | | Type | rw | rw | rw | rw | rw | | | |
| $AA_H$ | **SSC_CONL** **Reset: $00_H$** Control Register Low Operating Mode | Bit Field | 0 | | | | BC | | | |
| | | Type | r | | | | rh | | | |
| $AB_H$ | **SSC_CONH** **Reset: $00_H$** Control Register High Programming Mode | Bit Field | EN | MS | 0 | AREN | BEN | PEN | REN | TEN |
| | | Type | rw | rw | r | rw | rw | rw | rw | rw |
| $AB_H$ | **SSC_CONH** **Reset: $00_H$** Control Register High Operating Mode | Bit Field | EN | MS | 0 | BSY | BE | PE | RE | TE |
| | | Type | rw | rw | r | rh | rwh | rwh | rwh | rwh |
| $AC_H$ | **SSC_TBL** **Reset: $00_H$** Transmitter Buffer Register Low | Bit Field | TB_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |
| $AD_H$ | **SSC_RBL** **Reset: $00_H$** Receiver Buffer Register Low | Bit Field | RB_VALUE | | | | | | | |
| | | Type | rh | | | | | | | |
| $AE_H$ | **SSC_BRL** **Reset: $00_H$** Baud Rate Timer Reload Register Low | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |
| $AF_H$ | **SSC_BRH** **Reset: $00_H$** Baud Rate Timer Reload Register High | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |

### 3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 17 CAN Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 | | | | | | | | | | |
| **$D8_H$** | **ADCON** **Reset: $00_H$** CAN Address/Data Control Register | Bit Field | V3 | V2 | V1 | V0 | AUAD | | BSY | RWEN |
| | | Type | rw | rw | rw | rw | rw | | rh | rw |
| $D9_H$ | **ADL** **Reset: $00_H$** CAN Address Register Low | Bit Field | CA9 | CA8 | CA7 | CA6 | CA5 | CA4 | CA3 | CA2 |
| | | Type | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |
| $DA_H$ | **ADH** **Reset: $00_H$** CAN Address Register High | Bit Field | 0 | | | | CA13 | CA12 | CA11 | CA10 |
| | | Type | r | | | | rwh | rwh | rwh | rwh |

## 3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC886/888 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

### 3.4.1 Interrupt Source

**Figure 13** to **Figure 17** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

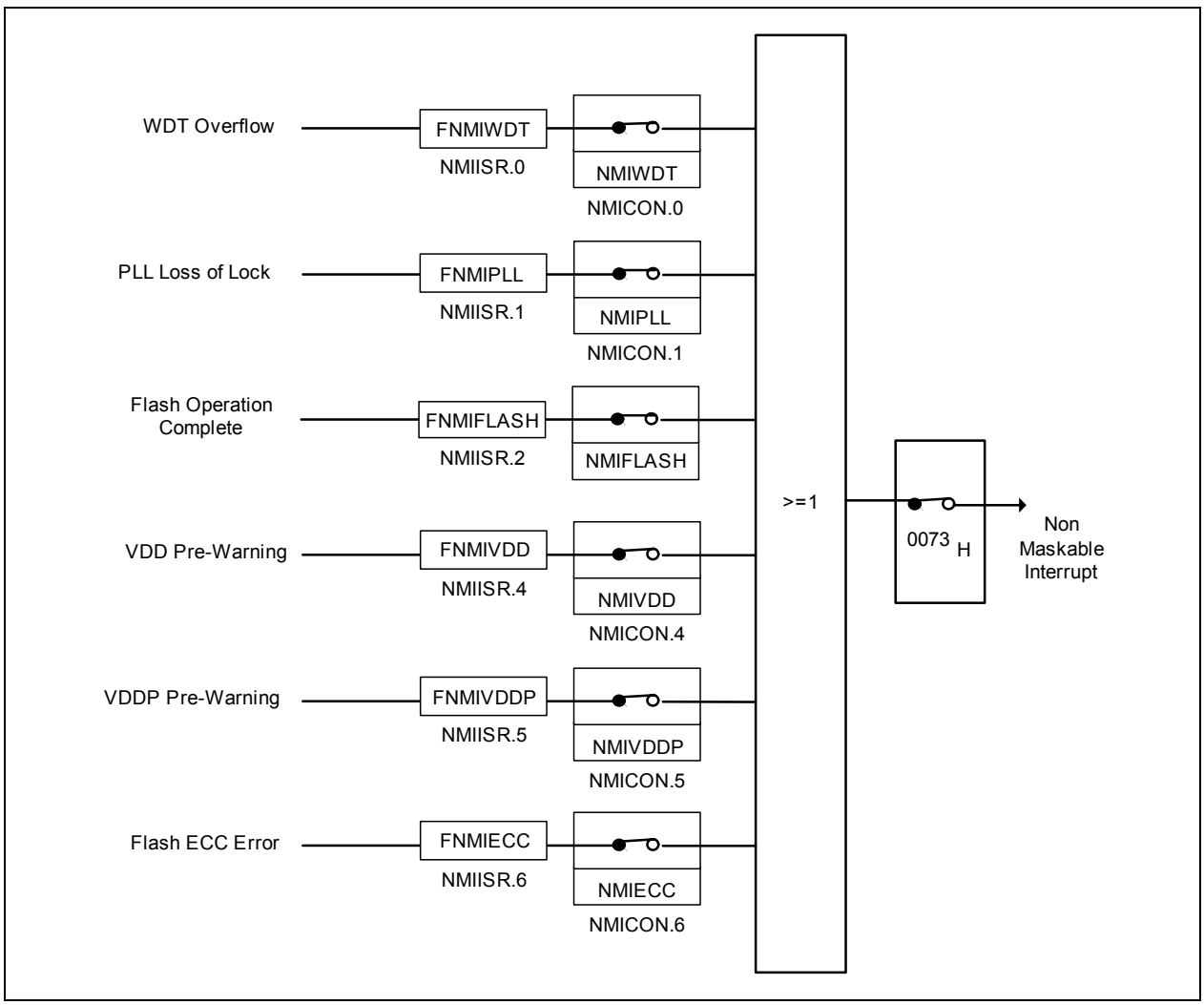



**Figure 13 Non-Maskable Interrupt Request Sources**

**Figure 19** shows the structure of a bidirectional port pin.

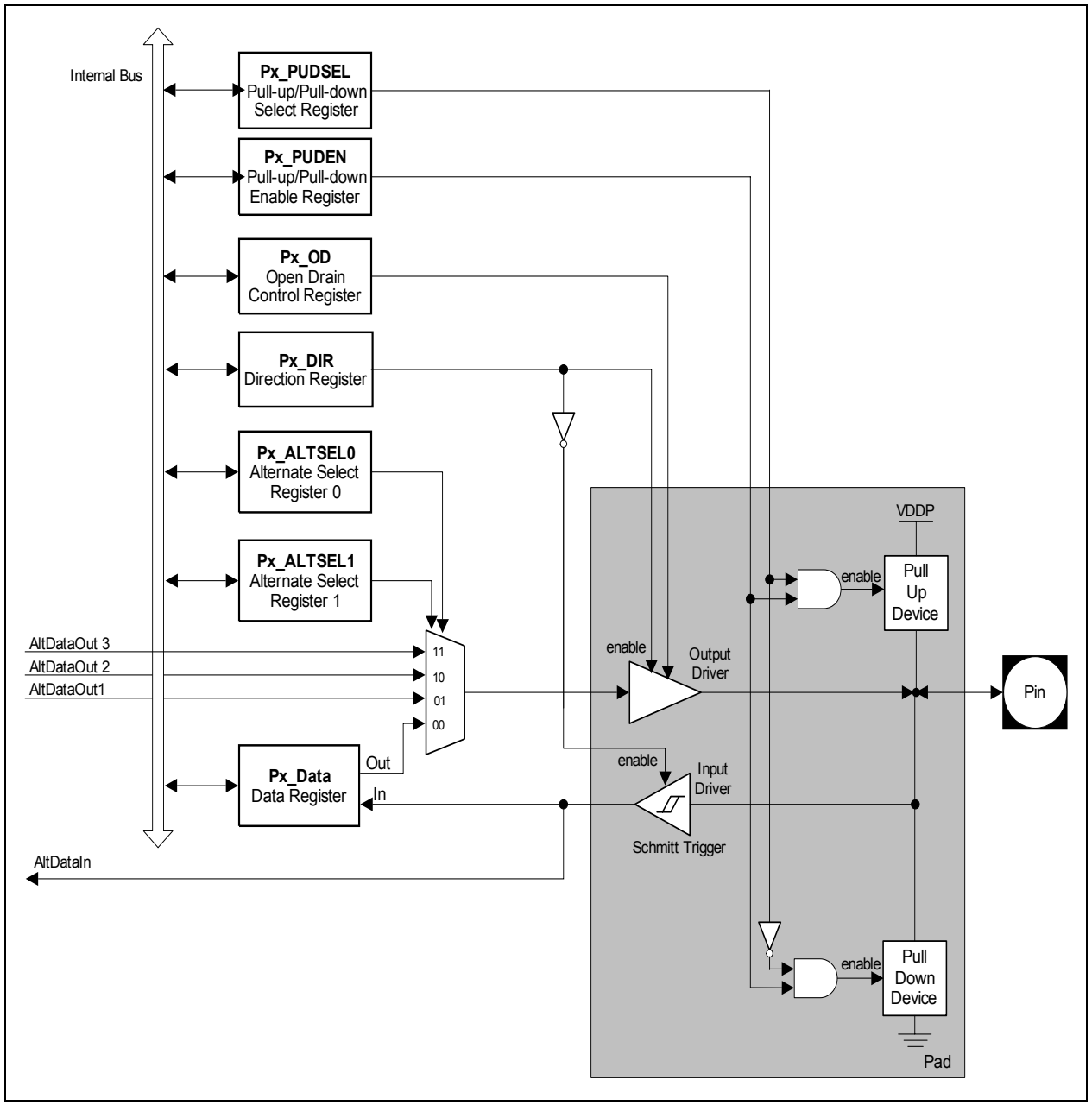



**Figure 19 General Structure of Bidirectional Port**

**Figure 20** shows the structure of an input-only port pin.

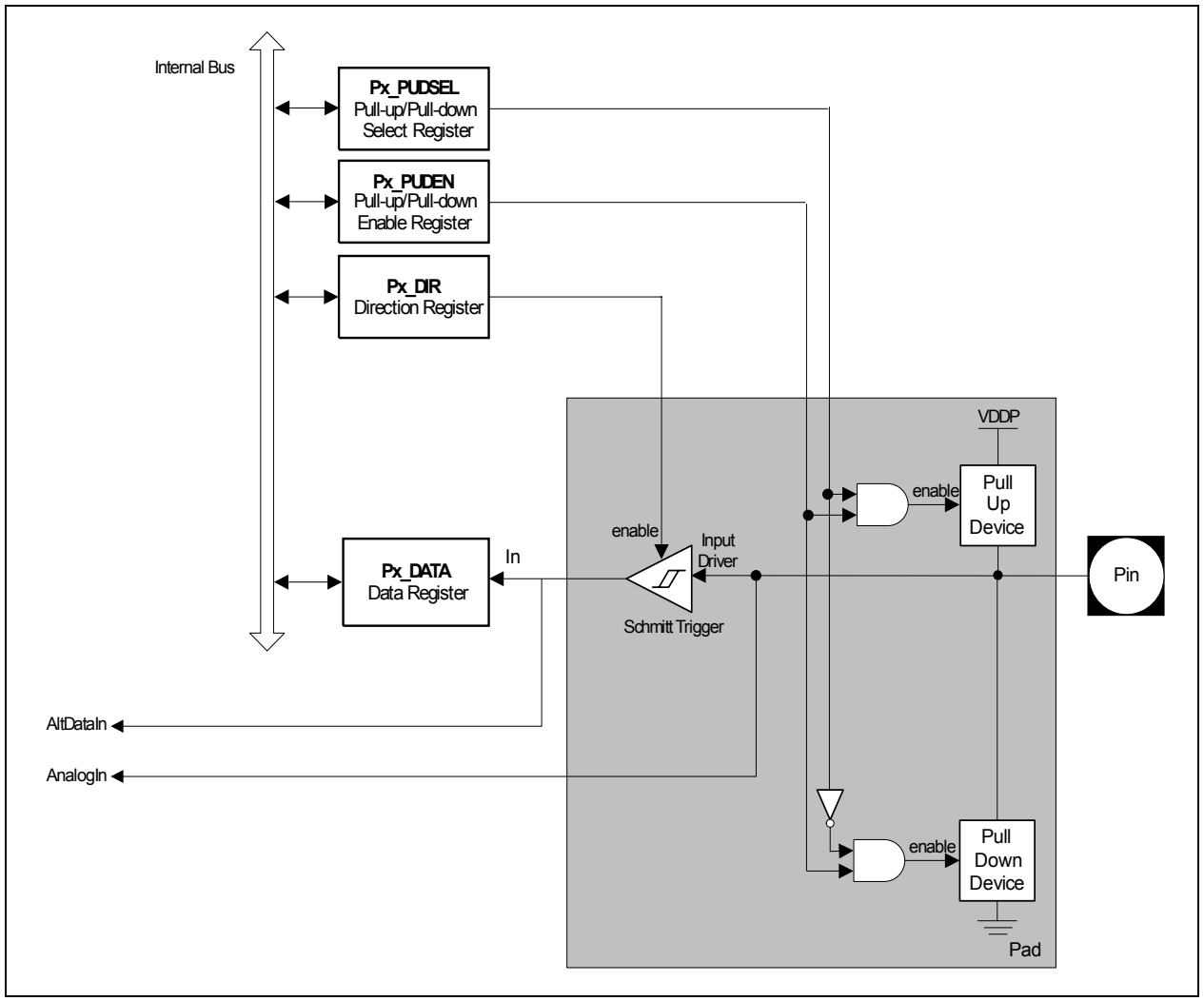



**Figure 20 General Structure of Input Port**

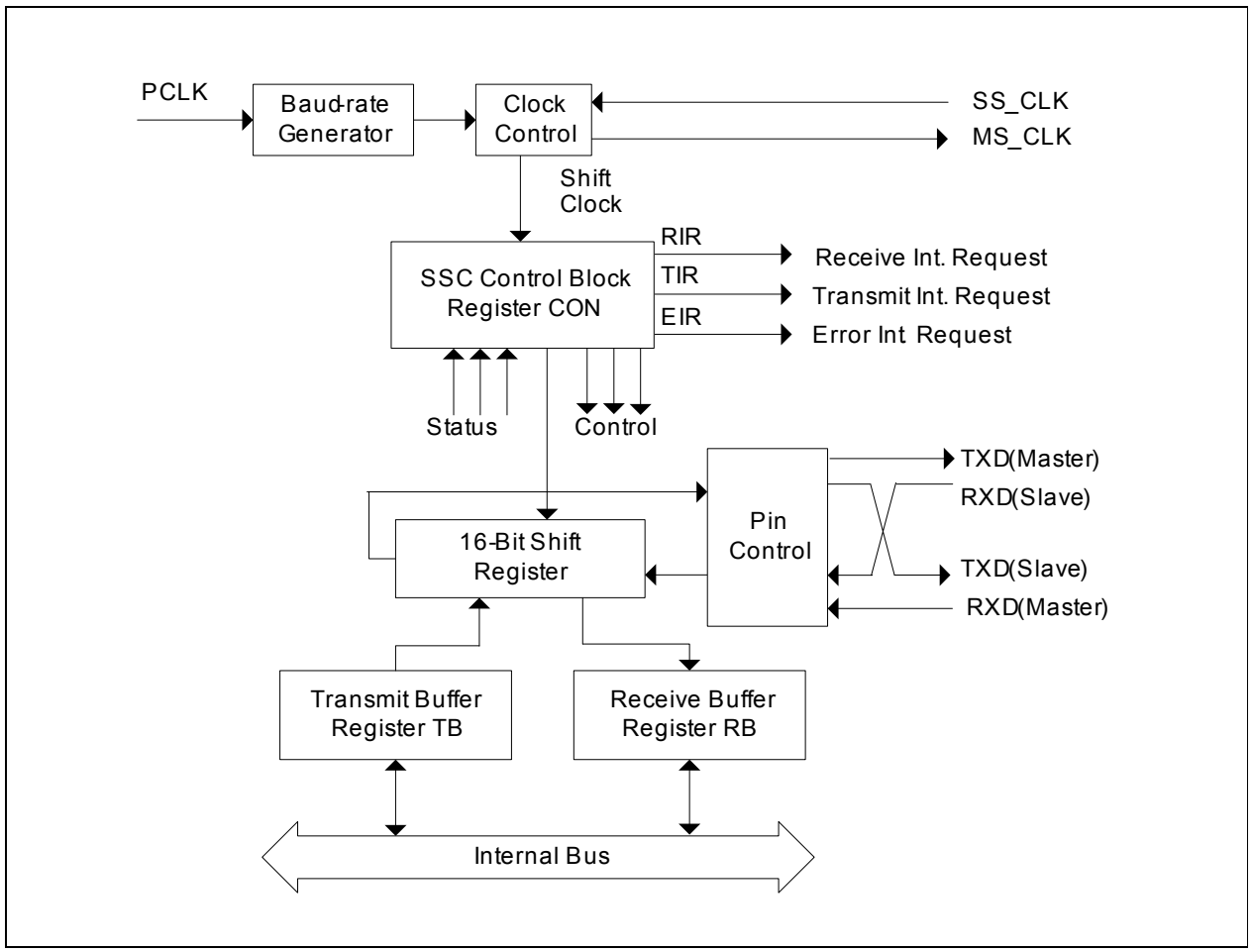



**Figure 32 SSC Block Diagram**

## 3.23 Chip Identification Number

The XC886/888 identity (ID) register is located at Page 1 of address $B3_H$. The value of ID register is $09_H$ for Flash devices and $22_H$ for ROM devices. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

**Table 36** lists the chip identification numbers of available XC886/888 Flash and ROM device variants.

**Table 36 Chip Identification Number**

| Product Variant | Chip Identification Number | | |
|---|---|---|---|
| | AA-Step | AB-Step | AC-Step |
| **Flash Devices** | | | |
| XC886CLM-8FFA 3V3 | - | $09500102_H$ | $0B500102_H$ |
| XC888CLM-8FFA 3V3 | - | $09500103_H$ | $0B500103_H$ |
| XC886LM-8FFA 3V3 | - | $09500122_H$ | $0B500122_H$ |
| XC888LM-8FFA 3V3 | - | $09500123_H$ | $0B500123_H$ |
| XC886CLM-6FFA 3V3 | - | $09551502_H$ | $0B551502_H$ |
| XC888CLM-6FFA 3V3 | - | $09551503_H$ | $0B551503_H$ |
| XC886LM-6FFA 3V3 | - | $09551522_H$ | $0B551522_H$ |
| XC888LM-6FFA 3V3 | - | $09551523_H$ | $0B551523_H$ |
| XC886CM-8FFA 3V3 | - | $09580102_H$ | $0B580102_H$ |
| XC888CM-8FFA 3V3 | - | $09580103_H$ | $0B580103_H$ |
| XC886C-8FFA 3V3 | - | $09580142_H$ | $0B580142_H$ |
| XC888C-8FFA 3V3 | - | $09580143_H$ | $0B580143_H$ |
| XC886-8FFA 3V3 | - | $09580162_H$ | $0B580162_H$ |
| XC888-8FFA 3V3 | - | $09580163_H$ | $0B580163_H$ |
| XC886CM-6FFA 3V3 | - | $095D1502_H$ | $0B5D1502_H$ |
| XC888CM-6FFA 3V3 | - | $095D1503_H$ | $0B5D1503_H$ |
| XC886C-6FFA 3V3 | - | $095D1542_H$ | $0B5D1542_H$ |
| XC888C-6FFA 3V3 | - | $095D1543_H$ | $0B5D1543_H$ |

### 4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC886/888 can be subjected to without permanent damage.

**Table 4-1 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Ambient temperature | $T_A$ | -40 | 125 | °C | under bias |
| Storage temperature | $T_{ST}$ | -65 | 150 | °C | 1) |
| Junction temperature | $T_J$ | -40 | 150 | °C | under bias1) |
| Voltage on power supply pin with respect to $V_{SS}$ | $V_{DDP}$ | -0.5 | 6 | V | 1) |
| Voltage on any pin with respect to $V_{SS}$ | $V_{IN}$ | -0.5 | $V_{DDP}$ + 0.5 or max. 6 | V | whichever is lower1) |
| Input current on any pin during overload condition | $I_{IN}$ | -10 | 10 | mA | 1) |
| Absolute sum of all input currents during overload condition | $\Sigma\|I_{IN}\|$ | – | 50 | mA | 1) |

1) Not subjected to production test, verified by design/characterization.

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pin with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.*

## 4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

### 4.2.1 Input/Output Characteristics

**Table 38** provides the characteristics of the input/output pins of the XC886/888.

**Table 38 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| **$V_{DDP}$ = 5 V Range** | | | | | | |
| Output low voltage | $V_{OL}$ | CC | – | 1.0 | V | $I_{OL}$ = 15 mA |
| | | | – | 1.0 | V | $I_{OL}$ = 5 mA, current into all pins > 60 mA |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA, current into all pins ≤ 60 mA |
| Output high voltage | $V_{OH}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -15 mA |
| | | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -5 mA, current from all pins > 60 mA |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -5 mA, current from all pins ≤ 60 mA |
| Input low voltage on port pins (all except P0.0 & P0.1) | $V_{ILP}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on P0.0 & P0.1 | $V_{ILP0}$ | SR | -0.2 | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on $\overline{\text{RESET}}$ pin | $V_{ILR}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on TMS pin | $V_{ILT}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on port pins (all except P0.0 & P0.1) | $V_{IHP}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on P0.0 & P0.1 | $V_{IHP0}$ | SR | 0.7 × $V_{DDP}$ | $V_{DDP}$ | V | CMOS Mode |

**Table 38 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Input high voltage on RESET pin | $V_{IHR}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on TMS pin | $V_{IHT}$ | SR | 0.75 × $V_{DDP}$ | – | V | CMOS Mode |
| Input Hysteresis on port pins | $HYSP$ | CC | 0.07 × $V_{DDP}$ | – | V | CMOS Mode[1)] |
| Input Hysteresis on XTAL1 | $HYSX$ | CC | 0.07 × $V_{DDC}$ | – | V | [1)] |
| Input low voltage at XTAL1 | $V_{ILX}$ | SR | $V_{SS}$ - 0.5 | 0.3 × $V_{DDC}$ | V | |
| Input high voltage at XTAL1 | $V_{IHX}$ | SR | 0.7 × $V_{DDC}$ | $V_{DDC}$ + 0.5 | V | |
| Pull-up current | $I_{PU}$ | SR | – | -10 | µA | $V_{IHP,min}$ |
| | | | -150 | – | µA | $V_{ILP,max}$ |
| Pull-down current | $I_{PD}$ | SR | – | 10 | µA | $V_{ILP,max}$ |
| | | | 150 | – | µA | $V_{IHP,min}$ |
| Input leakage current | $I_{OZ1}$ | CC | -1 | 1 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$[2)] |
| Input current at XTAL1 | $I_{ILX}$ | CC | -10 | 10 | µA | |
| Overload current on any pin | $I_{OV}$ | SR | -5 | 5 | mA | |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ | SR | – | 25 | mA | [3)] |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [4)] |
| Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$) | $I_M$ SR | SR | – | 15 | mA | |
| Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$) | $\Sigma\|I_M\|$ | SR | – | 90 | mA | |
| Maximum current into $V_{DDP}$ | $I_{MVDDP}$ | SR | – | 120 | mA | [3)] |

**Table 38 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 120 | mA | [3] |
| **$V_{DDP}$ = 3.3 V Range** | | | | | | |
| Output low voltage | $V_{OL}$ | CC | – | 1.0 | V | $I_{OL}$ = 8 mA |
| | | | – | 0.4 | V | $I_{OL}$ = 2.5 mA |
| Output high voltage | $V_{OH}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -8 mA |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -2.5 mA |
| Input low voltage on port pins (all except P0.0 & P0.1) | $V_{ILP}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on P0.0 & P0.1 | $V_{ILP0}$ | SR | -0.2 | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on RESET pin | $V_{ILR}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on TMS pin | $V_{ILT}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on port pins (all except P0.0 & P0.1) | $V_{IHP}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on P0.0 & P0.1 | $V_{IHP0}$ | SR | 0.7 × $V_{DDP}$ | $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on RESET pin | $V_{IHR}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on TMS pin | $V_{IHT}$ | SR | 0.75 × $V_{DDP}$ | – | V | CMOS Mode |
| Input Hysteresis | $HYS$ | CC | 0.03 × $V_{DDP}$ | – | V | CMOS Mode[1] |
| Input Hysteresis on XTAL1 | $HYSX$ | CC | 0.07 × $V_{DDC}$ | – | V | [1] |
| Input low voltage at XTAL1 | $V_{ILX}$ | SR | $V_{SS}$ - 0.5 | 0.3 × $V_{DDC}$ | V | |