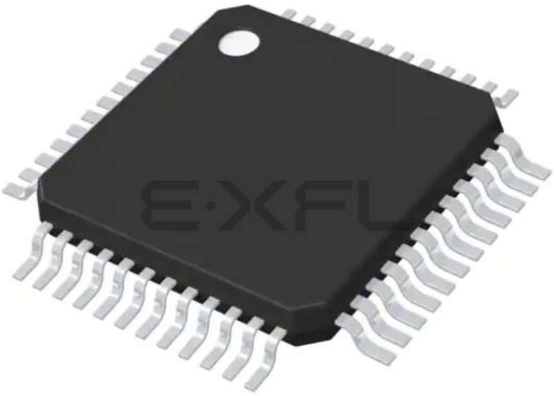

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc886cm-6ffa-5v-ac

Edition 2009-07

Published by
Infineon Technologies AG
81726 Munich, Germany

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XC886/888 Variant Devices

The XC886/888 product family features devices with different configurations, program memory sizes, package options, power supply voltage, temperature and quality profiles (Automotive or Industrial), to offer cost-effective solutions for different application requirements.

The list of XC886/888 device configurations are summarized in **Table 1**. For each configuration, 2 types of packages are available:

- PG-TQFP-48, which is denoted by XC886 and;
- PG-TQFP-64, which is denoted by XC888.

Table 1 Device Configuration

Device Name	CAN Module	LIN BSL Support	MDU Module
XC886/888	No	No	No
XC886/888C	Yes	No	No
XC886/888CM	Yes	No	Yes
XC886/888LM	No	Yes	Yes
XC886/888CLM	Yes	Yes	Yes

Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.

From these 10 different combinations of configuration and package type, each are further made available in many sales types, which are grouped according to device type, program memory sizes, power supply voltage, temperature and quality profile (Automotive or Industrial), as shown in **Table 2**.

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp-erature (°C)	Quality Profile
SAK-XC886*/888*-8FFA 5V	Flash	32	5.0	-40 to 125	Automotive
SAK-XC886*/888*-6FFA 5V	Flash	24	5.0	-40 to 125	Automotive
SAF-XC886*/888*-8FFA 5V	Flash	32	5.0	-40 to 85	Automotive
SAF-XC886*/888*-6FFA 5V	Flash	24	5.0	-40 to 85	Automotive
SAF-XC886*/888*-8FFI 5V	Flash	32	5.0	-40 to 85	Industrial
SAF-XC886*/888*-6FFI 5V	Flash	24	5.0	-40 to 85	Industrial

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN.	
P3.0	35/43		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CC61_2 COUT60_0 TXD1_1	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare channel 0 UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 TXDC1_1	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 RXDC0_1 T2EX1_0	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 EXF21_0 TXDC0_1	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	$\overline{\text{CTRAP\_0}}$	CCU6 Trap Input

3.2 Memory Organization

The XC886/888 CPU operates in the following five address spaces:

- 12 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 1.5 Kbytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 24/32 Kbytes of Flash program memory (Flash devices); or
  24/32 Kbytes of ROM program memory, with additional 4 Kbytes of Flash
  (ROM devices)

Figure 7 illustrates the memory address spaces of the 32-Kbyte Flash devices. For the 24-Kbyte Flash devices, the shaded banks are not available.

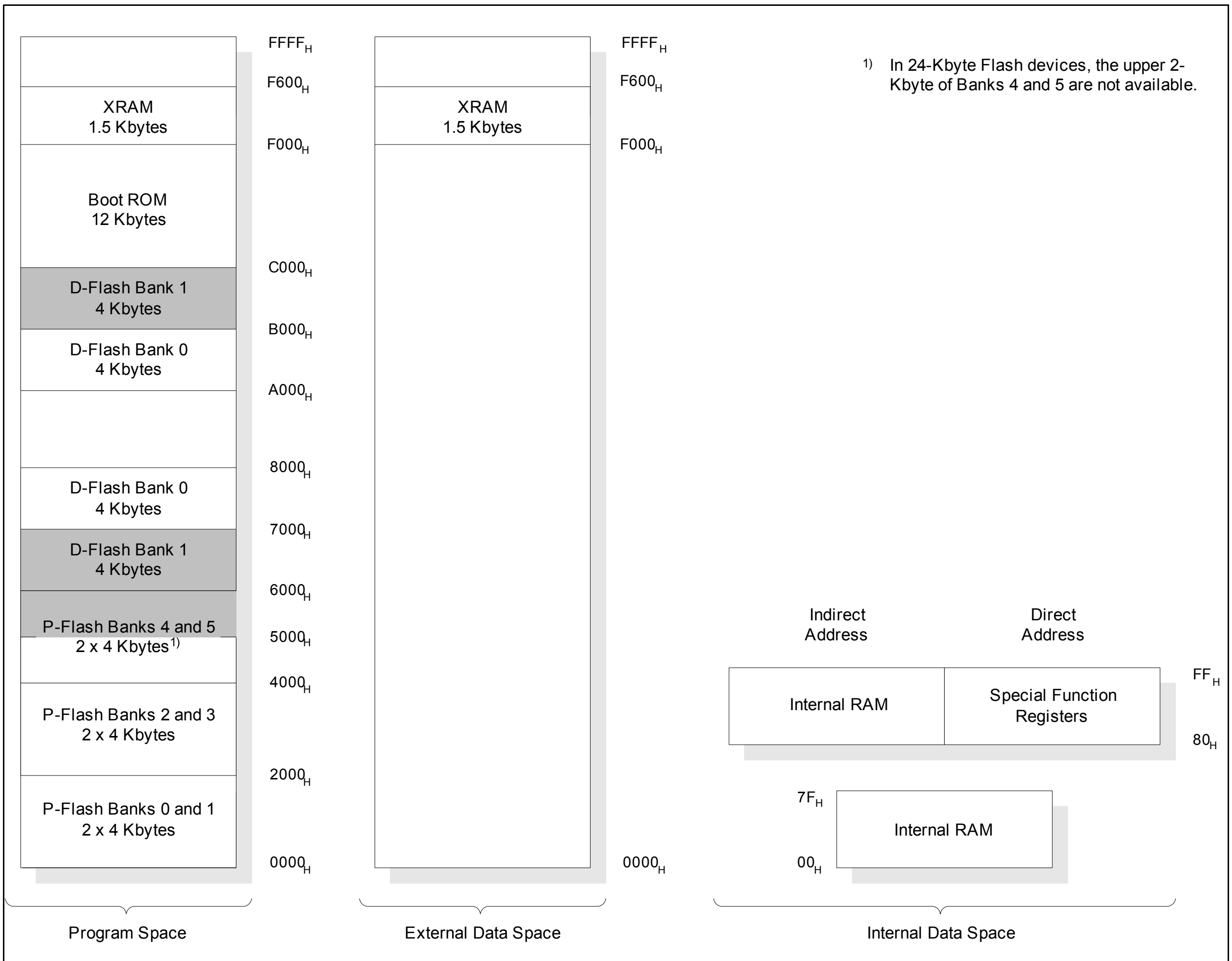

Figure 7 Memory Map of XC886/888 Flash Device

For both 24-Kbyte and 32-Kbyte ROM devices, the last four bytes of the ROM from $7FFC_H$ to $7FFF_H$ are reserved for the ROM signature and cannot be used to store user

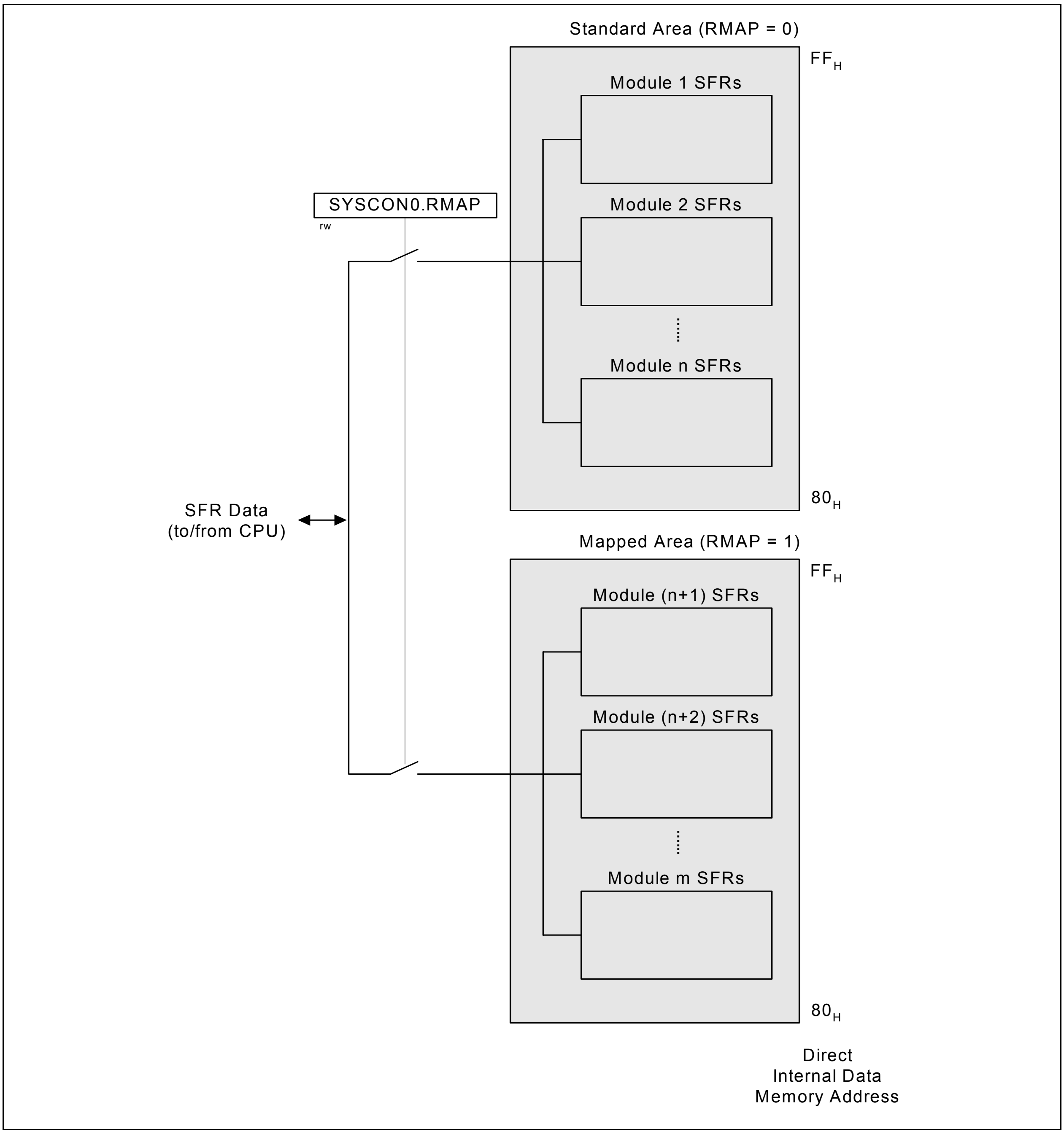

Figure 8 Address Extension by Mapping

Table 5 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$A8_H$	**IEN0** **Reset: 00_H** Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
$B8_H$	**IP** **Reset: 00_H** Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
$B9_H$	**IPH** **Reset: 00_H** Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
$D0_H$	**PSW** **Reset: 00_H** Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
$E0_H$	**ACC** **Reset: 00_H** Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$E8_H$	**IEN1** **Reset: 00_H** Interrupt Enable Register 1	Bit Field	ECCIP 3	ECCIP 2	ECCIP 1	ECCIP 0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F0_H$	**B** **Reset: 00_H** B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F8_H$	**IP1** **Reset: 00_H** Interrupt Priority 1 Register	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$F9_H$	**IPH1** **Reset: 00_H** Interrupt Priority 1 High Register	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSC H	PADC H
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 MDU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$B0_H$	**MDUSTAT** **Reset: 00_H** MDU Status Register	Bit Field	0					BSY	IERR	IRDY
		Type	r					rh	rwh	rwh
$B1_H$	**MDUCON** **Reset: 00_H** MDU Control Register	Bit Field	IE	IR	RSEL	STAR T	OPCODE			
		Type	rw	rw	rw	rwh	rw			
$B2_H$	**MD0** **Reset: 00_H** MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
$B2_H$	**MR0** **Reset: 00_H** MDU Result Register 0	Bit Field	DATA							
		Type	rh							
$B3_H$	**MD1** **Reset: 00_H** MDU Operand Register 1	Bit Field	DATA							
		Type	rw							

Table 8 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE_H	**COCON** **Reset: 00_H** Clock Output Control Register	Bit Field	0		TLEN	COUTS	COREL			
		Type	r		rw	rw	rw			
$E9_H$	**MISC_CON** **Reset: 00_H** Miscellaneous Control Register	Bit Field	0							DFLASHEN
		Type	r							rwh
RMAP = 0, PAGE 3										
$B3_H$	**XADDRH** **Reset: $F0_H$** On-chip XRAM Address Higher Order	Bit Field	ADDRH							
		Type	rw							
$B4_H$	**IRCON3** **Reset: 00_H** Interrupt Request Register 3	Bit Field	0		CANSRC5	CCU6SR1	0		CANSRC4	CCU6SR0
		Type	r		rwh	rwh	r		rwh	rwh
$B5_H$	**IRCON4** **Reset: 00_H** Interrupt Request Register 4	Bit Field	0		CANSRC7	CCU6SR3	0		CANSRC6	CCU6SR2
		Type	r		rwh	rwh	r		rwh	rwh
$B7_H$	**MODPISEL1** **Reset: 00_H** Peripheral Input Select Register 1	Bit Field	EXINT6IS	0		UR1RIS		T21EXIS	JTAGTDIS1	JTAGTCKS1
		Type	rw	r		rw		rw	rw	rw
BA_H	**MODPISEL2** **Reset: 00_H** Peripheral Input Select Register 2	Bit Field	0				T21IS	T2IS	T1IS	T0IS
		Type	r				rw	rw	rw	rw
BB_H	**PMCON2** **Reset: 00_H** Power Mode Control Register 2	Bit Field	0						UART1_DIS	T21_DIS
		Type	r						rw	rw
BD_H	**MODSUSP** **Reset: 01_H** Module Suspend Control Register	Bit Field	0			T21SUSP	T2SUSP	T13SUSP	T12SUSP	WDTSUSP
		Type	r			rw	rw	rw	rw	rw

3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB_H	**WDTCON** **Reset: 00_H** Watchdog Timer Control Register	Bit Field	0		WINBEN	WDTPR	0	WDTEN	WDTRS	WDTIN
		Type	r		rw	rh	r	rw	rwh	rw
BC_H	**WDTREL** **Reset: 00_H** Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD_H	**WDTWINB** **Reset: 00_H** Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							

Table 9 WDT Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_DATA** **Reset: 00_H** P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_DIR** **Reset: 00_H** P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A0_H$	**P2_DATA** **Reset: 00_H** P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_DIR** **Reset: 00_H** P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_DATA** **Reset: 00_H** P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_DIR** **Reset: 00_H** P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FA_H	**CCU6_CC60SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 Low	Bit Field	CC60SL							
		Type	rwh							
FB_H	**CCU6_CC60SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 High	Bit Field	CC60SH							
		Type	rwh							
FC_H	**CCU6_CC61SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 Low	Bit Field	CC61SL							
		Type	rwh							
FD_H	**CCU6_CC61SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 High	Bit Field	CC61SH							
		Type	rwh							
FE_H	**CCU6_CC62SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 Low	Bit Field	CC62SL							
		Type	rwh							
FF_H	**CCU6_CC62SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 High	Bit Field	CC62SH							
		Type	rwh							
RMAP = 0, PAGE 1										
$9A_H$	**CCU6_CC63RL** **Reset: 00_H** Capture/Compare Register for Channel CC63 Low	Bit Field	CC63VL							
		Type	rh							
$9B_H$	**CCU6_CC63RH** **Reset: 00_H** Capture/Compare Register for Channel CC63 High	Bit Field	CC63VH							
		Type	rh							
$9C_H$	**CCU6_T12PRL** **Reset: 00_H** Timer T12 Period Register Low	Bit Field	T12PVL							
		Type	rwh							
$9D_H$	**CCU6_T12PRH** **Reset: 00_H** Timer T12 Period Register High	Bit Field	T12PVH							
		Type	rwh							
$9E_H$	**CCU6_T13PRL** **Reset: 00_H** Timer T13 Period Register Low	Bit Field	T13PVL							
		Type	rwh							
$9F_H$	**CCU6_T13PRH** **Reset: 00_H** Timer T13 Period Register High	Bit Field	T13PVH							
		Type	rwh							
$A4_H$	**CCU6_T12DTCL** **Reset: 00_H** Dead-Time Control Register for Timer T12 Low	Bit Field	DTM							
		Type	rw							
$A5_H$	**CCU6_T12DTCH** **Reset: 00_H** Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0
		Type	r	rh	rh	rh	r	rw	rw	rw
$A6_H$	**CCU6_TCTR0L** **Reset: 00_H** Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE12	T12R	T12 PRE	T12CLK		
		Type	rw	rh	rh	rh	rw	rw		
$A7_H$	**CCU6_TCTR0H** **Reset: 00_H** Timer Control Register 0 High	Bit Field	0		STE13	T13R	T13 PRE	T13CLK		
		Type	r		rh	rh	rw	rw		
FA_H	**CCU6_CC60RL** **Reset: 00_H** Capture/Compare Register for Channel CC60 Low	Bit Field	CC60VL							
		Type	rh							

3.3.3 Flash Programming Width

For the P-Flash banks, a programmed wordline (WL) must be erased before it can be reprogrammed as the Flash cells can only withstand one gate disturb. This means that the entire sector containing the WL must be erased since it is impossible to erase a single WL.

For the D-Flash bank, the same WL can be programmed twice before erasing is required as the Flash cells are able to withstand two gate disturbs. This means if the number of data bytes that needs to be written is smaller than the 32-byte minimum programming width, the user can opt to program this number of data bytes (x; where x can be any integer from 1 to 31) first and program the remaining bytes (32 - x) later. Hence, it is possible to program the same WL, for example, with 16 bytes of data two times (see **Figure 12**)

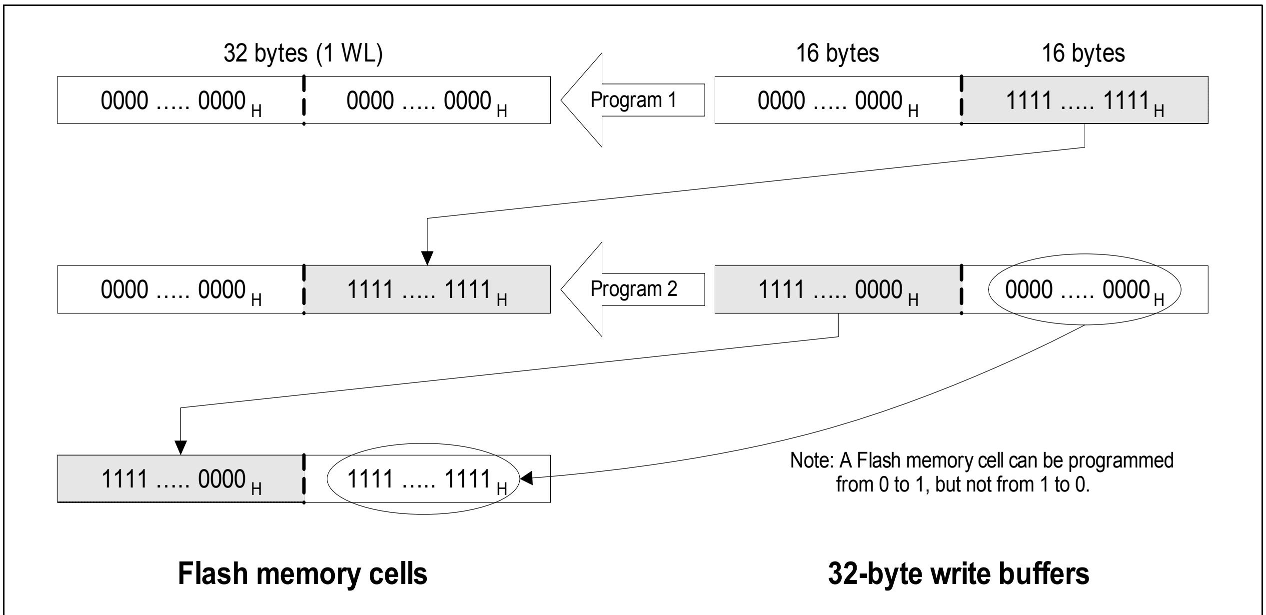

Figure 12 D-Flash Programming

Note: When programming a D-Flash WL the second time, the previously programmed Flash memory cells (whether 0s or 1s) should be reprogrammed with 0s to retain its original contents and to prevent "over-programming".

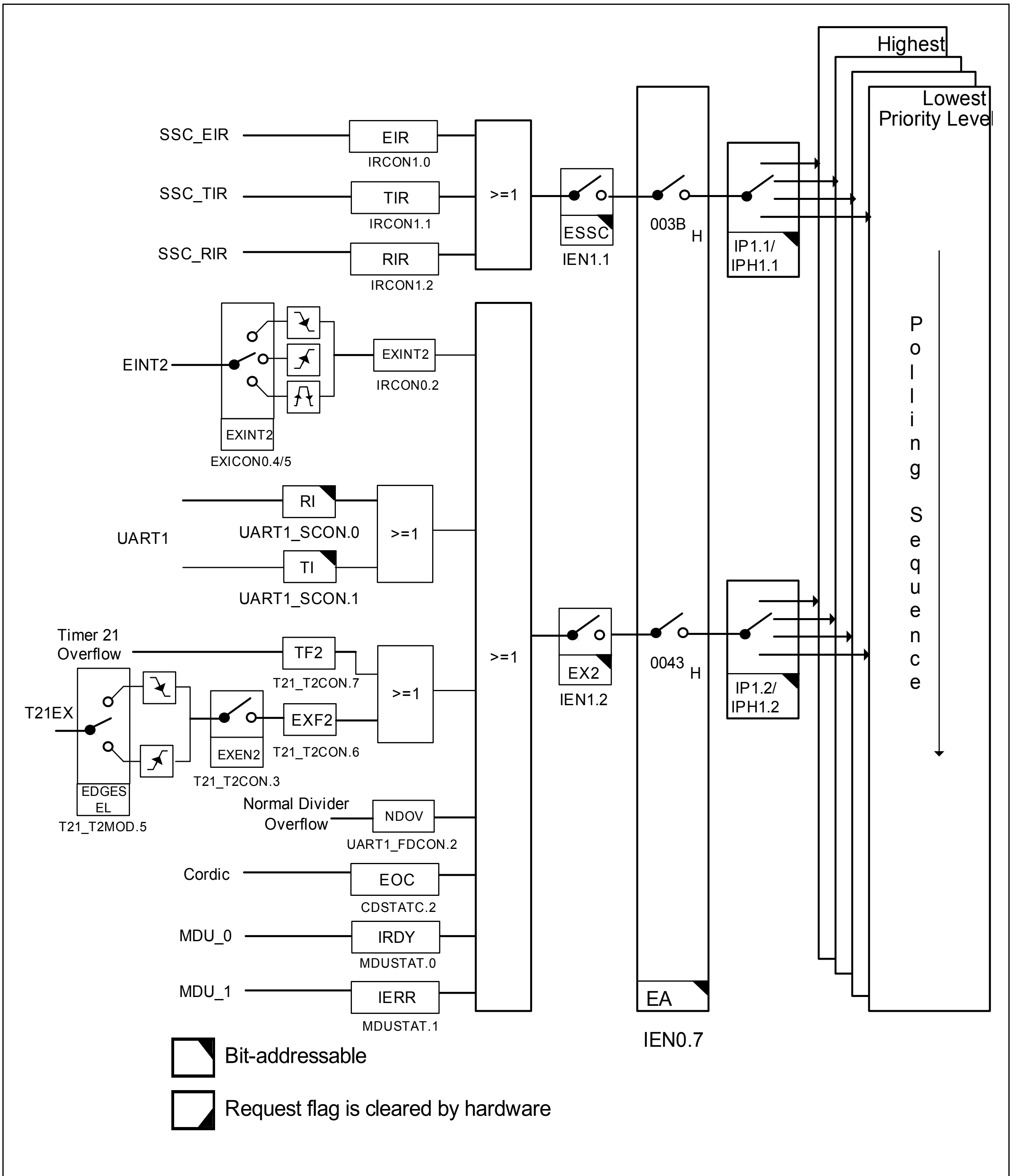

Figure 16 Interrupt Request Sources (Part 3)

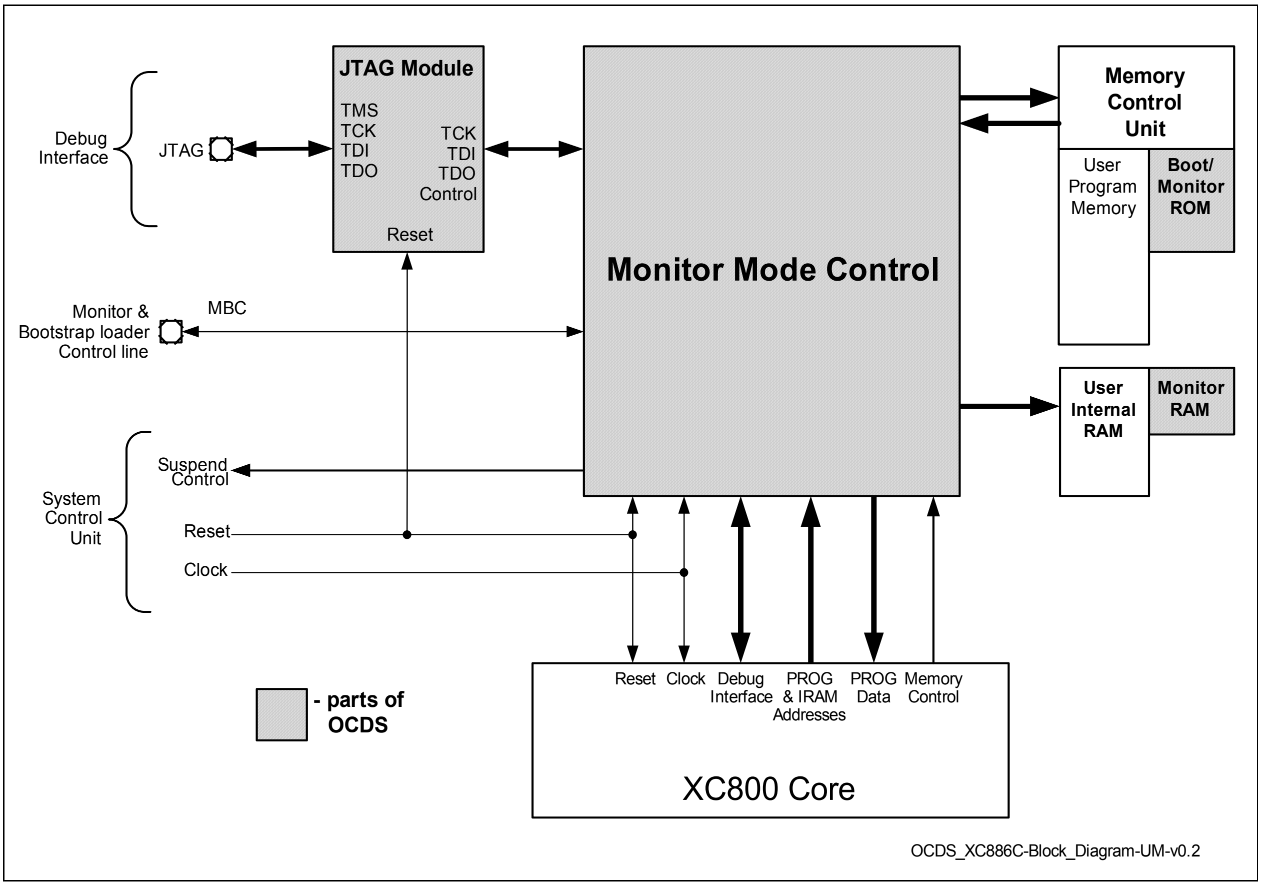

Figure 37 OCDS Block Diagram

3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC886/888 Flash devices are given in **Table 35**.

Table 35 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC886/888*-8FF	$1012\ 0083_H$
	XC886/888*-6FF	$1012\ 5083_H$
ROM	XC886/888*-8RF	$1013\ C083_H$
	XC886/888*-6RF	$1013\ D083_H$

Note: The asterisk (*) above denotes all possible device configurations.

Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage at XTAL1	V_{IHX}	SR	$0.7 \times V_{DDC}$	$V_{DDC} + 0.5$	V	
Pull-up current	I_{PU}	SR	–	-5	µA	$V_{IHP,min}$
			-50	–	µA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	5	µA	$V_{ILP,max}$
			50	–	µA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$[2]
Input current at XTAL1	I_{ILX}	CC	- 10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	[3]
Maximum current out of V_{SS}	I_{MVSS}	SR	–	120	mA	[3]

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 40 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Overload current coupling factor for digital I/O pins	K_{OVD}	CC	–	–	5.0 x 10^{-3}	–	$I_{OV} > 0$ [1)3)]
			–	–	1.0 x 10^{-2}	–	$I_{OV} < 0$ [1)3)]
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	20	pF	[1)4)]
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	5	7	pF	[1)5)]
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	[1)]
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	1.5	kΩ	[1)]

1) Not subjected to production test, verified by design/characterization

2) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DDP} = 5.0 V.

3) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ1}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

4) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

5) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

4.2.4 Power Supply Current

Table 41, **Table 42**, **Table 43** and **Table 44** provide the characteristics of the power supply current in the XC886/888.

Table 41 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	27.2	32.8	mA	Flash Device[3]
		24.3	29.8	mA	ROM Device[3]
Idle Mode	I_{DDP}	21.1	25.3	mA	Flash Device[4]
		18.2	21.6	mA	ROM Device[4]
Active Mode with slow-down enabled	I_{DDP}	14.1	17.0	mA	Flash Device[5]
		11.9	14.3	mA	ROM Device[5]
Idle Mode with slow-down enabled	I_{DDP}	11.7	15.0	mA	Flash Device[6]
		9.7	11.9	mA	ROM Device[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to 1001_B), $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to 0110_B, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to 0110_B, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

5.3 Quality Declaration

Table 2 shows the characteristics of the quality parameters in the XC886/888.

Table 2 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B[1)]
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C[1)]

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

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