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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc886lm-8ffa-5v-ac

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Summary of Features

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
 - PLL loss-of-lock detection
- Power saving modes
 - slow-down mode
 - idle mode
 - power-down mode with wake-up capability via RXD or EXINT0
 - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Six ports
 - Up to 48 pins as digital I/O
 - 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Four 16-bit timers
 - Timer 0 and Timer 1 (T0 and T1)
 - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- Software libraries to support floating point and MDU calculations
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Capture/compare unit for PWM signal generation (CCU6)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
 - 1 Kbyte of monitor ROM (part of the 12-Kbyte Boot ROM)
 - 64 bytes of monitor RAM
- Packages:
 - PG-TQFP-48
 - PG-TQFP-64
- Temperature range *T*_A:
 - SAF (-40 to 85 °C)
 - SAK (-40 to 125 °C)



General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function				
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.				
P1.0	26/34		PU	RXD_0 T2EX RXDC0_0	UART Receive Data Input Timer 2 External Trigger Input MultiCAN Node 0 Receiver Input			
P1.1	27/35		PU	EXINT3 T0_1 TDO_1 TXD_0 TXDC0_0	External Interrupt Input 3 Timer 0 Input JTAG Serial Data Output UART Transmit Data Output/Clock Output MultiCAN Node 0 Transmitter Output			
P1.2	28/36		PU	SCK_0	SSC Clock Input/Output			
P1.3	29/37		PU	MTSR_0 TXDC1_3	SSC Master Transmit Output/Slave Receive Input MultiCAN Node 1 Transmitter Output			
P1.4	30/38		PU	MRST_0 EXINT0_1 RXDC1_3	SSC Master Receive Input/ Slave Transmit Output External Interrupt Input 0 MultiCAN Node 1 Receiver Input			
P1.5	31/39		PU	CCPOS0_1 EXINT5 T1_1 EXF2_0 RXDO_0	CCU6 Hall Input 0 External Interrupt Input 5 Timer 1 Input Timer 2 External Flag Output UART Transmit Data Output			

Table 3Pin Definitions and Functions (cont'd)



XC886/888CLM

General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function	
P3		I/O		Port 3 Port 3 is an 8 I/O port. It ca for CCU6, U/	B-bit bidirectional general purpose on be used as alternate functions ART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CC61_2 COUT60_0	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare
				TXD1_1	UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 TXDC1_1	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 RXDC0_1 T2EX1_0	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 EXF21_0 TXDC0_1	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	CTRAP 0	CCU6 Trap Input

Table 3Pin Definitions and Functions (cont'd)



3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_{H} to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.



 Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE

(this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)



Figure 10 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC886/888 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers



3.2.3.1 Password Register

PASSWD

Password	d Register					Reset '	Value: 07 _H
7	6	5	4	3	2	1	0
	1	PASS	I	1	PROTECT _S	мо	DE
		wh	•		rh	۳	N

Field	Bits	Туре	Description	
MODE	[1:0]	rw	 Bit Protection Scheme Control Bits 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others:Scheme Enabled. These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B; only then, will the MODE[1:0] be registered. 	
PROTECT_S	2	rh	 Bit Protection Signal Status Bit This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits. 	
PASS	[7:3]	wh	Password BitsThe Bit Protection Scheme only recognizes threepatterns. 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits	



3.3.3 Flash Programming Width

For the P-Flash banks, a programmed wordline (WL) must be erased before it can be reprogrammed as the Flash cells can only withstand one gate disturb. This means that the entire sector containing the WL must be erased since it is impossible to erase a single WL.

For the D-Flash bank, the same WL can be programmed twice before erasing is required as the Flash cells are able to withstand two gate disturbs. This means if the number of data bytes that needs to be written is smaller than the 32-byte minimum programming width, the user can opt to program this number of data bytes (x; where x can be any integer from 1 to 31) first and program the remaining bytes (32 - x) later. Hence, it is possible to program the same WL, for example, with 16 bytes of data two times (see **Figure 12**)



Figure 12 D-Flash Programming

Note: When programming a D-Flash WL the second time, the previously programmed Flash memory cells (whether 0s or 1s) should be reprogrammed with 0s to retain its original contents and to prevent "over-programming".







Functional Description

Table 20	Interrupt Vector Addresses (cont'd)										
Interrupt Source	Vector Address	Assignment for XC886/888	Enable Bit	SFR							
XINTR6	0033 _H	MultiCAN Nodes 1 and 2	EADC	IEN1							
		ADC[1:0]									
XINTR7	003B _H	SSC	ESSC								
XINTR8	0043 _H	External Interrupt 2	EX2								
		T21									
		CORDIC									
		UART1									
		UART1 Fractional Divider (Normal Divider Overflow)									
		MDU[1:0]									
XINTR9	004B _H	External Interrupt 3	EXM								
		External Interrupt 4									
		External Interrupt 5	ernal Interrupt 5								
		External Interrupt 6									
		MultiCAN Node 3									
XINTR10	0053 _H	CCU6 INP0	ECCIP0								
		MultiCAN Node 4									
XINTR11	005B _H	CCU6 INP1	ECCIP1								
		MultiCAN Node 5									
XINTR12	0063 _H	CCU6 INP2	ECCIP2								
		MultiCAN Node 6									
XINTR13	006B _H	CCU6 INP3	ECCIP3								
		MultiCAN Node 7									



3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys} . During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.



Figure 26 Clock Generation from f_{sys}



- Interrupt enabling and corresponding flag

3.13 UART and UART1

The XC886/888 provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
 - 8-bit or 9-bit data frames, LSB first
 - Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 29**.

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	f _{PCLK} /2
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{\rm PCLK}/32 \text{ or } f_{\rm PCLK}/64^{1)}$
Mode 3: 9-bit shift UART	Variable

Table 29UART Modes

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{\rm PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{\rm PCLK}/32$ or $f_{\rm PCLK}/64$. For UART1 module, only $f_{\rm PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and



needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data. The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

- STEP 4: Enter for Master Request Frame or for Slave Response Frame
- Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.



3.18 Timer 2 and Timer 21

Timer 2 and Timer 21 are 16-bit general purpose timers (THL2) that are fully compatible and have two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode, see **Table 33**. As a timer, the timers count with an input clock of PCLK/12 (if prescaler is disabled). As a counter, they count 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is PCLK/24 (if prescaler is disabled).

Table 33	Timer 2 Modes							
Mode	Description							
Auto-reload	 Up/Down Count Disabled Count up only Start counting from 16-bit reload value, overflow at FFFF_H Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well Programmble reload value in register RC2 Interrupt is generated with reload event Up/Down Count Enabled Count up or down, direction determined by level at input pin T2EX No interrupt is generated Count up Start counting from 16-bit reload value, overflow at FFFF_H Reload event triggered by overflow condition Programmble reload value in register RC2 Count up Start counting from 16-bit reload value, overflow at FFFF_H Reload event triggered by overflow condition Programmble reload value in register RC2 Count down Start counting from FFFF_H, underflow at value defined in register RC2 Reload event triggered by underflow condition Reload event triggered by underflow condition Reload event triggered by underflow condition 							
Channel capture	 Count up only Start counting from 0000_H, overflow at FFFF_H Reload event triggered by overflow condition Reload value fixed at 0000_H Capture event triggered by falling/rising edge at pin T2EX Captured timer value stored in register RC2 Interrupt is generated with reload or capture event 							



Electrical Parameters

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC886/888.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC886/888 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

• CC

These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC886/888 and must be regarded for a system design.

• SR

These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC886/888 is designed in.



Electrical Parameters

4.3.2 Output Rise/Fall Times

Table 45 provides the characteristics of the output rise/fall times in the XC886/888.

Table 45 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	L Va	imit alues	Unit	Test Conditions	
		min.	max.			
V_{DDP} = 5V Range						
Rise/fall times	t _R , t _F	_	10	ns	20 pF. ¹⁾²⁾³⁾	
V _{DDP} = 3.3V Range						
Rise/fall times	t _R , t _F	-	10	ns	20 pF. ¹⁾²⁾⁴⁾	
					1	

1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) Additional rise/fall time valid for $C_{\rm L}$ = 20pF - 100pF @ 0.125 ns/pF.

4) Additional rise/fall time valid for $C_{\rm L}$ = 20pF - 100pF @ 0.225 ns/pF.



Figure 43 Rise/Fall Times Parameters



Electrical Parameters

4.3.5 External Clock Drive XTAL1

Table 48 shows the parameters that define the external clock supply for XC886/888. These timing parameters are based on the direct XTAL1 drive of clock input signals. They are not applicable if an external crystal or ceramic resonator is considered.

Symbol	Symbol		Values	Unit	Test Conditions	
		Min.	Max.			
t _{osc}	SR	83.3	250	ns	1)2)	
<i>t</i> ₁	SR	25	-	ns	2)3)	
<i>t</i> ₂	SR	25	-	ns	2)3)	
t ₃	SR	-	20	ns	2)3)	
<i>t</i> ₄	SR	-	20	ns	2)3)	
	Symbol t_{osc} t_1 t_2 t_3 t_4	Symbol t_{osc} SR t_1 SR t_2 SR t_3 SR t_4 SR	Symbol Limit t_{osc} SR 83.3 t_1 SR 25 t_2 SR 25 t_3 SR - t_4 SR -	Symbol Limit \vee lues Min. Max. t_{osc} SR 83.3 250 t_1 SR 25 - t_2 SR 25 - t_3 SR - 20 t_4 SR - 20	Symbol Limit $>$ lues Unit $Min.$ Max. 1 t_{osc} SR 83.3 250 ns t_1 SR 25 - ns t_2 SR 25 - ns t_3 SR - 20 ns t_4 SR - 20 ns	

 Table 48
 External Clock Drive Characteristics (Operating Conditions apply)

1) The clock input signals with 45-55% duty cycle are used.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) The clock input signal must reach the defined levels $V_{\rm ILX}$ and $V_{\rm IHX}$.



Figure 45 External Clock Drive XTAL1



Package and Quality Declaration

5 Package and Quality Declaration

Chapter 5 provides the information of the XC886/888 package and reliability section.

5.1 Package Parameters

Table 1 provides the thermal characteristics of the package used in XC886 and XC888.

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
PG-TQFP-48 (XC886)	1			1	1	1
Thermal resistance junction case	R _{TJC} C	CC	-	13	K/W	1)2)
Thermal resistance junction lead	R _{TJL} C	CC	-	32.5	K/W	1)2)_
PG-TQFP-64 (XC888)		•				
Thermal resistance junction case	R _{TJC} C	CC	-	12.6	K/W	1)2)
Thermal resistance junction lead	R _{TJL} C	CC	-	33.4	K/W	1)2)
	1				I	

Table 1 Thermal Characteristics of the Packages

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}) , the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}) . The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) . The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by

a) simply adding only the two thermal resistances (junction lead and lead ambient), or

b) by taking all four resistances into account, depending on the precision needed.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.



Package and Quality Declaration





Figure 49 PG-TQFP-64 Package Outline

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