Infineon Technologies - SAF-XC888C-6FFA 5V AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc888c-6ffa-5v-ac

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC886/888.

2.1 Block Diagram

The block diagram of the XC886/888 is shown in **Figure 2**.

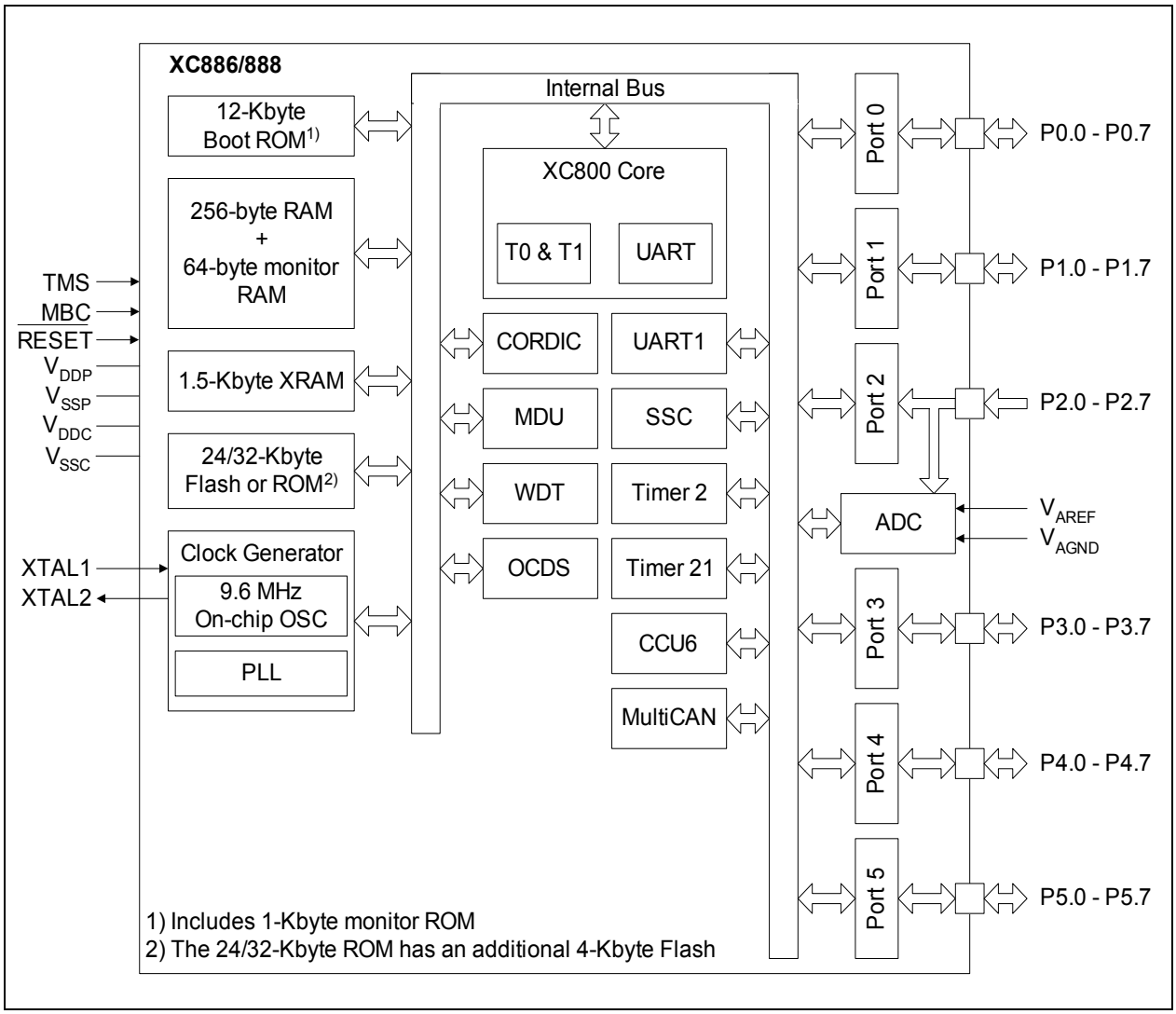


Figure 2 XC886/888 Block Diagram

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P1.6	8/10		PU	CCPOS1_1 CCU6 Hall Input 1 T12HR_0 CCU6 Timer 12 Hardware Run Input EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	9/11		PU	CCPOS2_1 CCU6 Hall Input 2 T13HR_0 CCU6 Timer 13 Hardware Run Input T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

Table 9 WDT Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_DATA** **Reset: 00_H** P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_DIR** **Reset: 00_H** P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A0_H$	**P2_DATA** **Reset: 00_H** P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_DIR** **Reset: 00_H** P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_DATA** **Reset: 00_H** P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_DIR** **Reset: 00_H** P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CC_H	**ADC_CHINSR Reset: 00_H** Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w
CD_H	**ADC_CHINPR Reset: 00_H** Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE_H	**ADC_EVINFR Reset: 00_H** Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF_H	**ADC_EVINCR Reset: 00_H** Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
$D2_H$	**ADC_EVINSR Reset: 00_H** Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
$D3_H$	**ADC_EVINPR Reset: 00_H** Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA_H	**ADC_CRCR1 Reset: 00_H** Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB_H	**ADC_CRPR1 Reset: 00_H** Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC_H	**ADC_CRMR1 Reset: 00_H** Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD_H	**ADC_QMR0 Reset: 00_H** Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE_H	**ADC_QSR0 Reset: 20_H** Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF_H	**ADC_Q0R0 Reset: 00_H** Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QBUR0 Reset: 00_H** Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
$D2_H$	**ADC_QINR0 Reset: 00_H** Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Table 13 T21 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T21_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A3_H$	**CCU6_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
$9A_H$	**CCU6_CC63SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 Low	Bit Field	CC63SL							
		Type	rw							
$9B_H$	**CCU6_CC63SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 High	Bit Field	CC63SH							
		Type	rw							
$9C_H$	**CCU6_TCTR4L** **Reset: 00_H** Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	0		DT RES	T12 RES	T12R S	T12R R
		Type	w	w	r		w	w	w	w
$9D_H$	**CCU6_TCTR4H** **Reset: 00_H** Timer Control Register 4 High	Bit Field	T13 STD	T13 STR	0			T13 RES	T13R S	T13R R
		Type	w	w	r			w	w	w
$9E_H$	**CCU6_MCMOUTSL** **Reset: 00_H** Multi-Channel Mode Output Shadow Register Low	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
$9F_H$	**CCU6_MCMOUTSH** **Reset: 00_H** Multi-Channel Mode Output Shadow Register High	Bit Field	STRH P	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
$A4_H$	**CCU6_ISRL** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register Low	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISRH** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register High	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
$A6_H$	**CCU6_CMPMODIFL** **Reset: 00_H** Compare State Modification Register Low	Bit Field	0	MCC6 3S	0			MCC6 2S	MCC6 1S	MCC6 0S
		Type	r	w	r			w	w	w
$A7_H$	**CCU6_CMPMODIFH** **Reset: 00_H** Compare State Modification Register High	Bit Field	0	MCC6 3R	0			MCC6 2R	MCC6 1R	MCC6 0R
		Type	r	w	r			w	w	w

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FA_H	**CCU6_CC60SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 Low	Bit Field	CC60SL							
		Type	rwh							
FB_H	**CCU6_CC60SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 High	Bit Field	CC60SH							
		Type	rwh							
FC_H	**CCU6_CC61SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 Low	Bit Field	CC61SL							
		Type	rwh							
FD_H	**CCU6_CC61SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 High	Bit Field	CC61SH							
		Type	rwh							
FE_H	**CCU6_CC62SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 Low	Bit Field	CC62SL							
		Type	rwh							
FF_H	**CCU6_CC62SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 High	Bit Field	CC62SH							
		Type	rwh							
RMAP = 0, PAGE 1										
$9A_H$	**CCU6_CC63RL Reset: 00_H** Capture/Compare Register for Channel CC63 Low	Bit Field	CC63VL							
		Type	rh							
$9B_H$	**CCU6_CC63RH Reset: 00_H** Capture/Compare Register for Channel CC63 High	Bit Field	CC63VH							
		Type	rh							
$9C_H$	**CCU6_T12PRL Reset: 00_H** Timer T12 Period Register Low	Bit Field	T12PVL							
		Type	rwh							
$9D_H$	**CCU6_T12PRH Reset: 00_H** Timer T12 Period Register High	Bit Field	T12PVH							
		Type	rwh							
$9E_H$	**CCU6_T13PRL Reset: 00_H** Timer T13 Period Register Low	Bit Field	T13PVL							
		Type	rwh							
$9F_H$	**CCU6_T13PRH Reset: 00_H** Timer T13 Period Register High	Bit Field	T13PVH							
		Type	rwh							
$A4_H$	**CCU6_T12DTCL Reset: 00_H** Dead-Time Control Register for Timer T12 Low	Bit Field	DTM							
		Type	rw							
$A5_H$	**CCU6_T12DTCH Reset: 00_H** Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0
		Type	r	rh	rh	rh	r	rw	rw	rw
$A6_H$	**CCU6_TCTR0L Reset: 00_H** Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE12	T12R	T12PRE	T12CLK		
		Type	rw	rh	rh	rh	rw	rw		
$A7_H$	**CCU6_TCTR0H Reset: 00_H** Timer Control Register 0 High	Bit Field	0		STE13	T13R	T13PRE	T13CLK		
		Type	r		rh	rh	rw	rw		
FA_H	**CCU6_CC60RL Reset: 00_H** Capture/Compare Register for Channel CC60 Low	Bit Field	CC60VL							
		Type	rh							

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FE_H	**CCU6_CMPSTATL Reset: 00_H** Compare State Register Low	Bit Field	0	CC63 ST	CC POS2	CC POS1	CC POS0	CC62 ST	CC61 ST	CC60 ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT 63PS	COUT 62PS	CC62 PS	COUT 61PS	CC61 PS	COUT 60PS	CC60 PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C8_H$	**SCON Reset: 00_H** Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
$C9_H$	**SBUF Reset: 00_H** Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
CA_H	**BCON Reset: 00_H** Baud Rate Control Register	Bit Field	0				BRPRE			R
		Type	r				rw			rw
CB_H	**BG Reset: 00_H** Baud Rate Timer/Reload Register	Bit Field	BR_VALUE							
		Type	rwh							
CC_H	**FDCON Reset: 00_H** Fractional Divider Control Register	Bit Field	0					NDOV	FDM	FDEN
		Type	r					rwh	rw	rw
CD_H	**FDSTEP Reset: 00_H** Fractional Divider Reload Register	Bit Field	STEP							
		Type	rw							
CE_H	**FDRES Reset: 00_H** Fractional Divider Result Register	Bit Field	RESULT							
		Type	rh							

Table 17 CAN Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
DB_H	**DATA0** **Reset: 00_H** CAN Data Register 0	Bit Field	CD							
		Type	rwh							
DC_H	**DATA1** **Reset: 00_H** CAN Data Register 1	Bit Field	CD							
		Type	rwh							
DD_H	**DATA2** **Reset: 00_H** CAN Data Register 2	Bit Field	CD							
		Type	rwh							
DE_H	**DATA3** **Reset: 00_H** CAN Data Register 3	Bit Field	CD							
		Type	rwh							

3.2.4.14 OCDS Registers

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 18 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$E9_H$	**MMCR2** **Reset: $1U_H$** Monitor Mode Control 2 Register	Bit Field	STMODE	EXBC	DSUSP	MBCON	ALTDI	MMEP	MMODE	JENA
		Type	rw	rw	rw	rwh	rw	rwh	rh	rh
$F1_H$	**MMCR** **Reset: 00_H** Monitor Mode Control Register	Bit Field	MEXIT_P	MEXIT	0	MSTEP	MRAMS_P	MRAMS	TRF	RRF
		Type	w	rwh	r	rw	w	rwh	rh	rh
$F2_H$	**MMSR** **Reset: 00_H** Monitor Mode Status Register	Bit Field	MBCAM	MBCIN	EXBF	SWBF	HWB3F	HWB2F	HWB1F	HWB0F
		Type	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
$F3_H$	**MMBPCR** **Reset: 00_H** Breakpoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1C	HWB0C	
		Type	rw	rw		rw		rw	rw	
$F4_H$	**MMICR** **Reset: 00_H** Monitor Mode Interrupt Control Register	Bit Field	DVECT	DRETR	COMRST	MSTSEL	MMUIE_P	MMUIE	RRIE_P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
$F5_H$	**MMDR** **Reset: 00_H** Monitor Mode Data Transfer Register Receive	Bit Field	MMRR							
		Type	rh							
$F6_H$	**HWBPSR** **Reset: 00_H** Hardware Breakpoints Select Register	Bit Field	0			BPSEL_P	BPSEL			
		Type	r			w	rw			
$F7_H$	**HWBPDR** **Reset: 00_H** Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							
EB_H	**MMWR1** **Reset: 00_H** Monitor Work Register 1	Bit Field	MMWR1							
		Type	rw							

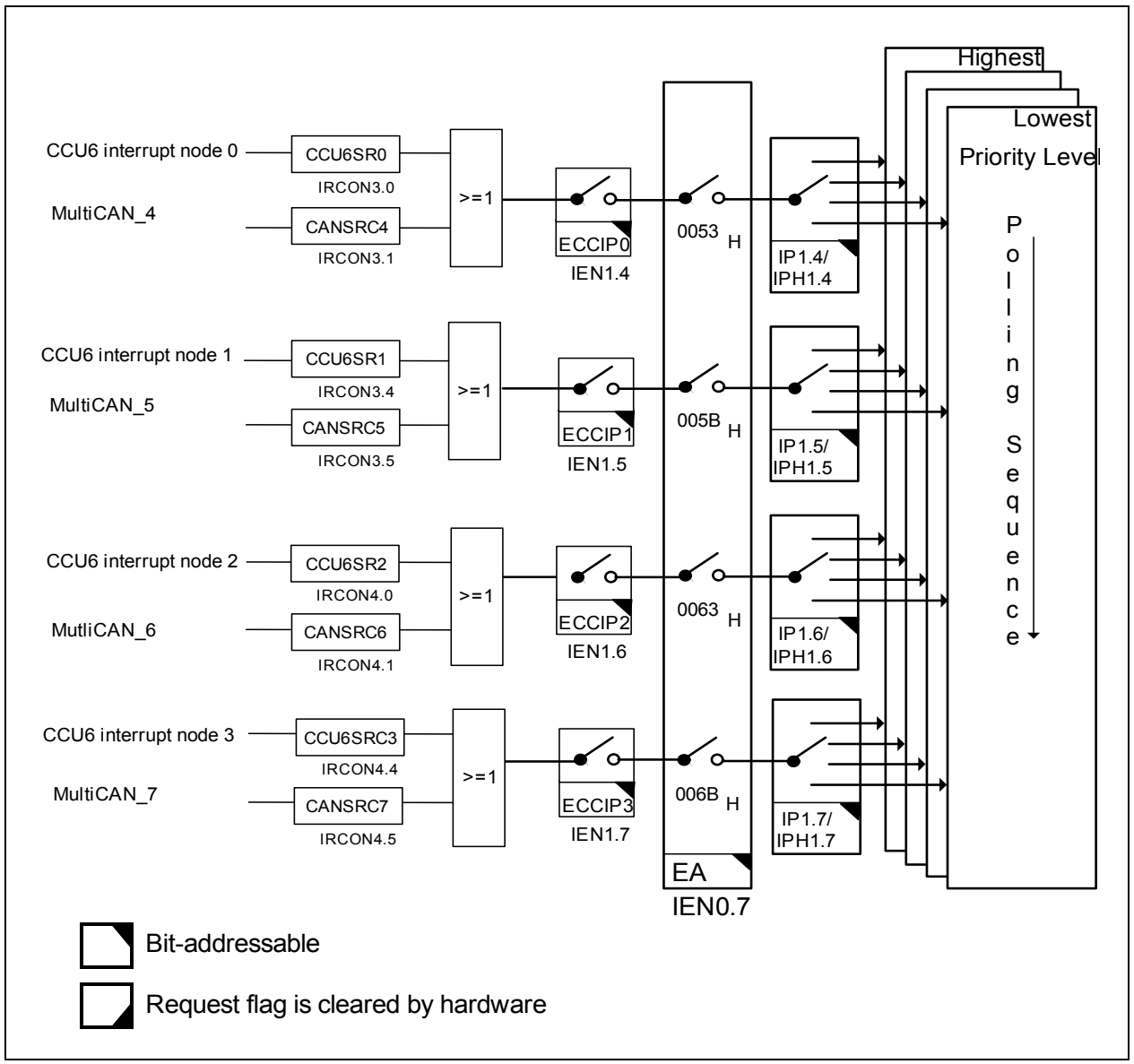


Figure 18 Interrupt Request Sources (Part 5)

3.6 Power Supply System with Embedded Voltage Regulator

The XC886/888 microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

Figure 21 shows the XC886/888 power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

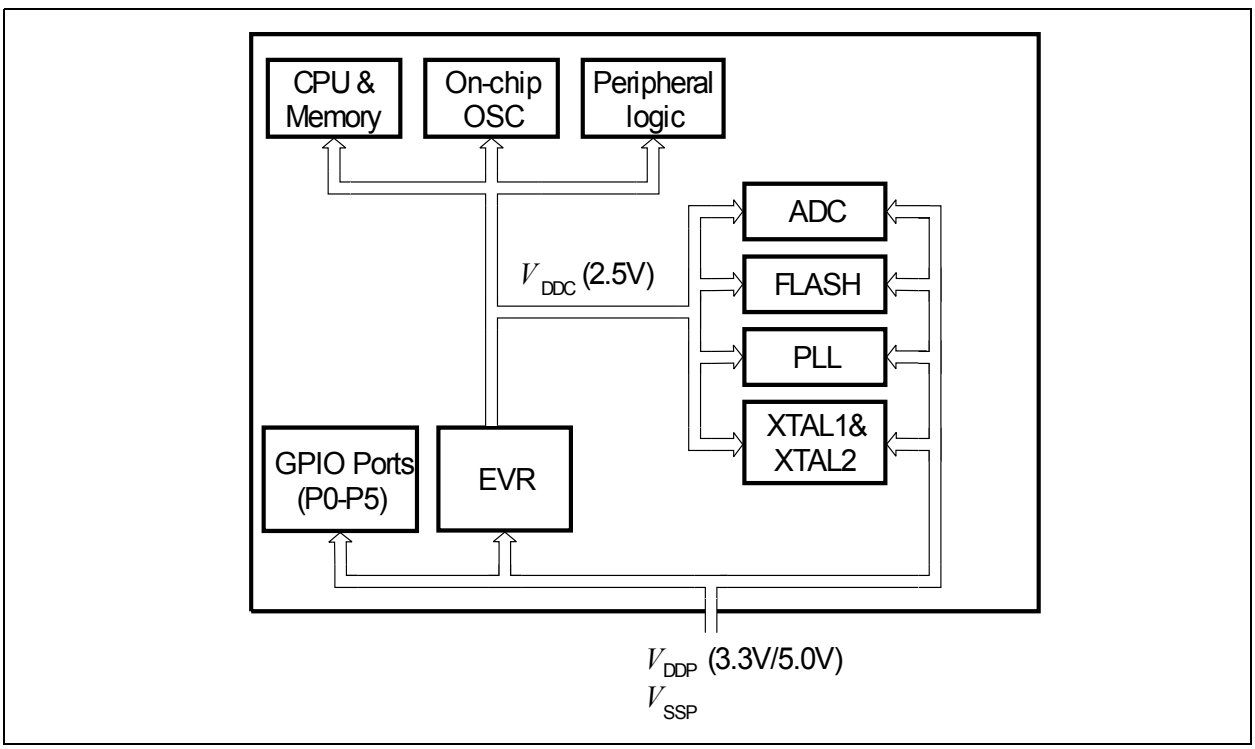


Figure 21 XC886/888 Power Supply System

EVR Features

- Input voltage (V_{DDP}): 3.3 V/5.0 V
- Output voltage (V_{DDC}): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode
- V_{DDC} and V_{DDP} prewarning detection
- V_{DDC} brownout detection

1) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
2) OSC is bypassed in MultiCAN BSL mode
3) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC886/888. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC886/888, the oscillator can be from either of these two sources: the on-chip oscillator (9.6 MHz) or the external oscillator (4 MHz to 12 MHz). The term “oscillator” is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default.The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

Table 31 Deviation Error for UART with Fractional Divider enabled

f_{PCLK}	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
24 MHz	1	10 (A_H)	197 ($C5_H$)	+0.20 %
12 MHz	1	6 (6_H)	236 (EC_H)	+0.03 %
8 MHz	1	4 (4_H)	236 (EC_H)	+0.03 %
6 MHz	1	3 (3_H)	236 (EC_H)	+0.03 %

3.13.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

$$\text{Mode 1, 3 baud rate} = \frac{2^{SMOD} \times f_{PCLK}}{32 \times 2 \times (256 - TH1)} \quad (3.7)$$

3.14 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 30**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV}, where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP} \quad (3.8)$$

needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data. The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

STEP 4: Enter for Master Request Frame or for Slave Response Frame

*Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.*

3.21 Analog-to-Digital Converter

The XC886/888 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features

- Successive approximation
- 8-bit or 10-bit resolution
  (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access
  (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- Limit checking for conversion results
- Data reduction filter
  (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register

Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	**AB-Step**	**AC-Step**
XC886-6FFA 3V3	-	$095D1562_H$	$0B5D1562_H$
XC888-6FFA 3V3	-	$095D1563_H$	$0B5D1563_H$
XC886CLM-8FFA 5V	-	09900102_H	$0B900102_H$
XC888CLM-8FFA 5V	-	09900103_H	$0B900103_H$
XC886LM-8FFA 5V	-	09900122_H	$0B900122_H$
XC888LM-8FFA 5V	-	09900123_H	$0B900123_H$
XC886CLM-6FFA 5V	-	09951502_H	$0B951502_H$
XC888CLM-6FFA 5V	-	09951503_H	$0B951503_H$
XC886LM-6FFA 5V	-	09951522_H	$0B951522_H$
XC888LM-6FFA 5V	-	09951523_H	$0B951523_H$
XC886CM-8FFA 5V	-	09980102_H	$0B980102_H$
XC888CM-8FFA 5V	-	09980103_H	$0B980103_H$
XC886C-8FFA 5V	-	09980142_H	$0B980142_H$
XC888C-8FFA 5V	-	09980143_H	$0B980143_H$
XC886-8FFA 5V	-	09980162_H	$0B980162_H$
XC888-8FFA 5V	-	09980163_H	$0B980163_H$
XC886CM-6FFA 5V	-	$099D1502_H$	$0B9D1502_H$
XC888CM-6FFA 5V	-	$099D1503_H$	$0B9D1503_H$
XC886C-6FFA 5V	-	$099D1542_H$	$0B9D1542_H$
XC888C-6FFA 5V	-	$099D1543_H$	$0B9D1543_H$
XC886-6FFA 5V	-	$099D1562_H$	$0B9D1562_H$
XC888-6FFA 5V	-	$099D1563_H$	$0B9D1563_H$
ROM Devices			
XC886CLM-8RFA 3V3	22400502_H	-	-
XC888CLM-8RFA 3V3	22400503_H	-	-
XC886LM-8RFA 3V3	22400522_H	-	-
XC888LM-8RFA 3V3	22400523_H	-	-
XC886CLM-6RFA 3V3	22411502_H	-	-
XC888CLM-6RFA 3V3	22411503_H	-	-

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Characteristics

Table 38 provides the characteristics of the input/output pins of the XC886/888.

Table 38 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
V_{DDP} = 5 V Range						
Output low voltage	V_{OL}	CC	–	1.0	V	I_{OL} = 15 mA
			–	1.0	V	I_{OL} = 5 mA, current into all pins > 60 mA
			–	0.4	V	I_{OL} = 5 mA, current into all pins ≤ 60 mA
Output high voltage	V_{OH}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -15 mA
			V_{DDP} - 1.0	–	V	I_{OH} = -5 mA, current from all pins > 60 mA
			V_{DDP} - 0.4	–	V	I_{OH} = -5 mA, current from all pins ≤ 60 mA
Input low voltage on port pins (all except P0.0 & P0.1)	V_{ILP}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on P0.0 & P0.1	V_{ILP0}	SR	-0.2	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on $\overline{\text{RESET}}$ pin	V_{ILR}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input low voltage on TMS pin	V_{ILT}	SR	–	0.3 × V_{DDP}	V	CMOS Mode
Input high voltage on port pins (all except P0.0 & P0.1)	V_{IHP}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on P0.0 & P0.1	V_{IHP0}	SR	0.7 × V_{DDP}	V_{DDP}	V	CMOS Mode

Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage on RESET pin	V_{IHR}	SR	0.7 × V_{DDP}	–	V	CMOS Mode
Input high voltage on TMS pin	V_{IHT}	SR	0.75 × V_{DDP}	–	V	CMOS Mode
Input Hysteresis on port pins	$HYSP$	CC	0.07 × V_{DDP}	–	V	CMOS Mode[1)]
Input Hysteresis on XTAL1	$HYSX$	CC	0.07 × V_{DDC}	–	V	[1)]
Input low voltage at XTAL1	V_{ILX}	SR	V_{SS} - 0.5	0.3 × V_{DDC}	V	
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	–	-10	µA	$V_{IHP,min}$
			-150	–	µA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	10	µA	$V_{ILP,max}$
			150	–	µA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$[2)]
Input current at XTAL1	I_{ILX}	CC	-10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3)]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4)]
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	[3)]

Table 40 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Overload current coupling factor for digital I/O pins	K_{OVD}	CC	–	–	5.0 x 10^{-3}	–	$I_{OV} > 0$ 1)3)
			–	–	1.0 x 10^{-2}	–	$I_{OV} < 0$ 1)3)
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	20	pF	1)4)
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	5	7	pF	1)5)
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	1)
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	1.5	kΩ	1)

1) Not subjected to production test, verified by design/characterization

2) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DDP} = 5.0 V.

3) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ1}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

4) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

5) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

4.3.4 On-Chip Oscillator Characteristics

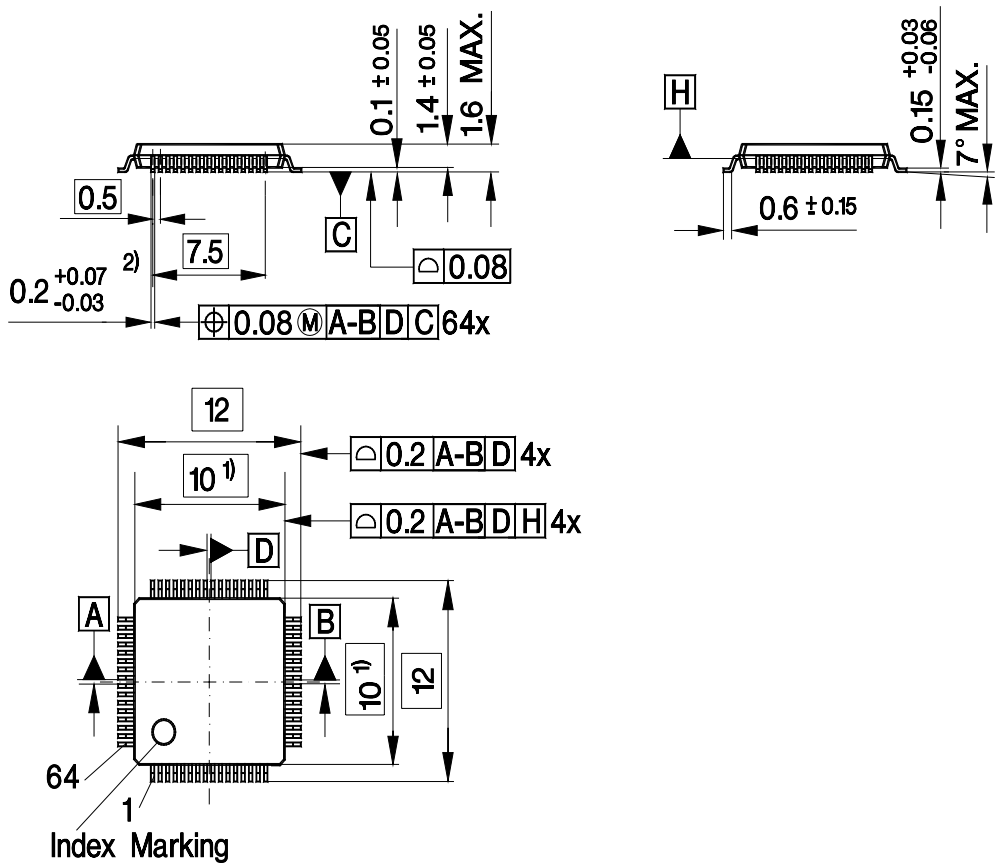
Table 47 provides the characteristics of the on-chip oscillator in the XC886/888.

Table 47 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM}	CC	9.36	9.6	9.84	MHz	under nominal conditions[1]
Long term frequency deviation	Δf_{LT}	CC	-5.0	–	5.0	%	with respect to f_{NOM}, over lifetime and temperature (-10°C to 125°C), for one given device after trimming
			-6.0	–	0	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to -10°C), for one given device after trimming
Short term frequency deviation	Δf_{ST}	CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

Figure 49 shows the package outlines of the XC888.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Figure 49 PG-TQFP-64 Package Outline