Infineon Technologies - SAF-XC888C-8FFI 3V3 AC Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc888c-8ffi-3v3-ac

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC886/888.

2.1 Block Diagram

The block diagram of the XC886/888 is shown in **Figure 2**.

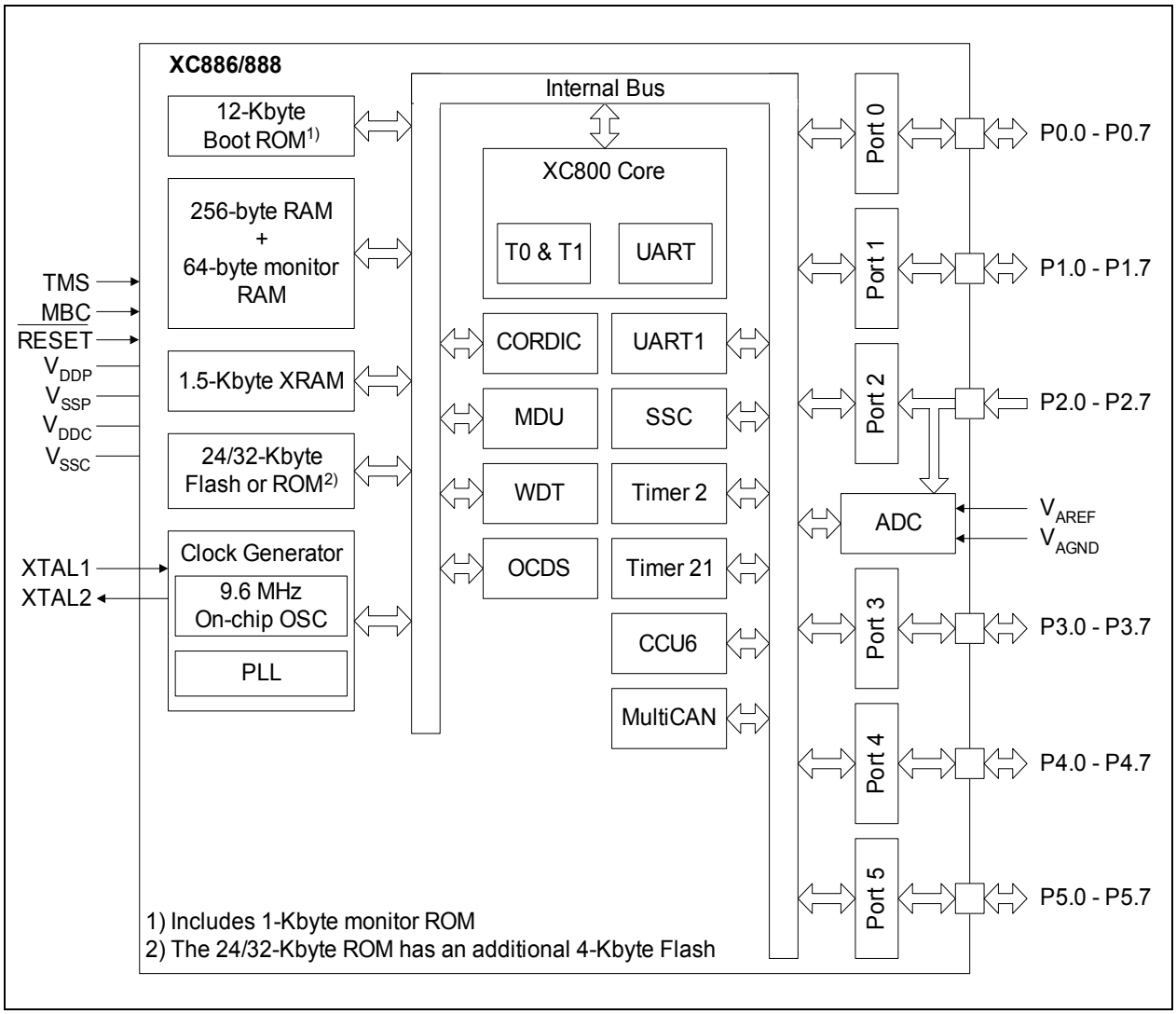


Figure 2 XC886/888 Block Diagram

2.4 Pin Definitions and Functions

The functions and default states of the XC886/888 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P0		I/O		**Port 0** Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, Timer 2, Timer 21, MultiCAN and SSC.
P0.0	11/17		Hi-Z	TCK_0 JTAG Clock Input T12HR_1 CCU6 Timer 12 Hardware Run Input CC61_1 Input/Output of Capture/Compare channel 1 CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	13/21		Hi-Z	TDI_0 JTAG Serial Data Input T13HR_1 CCU6 Timer 13 Hardware Run Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input COUT61_1 Output of Capture/Compare channel 1 EXF2_1 Timer 2 External Flag Output
P0.2	12/18		PU	$\overline{\text{CTRAP}}$_2 CCU6 Trap Input TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output
P0.3	48/63		Hi-Z	SCK_1 SSC Clock Input/Output COUT63_1 Output of Capture/Compare channel 3 RXDO1_0 UART1 Transmit Data Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P0.4	1/64		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
				TXD1_0	UART1 Transmit Data Output/Clock Output
P0.5	2/1		Hi-Z	MRST_1	SSC Master Receive Input/Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				T2EX1_1	Timer 21 External Trigger Input
				RXD1_0	UART1 Receive Data Input
				COUT62_1	Output of Capture/Compare channel 2
P0.6	–/2		PU	GPIO	
P0.7	47/62		PU	CLKOUT_1	Clock Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P5		I/O		**Port 5** Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1 and JTAG.	
P5.0	–/8		PU	EXINT1_1	External Interrupt Input 1
P5.1	–/9		PU	EXINT2_1	External Interrupt Input 2
P5.2	–/12		PU	RXD_2	UART Receive Data Input
P5.3	–/13		PU	TXD_2	UART Transmit Data Output/Clock Output
P5.4	–/14		PU	RXDO_2	UART Transmit Data Output
P5.5	–/15		PU	TDO_2 TXD1_2	JTAG Serial Data Output UART1 Transmit Data Output/ Clock Output
P5.6	–/19		PU	TCK_2 RXDO1_2	JTAG Clock Input UART1 Transmit Data Output
P5.7	–/20		PU	TDI_2 RXD1_2	JTAG Serial Data Input UART1 Receive Data Input

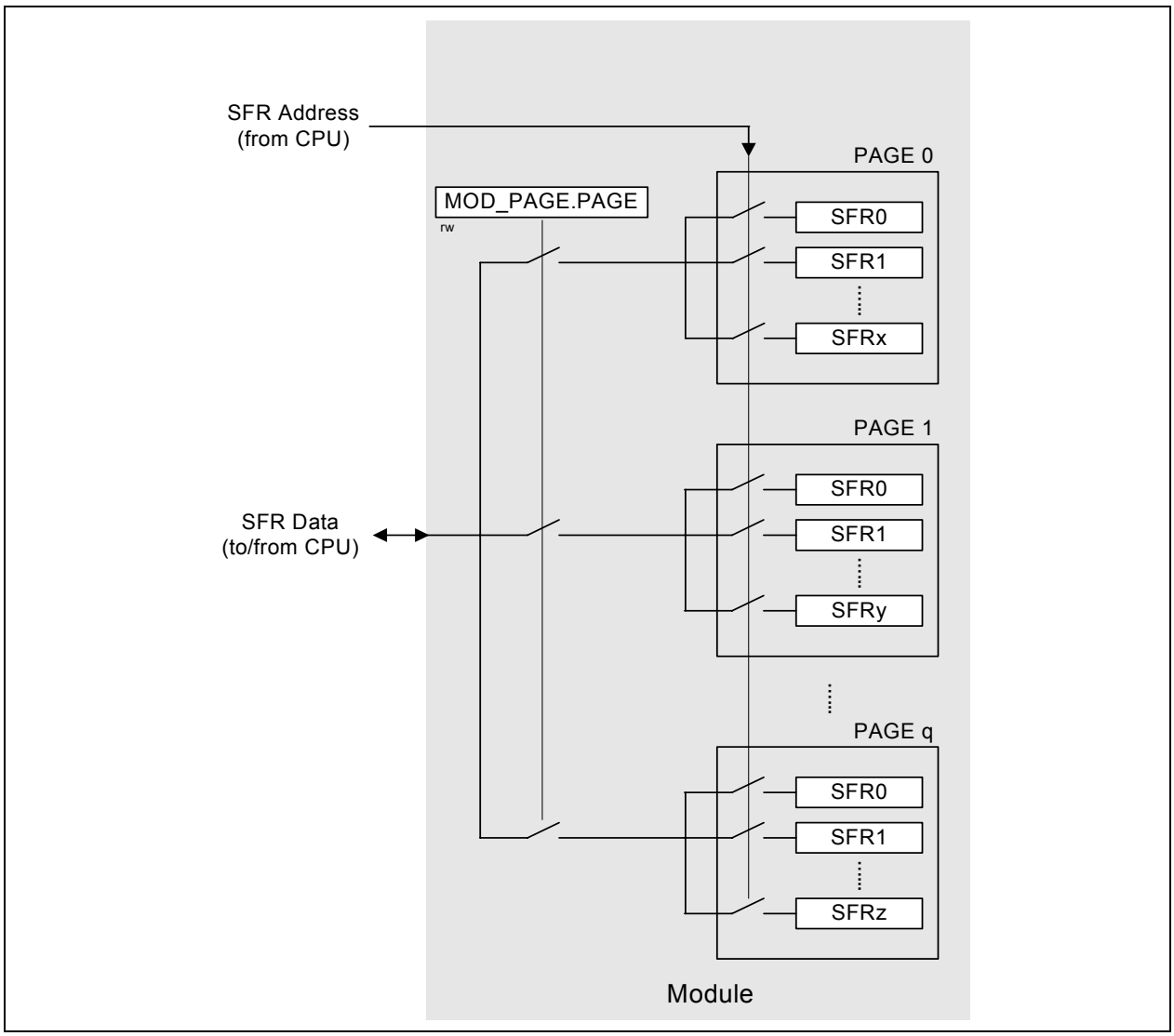


Figure 9 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

- Save the contents of PAGE in STx before overwriting with the new value
  (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or

Field	Bits	Type	Description
OP	[7:6]	w	**Operation** 0X Manual page mode. The value of STNR is ignored and PAGE is directly written. 10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR. 11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.
0	3	r	**Reserved** Returns 0 if read; should be written with 0.

3.2.3 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected bits (i.e., protected bits) using the PASSWD register. When the bit field MODE is 11_B, writing 10011_B to the bit field PASS opens access to writing of all protected bits, and writing 10101_B to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with 98_H or $A8_H$. It can only be changed when bit field PASS is written with 11000_B, for example, writing $D0_H$ to PASSWD register disables the bit protection scheme.

Note that access is opened for maximum 32 CCLKs if the “close access” password is not written. If “open access” password is written again before the end of 32 CCLK cycles, there will be a recount of 32 CCLK cycles. The protected bits include the N- and K-Divider bits, NDIV and KDIV; the Watchdog Timer enable bit, WDTEN; and the power-down and slow-down enable bits, PD and SD.

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FB_H	**CCU6_CC60RH** **Reset: 00_H** Capture/Compare Register for Channel CC60 High	Bit Field	CC60VH							
		Type	rh							
FC_H	**CCU6_CC61RL** **Reset: 00_H** Capture/Compare Register for Channel CC61 Low	Bit Field	CC61VL							
		Type	rh							
FD_H	**CCU6_CC61RH** **Reset: 00_H** Capture/Compare Register for Channel CC61 High	Bit Field	CC61VH							
		Type	rh							
FE_H	**CCU6_CC62RL** **Reset: 00_H** Capture/Compare Register for Channel CC62 Low	Bit Field	CC62VL							
		Type	rh							
FF_H	**CCU6_CC62RH** **Reset: 00_H** Capture/Compare Register for Channel CC62 High	Bit Field	CC62VH							
		Type	rh							
RMAP = 0, PAGE 2										
$9A_H$	**CCU6_T12MSELL** **Reset: 00_H** T12 Capture/Compare Mode Select Register Low	Bit Field	MSEL61				MSEL60			
		Type	rw				rw			
$9B_H$	**CCU6_T12MSELH** **Reset: 00_H** T12 Capture/Compare Mode Select Register High	Bit Field	DBYP	HSYNC			MSEL62			
		Type	rw	rw			rw			
$9C_H$	**CCU6_IENL** **Reset: 00_H** Capture/Compare Interrupt Enable Register Low	Bit Field	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$9D_H$	**CCU6_IENH** **Reset: 00_H** Capture/Compare Interrupt Enable Register High	Bit Field	ENSTR	ENIDLE	ENWHE	ENCHE	0	ENTRPF	ENT13PM	ENT13CM
		Type	rw	rw	rw	rw	r	rw	rw	rw
$9E_H$	**CCU6_INPL** **Reset: 40_H** Capture/Compare Interrupt Node Pointer Register Low	Bit Field	INPCHE		INPCC62		INPCC61		INPCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_INPH** **Reset: 39_H** Capture/Compare Interrupt Node Pointer Register High	Bit Field	0		INPT13		INPT12		INPERR	
		Type	r		rw		rw		rw	
$A4_H$	**CCU6_ISSL** **Reset: 00_H** Capture/Compare Interrupt Status Set Register Low	Bit Field	ST12PM	ST12OM	SCC62F	SCC62R	SCC61F	SCC61R	SCC60F	SCC60R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISSH** **Reset: 00_H** Capture/Compare Interrupt Status Set Register High	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWHC	STRPF	ST13PM	ST13CM
		Type	w	w	w	w	w	w	w	w
$A6_H$	**CCU6_PSLR** **Reset: 00_H** Passive State Level Register	Bit Field	PSL63	0	PSL					
		Type	rwh	r	rwh					
$A7_H$	**CCU6_MCMCTR** **Reset: 00_H** Multi-Channel Mode Control Register	Bit Field	0		SWSYN		0	SWSEL		
		Type	r		rw		r	rw		
FA_H	**CCU6_TCTR2L** **Reset: 00_H** Timer Control Register 2 Low	Bit Field	0	T13TED	T13TEC				T13SSC	T12SSC
		Type	r	rw	rw				rw	rw

3.7.1 Module Reset Behavior

Table 22 lists the functions of the XC886/888 and the various reset types that affect these functions. The symbol "■" signifies that the particular function is reset to its default state.

Table 22 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core	■	■	■	■	■
Peripherals	■	■	■	■	■
On-Chip Static RAM	Not affected, Reliable	Not affected, Reliable	Not affected, Reliable	Affected, un-reliable	Affected, un-reliable
Oscillator, PLL	■	Not affected	■	■	■
Port Pins	■	■	■	■	■
EVR	The voltage regulator is switched on	Not affected	■	■	■
FLASH	■	■	■	■	■
NMI	Disabled	Disabled	■	■	■

3.7.2 Booting Scheme

When the XC886/888 is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. Table 23 shows the available boot options in the XC886/888.

Table 23 XC886/888 Boot Selection

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	X	User Mode[1]; on-chip OSC/PLL non-bypassed	0000_H
0	0	X	BSL Mode; on-chip OSC/PLL non-bypassed[2]	0000_H
0	1	0	OCDS Mode; on-chip OSC/PLL non-bypassed	0000_H
1	1	0	User (JTAG) Mode[3]; on-chip OSC/PLL non-bypassed (normal)	0000_H

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.

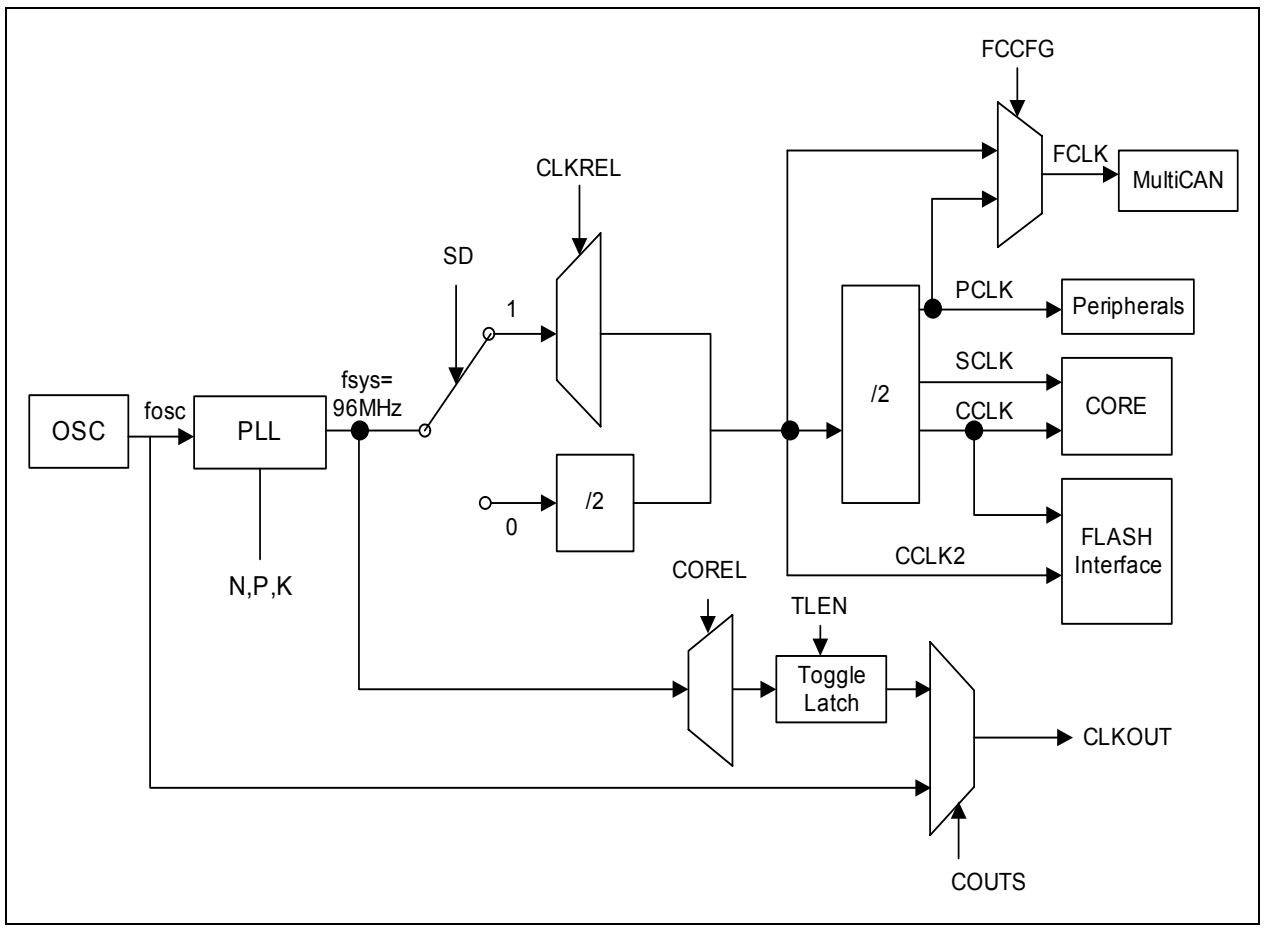


Figure 26 Clock Generation from f_{sys}

3.9 Power Saving Modes

The power saving modes of the XC886/888 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 27**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

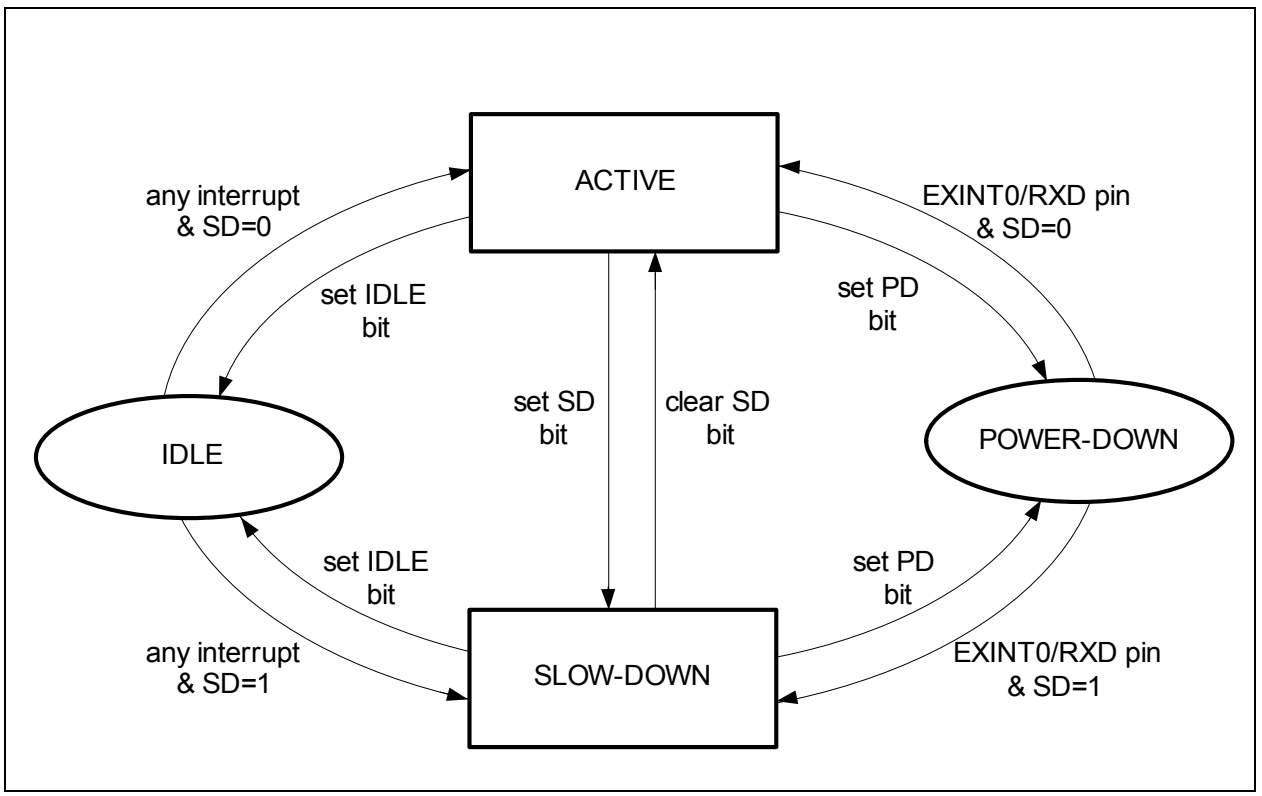


Figure 27 Transition between Power Saving Modes

– Interrupt enabling and corresponding flag

3.13 UART and UART1

The XC886/888 provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

Features

- Full-duplex asynchronous modes
  – 8-bit or 9-bit data frames, LSB first
  – Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in **Table 29**.

Table 29 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32$ or $f_{PCLK}/64$[1)]
Mode 3: 9-bit shift UART	Variable

1) For UART1 module, the baud rate is fixed at $f_{PCLK}/64$.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at $f_{PCLK}/2$. In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either $f_{PCLK}/32$ or $f_{PCLK}/64$. For UART1 module, only $f_{PCLK}/64$ is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and

However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if f_{ADC} becomes too low during slow-down mode.

3.21.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:

- Synchronization phase (t_{SYN})
- Sample phase (t_S)
- Conversion phase
- Write result phase (t_{WR})

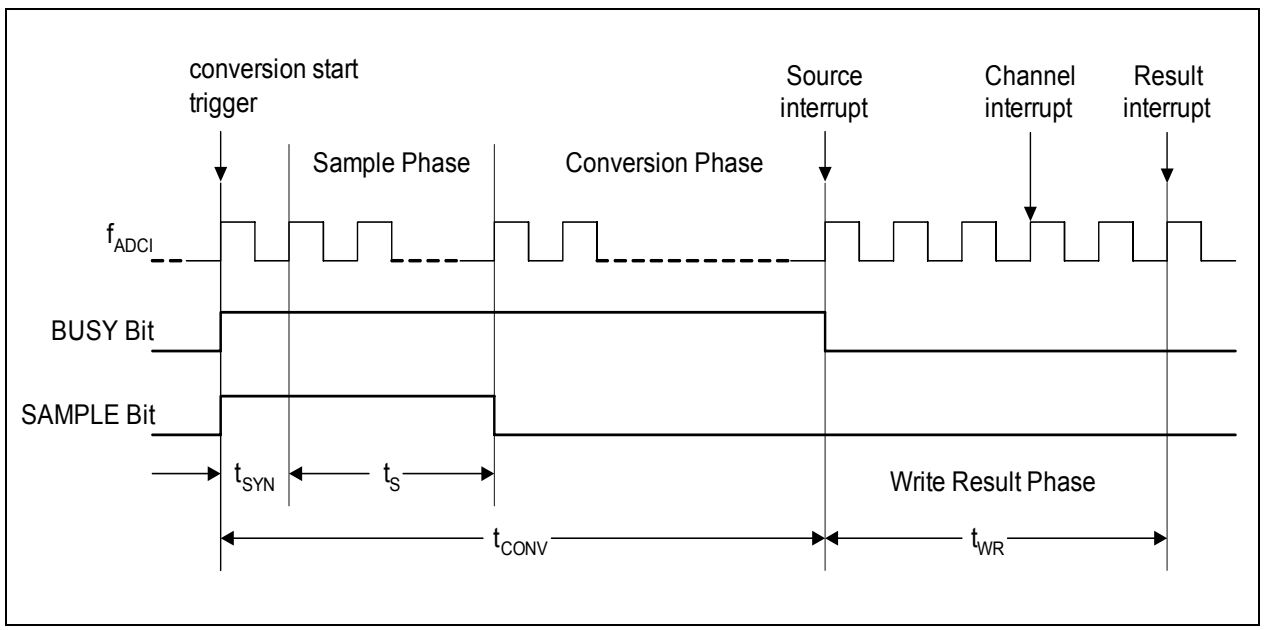


Figure 36 ADC Conversion Timing

3.22 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

Features

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in **Figure 37**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG[1)], which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC886/888 has been started in OCDS mode.

1) The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).
User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

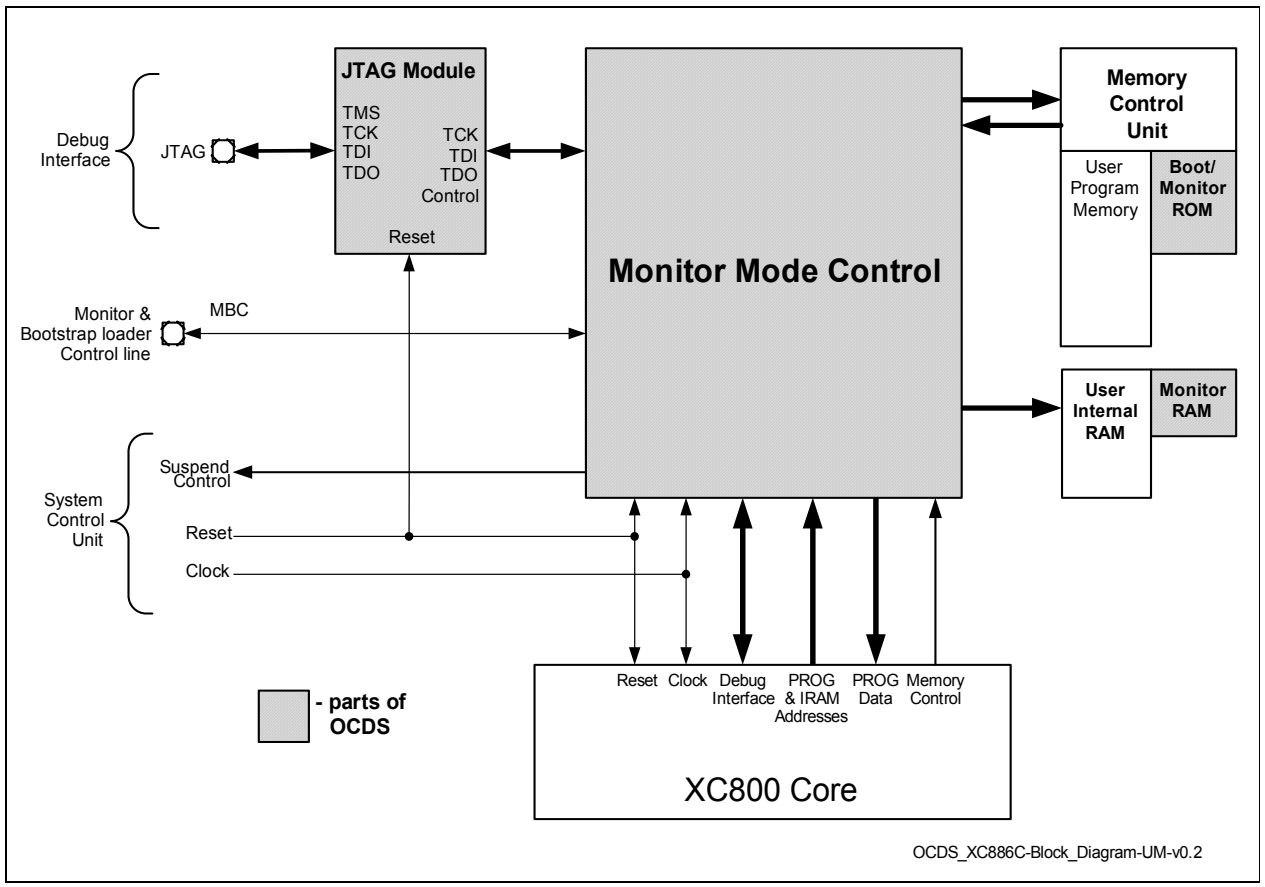


Figure 37 OCDS Block Diagram

3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC886/888 Flash devices are given in **Table 35**.

Table 35 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC886/888*-8FF	$1012\ 0083_H$
	XC886/888*-6FF	$1012\ 5083_H$
ROM	XC886/888*-8RF	$1013\ C083_H$
	XC886/888*-6RF	$1013\ D083_H$

Note: The asterisk (*) above denotes all possible device configurations.

4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC886/888. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 37 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
Digital core supply voltage	V_{DDC}	2.3	2.7	V	
System Clock Frequency[1)]	f_{SYS}	88.8	103.2	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC886/888...
		-40	125	°C	SAK-XC886/888...

1) f_{SYS} is the PLL output clock. During normal operating mode, CPU clock is f_{SYS} / 4. Please refer to **Figure 26** for detailed description.

4.3.2 Output Rise/Fall Times

Table 45 provides the characteristics of the output rise/fall times in the XC886/888.

Table 45 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
V_{DDP} = 5V Range					
Rise/fall times	t_R, t_F	–	10	ns	20 pF.[1)2)3)]
V_{DDP} = 3.3V Range					
Rise/fall times	t_R, t_F	–	10	ns	20 pF.[1)2)4)]

1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.
2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
3) Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.125 ns/pF.
4) Additional rise/fall time valid for C_L = 20pF - 100pF @ 0.225 ns/pF.

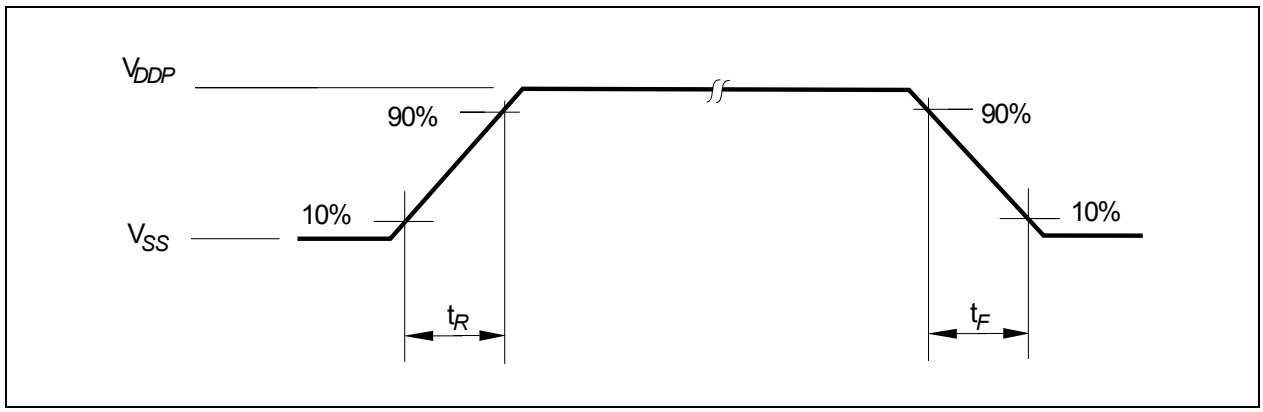


Figure 43 Rise/Fall Times Parameters

4.3.4 On-Chip Oscillator Characteristics

Table 47 provides the characteristics of the on-chip oscillator in the XC886/888.

Table 47 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM}	CC	9.36	9.6	9.84	MHz	under nominal conditions[1]
Long term frequency deviation	Δf_{LT}	CC	-5.0	–	5.0	%	with respect to f_{NOM}, over lifetime and temperature (-10°C to 125°C), for one given device after trimming
			-6.0	–	0	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to -10°C), for one given device after trimming
Short term frequency deviation	Δf_{ST}	CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.

5 Package and Quality Declaration

Chapter 5 provides the information of the XC886/888 package and reliability section.

5.1 Package Parameters

Table 1 provides the thermal characteristics of the package used in XC886 and XC888.

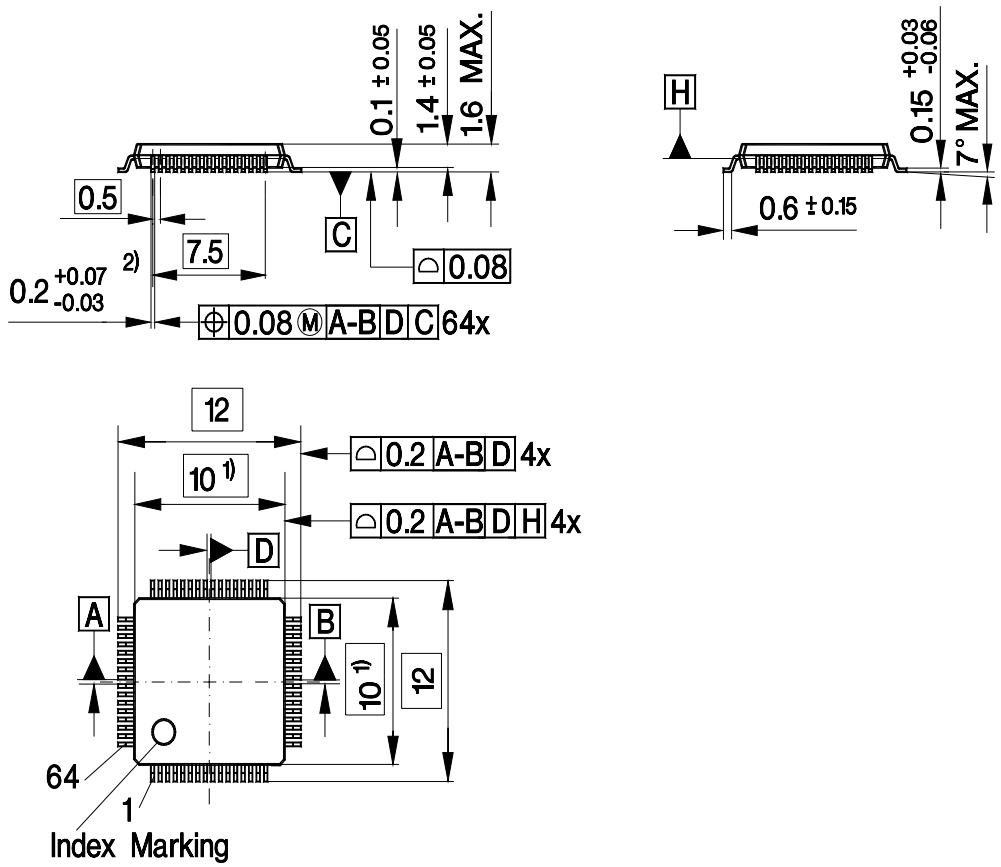
Table 1 Thermal Characteristics of the Packages

Parameter	Symbol		Limit Values		Unit	Notes
			Min.	Max.		
PG-TQFP-48 (XC886)						
Thermal resistance junction case	R_{TJC}	CC	-	13	K/W	1)2)
Thermal resistance junction lead	R_{TJL}	CC	-	32.5	K/W	1)2)
PG-TQFP-64 (XC888)						
Thermal resistance junction case	R_{TJC}	CC	-	12.6	K/W	1)2)
Thermal resistance junction lead	R_{TJL}	CC	-	33.4	K/W	1)2)

1) The thermal resistances between the case and the ambient (R_{TCA}) , the lead and the ambient (R_{TLA}) are to be combined with the thermal resistances between the junction and the case (R_{TJC}), the junction and the lead (R_{TJL}) given above, in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCA}), the lead and the ambient (R_{TLA}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

Figure 49 shows the package outlines of the XC888.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

Figure 49 PG-TQFP-64 Package Outline

5.3 Quality Declaration

Table 2 shows the characteristics of the quality parameters in the XC886/888.

Table 2 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B[1)]
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C[1)]

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.