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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc888clm-6ffa-5v-ac

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General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P0.4	1/64		Hi-Z	MTSR_1 SSC Master Transmit Output/ Slave Receive Input CC62_1 Input/Output of Capture/Compare channel 2 TXD1_0 UART1 Transmit Data Output/Clock Output
P0.5	2/1		Hi-Z	MRST_1 SSC Master Receive Input/Slave Transmit Output EXINT0_0 External Interrupt Input 0 T2EX1_1 Timer 21 External Trigger Input RXD1_0 UART1 Receive Data Input COUT62_1 Output of Capture/Compare channel 2
P0.6	-/2		PU	GPIO
P0.7	47/62		PU	CLKOUT_1 Clock Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.
P1.0	26/34		PU	RXD_0 UART Receive Data Input T2EX Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input
P1.1	27/35		PU	EXINT3 External Interrupt Input 3 T0_1 Timer 0 Input TDO_1 JTAG Serial Data Output TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output
P1.2	28/36		PU	SCK_0 SSC Clock Input/Output
P1.3	29/37		PU	MSTR_0 SSC Master Transmit Output/Slave Receive Input TXDC1_3 MultiCAN Node 1 Transmitter Output
P1.4	30/38		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input
P1.5	31/39		PU	CCPOS0_1 CCU6 Hall Input 0 EXINT5 External Interrupt Input 5 T1_1 Timer 1 Input EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P5		I/O		Port 5 Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1 and JTAG.
P5.0	-/8		PU	EXINT1_1 External Interrupt Input 1
P5.1	-/9		PU	EXINT2_1 External Interrupt Input 2
P5.2	-/12		PU	RXD_2 UART Receive Data Input
P5.3	-/13		PU	TXD_2 UART Transmit Data Output/Clock Output
P5.4	-/14		PU	RXDO_2 UART Transmit Data Output
P5.5	-/15		PU	TDO_2 JTAG Serial Data Output TXD1_2 UART1 Transmit Data Output/ Clock Output
P5.6	-/19		PU	TCK_2 JTAG Clock Input RXDO1_2 UART1 Transmit Data Output
P5.7	-/20		PU	TDI_2 JTAG Serial Data Input RXD1_2 UART1 Receive Data Input

Functional Description
Table 7 CORDIC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
A0 _H	CD_STATC Reset: 00 _H CORDIC Status and Data Control Register	Bit Field	KEEP Z	KEEP Y	KEEP X	DMAP	INT_EN	EOC	ERROR	BSY
		Type	rw	rw	rw	rw	rw	rwh	rh	rh
A1 _H	CD_CON Reset: 00 _H CORDIC Control Register	Bit Field	MPS		X_USIGN	ST_MODE	ROTV EC	MODE		ST
		Type	rw		rw	rw	rw	rw		rwh

3.2.4.4 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 8 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP = 0 or 1											
8F _H	SYSCON0 Reset: 04 _H System Control Register 0	Bit Field	0			IMODE	0	1	0	RMAP	
		Type	r			rw	r	r	r	rw	
RMAP = 0											
BF _H	SCU_PAGE Reset: 00 _H Page Register	Bit Field	OP		STNR		0	PAGE			
		Type	w		w		r	rw			
RMAP = 0, PAGE 0											
B3 _H	MODPISEL Reset: 00 _H Peripheral Input Select Register	Bit Field	0	URRISH	JTAGT DIS	JTAGT CKS	EXINT 2IS	EXINT 1IS	EXINT 0IS	URRIS	
		Type	r	rw	rw	rw	rw	rw	rw	rw	
B4 _H	IRCON0 Reset: 00 _H Interrupt Request Register 0	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0	
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	
B5 _H	IRCON1 Reset: 00 _H Interrupt Request Register 1	Bit Field	0	CANS RC2	CANS RC1	ADCS R1	ADCS R0	RIR	TIR	EIR	
		Type	r	rwh	rwh	rw	rw	rw	rw	rw	
B6 _H	IRCON2 Reset: 00 _H Interrupt Request Register 2	Bit Field	0			CANS RC3	0			CANS RC0	
		Type	r			rw	r			rw	
B7 _H	EXICON0 Reset: F0 _H External Interrupt Control Register 0	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0		
		Type	rw		rw		rw		rw		
BA _H	EXICON1 Reset: 3F _H External Interrupt Control Register 1	Bit Field	0			EXINT6		EXINT5		EXINT4	
		Type	r			rw		rw		rw	
BB _H	NMICON Reset: 00 _H NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	NMI VDD	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT	
		Type	r	rw	rw	rw	rw	rw	rw	rw	

Functional Description
Table 8 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE _H	COCON Reset: 00 _H Clock Output Control Register	Bit Field	0		TLEN	COU S	COREL			
		Type	r		rw	rw	rw			
E9 _H	MISC_CON Reset: 00 _H Miscellaneous Control Register	Bit Field	0							DFL AS HEN
		Type	r							rwh
RMAP = 0, PAGE 3										
B3 _H	XADDRH Reset: F0 _H On-chip XRAM Address Higher Order	Bit Field	ADDRH							
		Type	rw							
B4 _H	IRCON3 Reset: 00 _H Interrupt Request Register 3	Bit Field	0		CANS RC5	CCU6 SR1	0		CANS RC4	CCU6 SR0
		Type	r		rwh	rwh	r		rwh	rwh
B5 _H	IRCON4 Reset: 00 _H Interrupt Request Register 4	Bit Field	0		CANS RC7	CCU6 SR3	0		CANS RC6	CCU6 SR2
		Type	r		rwh	rwh	r		rwh	rwh
B7 _H	MODPISEL1 Reset: 00 _H Peripheral Input Select Register 1	Bit Field	EXINT 6IS	0		UR1RIS		T21EX IS	JTAGT DIS1	JTAGT CKS1
		Type	rw	r		rw		rw	rw	rw
BA _H	MODPISEL2 Reset: 00 _H Peripheral Input Select Register 2	Bit Field	0				T21IS	T2IS	T1IS	T0IS
		Type	r				rw	rw	rw	rw
BB _H	PMCON2 Reset: 00 _H Power Mode Control Register 2	Bit Field	0						UART 1_DIS	T21_D IS
		Type	r						rw	rw
BD _H	MODSUSP Reset: 01 _H Module Suspend Control Register	Bit Field	0			T21SU SP	T2SUS P	T13SU SP	T12SU SP	WDT SUSP
		Type	r			rw	rw	rw	rw	rw

3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
BB _H	WDTCON Reset: 00 _H Watchdog Timer Control Register	Bit Field	0		WINB EN	WDTP R	0	WDTE N	WDTR S	WDTI N
		Type	r		rw	rh	r	rw	rwh	rw
BC _H	WDTREL Reset: 00 _H Watchdog Timer Reload Register	Bit Field	WDTREL							
		Type	rw							
BD _H	WDTWINB Reset: 00 _H Watchdog Window-Boundary Count Register	Bit Field	WDTWINB							
		Type	rw							

Functional Description
Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CC _H	ADC_CHINSR Reset: 00 _H Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Type	w	w	w	w	w	w	w	w
CD _H	ADC_CHINPR Reset: 00 _H Channel Interrupt Node Pointer Register	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
CE _H	ADC_EVINFR Reset: 00 _H Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	0		EVINF 1	EVINF 0
		Type	rh	rh	rh	rh	r		rh	rh
CF _H	ADC_EVINCR Reset: 00 _H Event Interrupt Clear Flag Register	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	0		EVINC 1	EVINC 0
		Type	w	w	w	w	r		w	w
D2 _H	ADC_EVINSR Reset: 00 _H Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	0		EVINS 1	EVINS 0
		Type	w	w	w	w	r		w	w
D3 _H	ADC_EVINPR Reset: 00 _H Event Interrupt Node Pointer Register	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0		EVINP 1	EVINP 0
		Type	rw	rw	rw	rw	r		rw	rw
RMAP = 0, PAGE 6										
CA _H	ADC_CRCR1 Reset: 00 _H Conversion Request Control Register 1	Bit Field	CH7	CH6	CH5	CH4	0			
		Type	rwh	rwh	rwh	rwh	r			
CB _H	ADC_CRPR1 Reset: 00 _H Conversion Request Pending Register 1	Bit Field	CHP7	CHP6	CHP5	CHP4	0			
		Type	rwh	rwh	rwh	rwh	r			
CC _H	ADC_CRMR1 Reset: 00 _H Conversion Request Mode Register 1	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
		Type	r	w	w	rw	rw	rw	r	rw
CD _H	ADC_QMR0 Reset: 00 _H Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Type	w	w	w	w	r	rw	r	rw
CE _H	ADC_QSR0 Reset: 20 _H Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0		FILL	
		Type	r	r	rh	rh	r		rh	
CF _H	ADC_Q0R0 Reset: 00 _H Queue 0 Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QBUR0 Reset: 00 _H Queue Backup Register 0	Bit Field	EXTR	ENSI	RF	V	0	REQCHNR		
		Type	rh	rh	rh	rh	r	rh		
D2 _H	ADC_QINR0 Reset: 00 _H Queue Input Register 0	Bit Field	EXTR	ENSI	RF	0		REQCHNR		
		Type	w	w	w	r		w		

Functional Description
3.2.4.8 Timer 2 Registers

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
C0 _H	T2_T2CON Reset: 00_H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN 2	TR2	C/ $\overline{T2}$	CP/ RL2
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1 _H	T2_T2MOD Reset: 00_H Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H	T2_RC2L Reset: 00_H Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3 _H	T2_RC2H Reset: 00_H Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4 _H	T2_T2L Reset: 00_H Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
C5 _H	T2_T2H Reset: 00_H Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
C0 _H	T21_T2CON Reset: 00_H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN 2	TR2	C/ $\overline{T2}$	CP/ RL2
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1 _H	T21_T2MOD Reset: 00_H Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H	T21_RC2L Reset: 00_H Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3 _H	T21_RC2H Reset: 00_H Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4 _H	T21_T2L Reset: 00_H Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							

Functional Description
Table 17 CAN Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
DB _H	DATA0 Reset: 00_H CAN Data Register 0	Bit Field	CD							
		Type	rwh							
DC _H	DATA1 Reset: 00_H CAN Data Register 1	Bit Field	CD							
		Type	rwh							
DD _H	DATA2 Reset: 00_H CAN Data Register 2	Bit Field	CD							
		Type	rwh							
DE _H	DATA3 Reset: 00_H CAN Data Register 3	Bit Field	CD							
		Type	rwh							

3.2.4.14 OCDS Registers

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 18 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
E9 _H	MMCR2 Reset: 1U_H Monitor Mode Control 2 Register	Bit Field	STMO DE	EXBC	DSUS P	MBCO N	ALTDI	MMEP	MMOD E	JENA
		Type	rw	rw	rw	rwh	rw	rwh	rh	rh
F1 _H	MMCR Reset: 00_H Monitor Mode Control Register	Bit Field	MEXIT _P	MEXIT	0	MSTE P	MRAM S_P	MRAM S	TRF	RRF
		Type	w	rwh	r	rw	w	rwh	rh	rh
F2 _H	MMSR Reset: 00_H Monitor Mode Status Register	Bit Field	MBCA M	MBCIN	EXBF	SWBF	HWB3 F	HWB2 F	HWB1 F	HWB0 F
		Type	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
F3 _H	MMBPCR Reset: 00_H Breakpoints Control Register	Bit Field	SWBC	HWB3C		HWB2C		HWB1 C	HWB0C	
		Type	rw	rw		rw		rw	rw	
F4 _H	MMICR Reset: 00_H Monitor Mode Interrupt Control Register	Bit Field	DVEC T	DRET R	COMR ST	MSTS EL	MMUI E_P	MMUI E	RRIE_ P	RRIE
		Type	rwh	rwh	rwh	rh	w	rw	w	rw
F5 _H	MMDR Reset: 00_H Monitor Mode Data Transfer Register Receive	Bit Field	MMRR							
		Type	rh							
F6 _H	HWBPSR Reset: 00_H Hardware Breakpoints Select Register	Bit Field	0			BPSEL _P	BPSEL			
		Type	r			w	rw			
F7 _H	HWBPDR Reset: 00_H Hardware Breakpoints Data Register	Bit Field	HWBPxx							
		Type	rw							
EB _H	MMWR1 Reset: 00_H Monitor Work Register 1	Bit Field	MMWR1							
		Type	rw							

3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The sectorization of the Flash memory allows each sector to be erased independently.

Features

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width¹⁾ of 32-byte for D-Flash and 64-byte for P-Flash
- 1-sector minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all zeros)
- Operating supply voltage: $2.5\text{ V} \pm 7.5\%$
- Read access time: $3 \times t_{\text{CCLK}} = 125\text{ ns}^2)$
- Program time: $248256 / f_{\text{SYS}} = 2.6\text{ ms}^3)$
- Erase time: $9807360 / f_{\text{SYS}} = 102\text{ ms}^3)$

1) P-Flash: 64-byte wordline can only be programmed once, i.e., one gate disturb allowed.
D-Flash: 32-byte wordline can be programmed twice, i.e., two gate disturbs allowed.

2) Values shown here are typical values. $f_{\text{SYS}} = 96\text{ MHz} \pm 7.5\%$ ($f_{\text{CCLK}} = 24\text{ MHz} \pm 7.5\%$) is the maximum frequency range for Flash read access.

3) Values shown here are typical values. $f_{\text{SYS}} = 96\text{ MHz} \pm 7.5\%$ is the only frequency range for Flash programming and erasing. f_{SYSmin} is used for obtaining the worst case timing.

Functional Description
Table 20 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC886/888	Enable Bit	SFR
XINTR6	0033 _H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	003B _H	SSC	ESSC	
XINTR8	0043 _H	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	004B _H	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		MultiCAN Node 3		
XINTR10	0053 _H	CCU6 INP0	ECCIP0	
		MultiCAN Node 4		
XINTR11	005B _H	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063 _H	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	006B _H	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		

3.7 Reset Control

The XC886/888 has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC886/888 is first powered up, the status of certain pins (see [Table 23](#)) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

In order to power up the system properly, the external reset pin $\overline{\text{RESET}}$ must be asserted until V_{DDC} reaches $0.9 \cdot V_{\text{DDC}}$. The delay of external reset can be realized by an external capacitor at $\overline{\text{RESET}}$ pin. This capacitor value must be selected so that V_{RESET} reaches 0.4 V, but not before V_{DDC} reaches $0.9 \cdot V_{\text{DDC}}$.

A typical application example is shown in [Figure 22](#). The V_{DDP} capacitor value is 100 nF while the V_{DDC} capacitor value is 220 nF. The capacitor connected to $\overline{\text{RESET}}$ pin is 100 nF.

Typically, the time taken for V_{DDC} to reach $0.9 \cdot V_{\text{DDC}}$ is less than 50 μs once V_{DDP} reaches 2.3V. Hence, based on the condition that 10% to 90% V_{DDP} (slew rate) is less than 500 μs , the $\overline{\text{RESET}}$ pin should be held low for 500 μs typically. See [Figure 23](#).

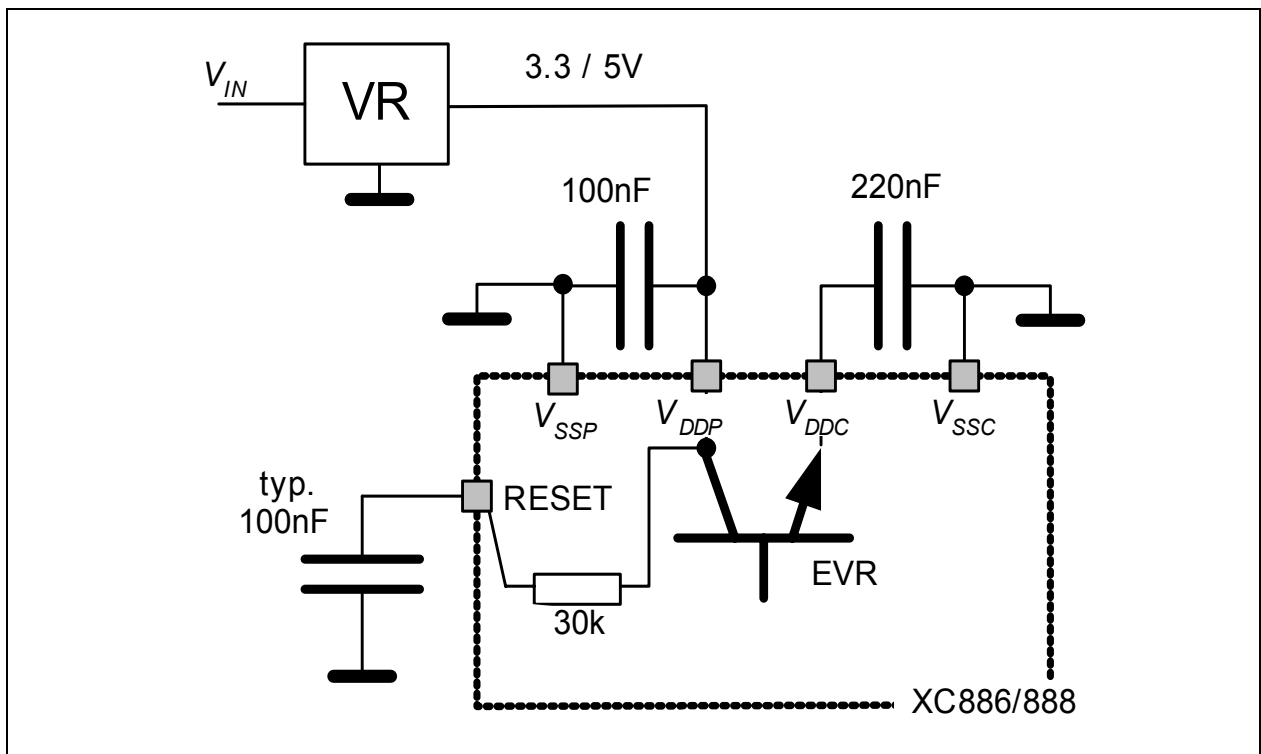


Figure 22 Reset Circuitry

Functional Description

- 1) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
- 2) OSC is bypassed in MultiCAN BSL mode
- 3) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC886/888. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC886/888, the oscillator can be from either of these two sources: the on-chip oscillator (9.6 MHz) or the external oscillator (4 MHz to 12 MHz). The term “oscillator” is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default. The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys} . During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.

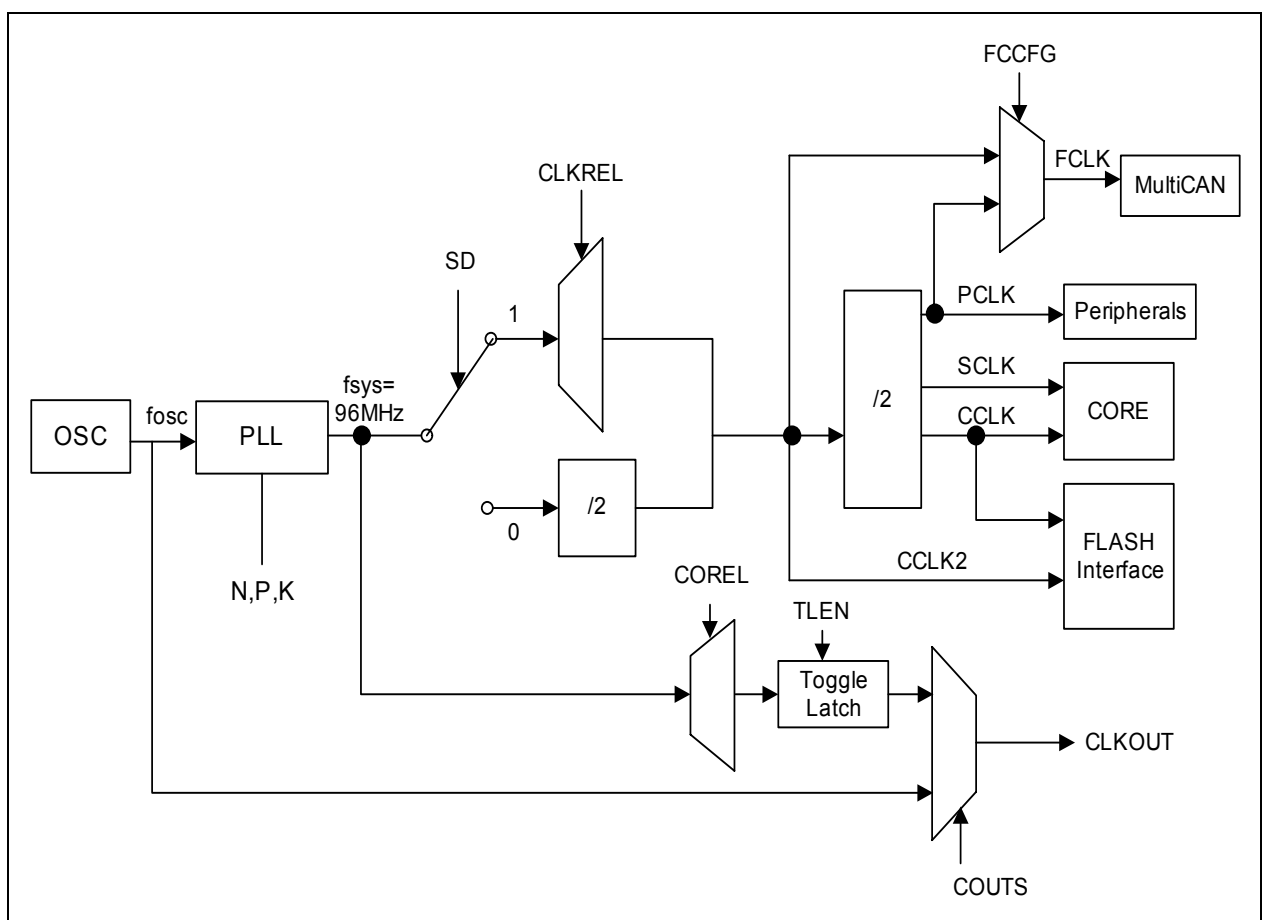


Figure 26 Clock Generation from f_{sys}

Functional Description

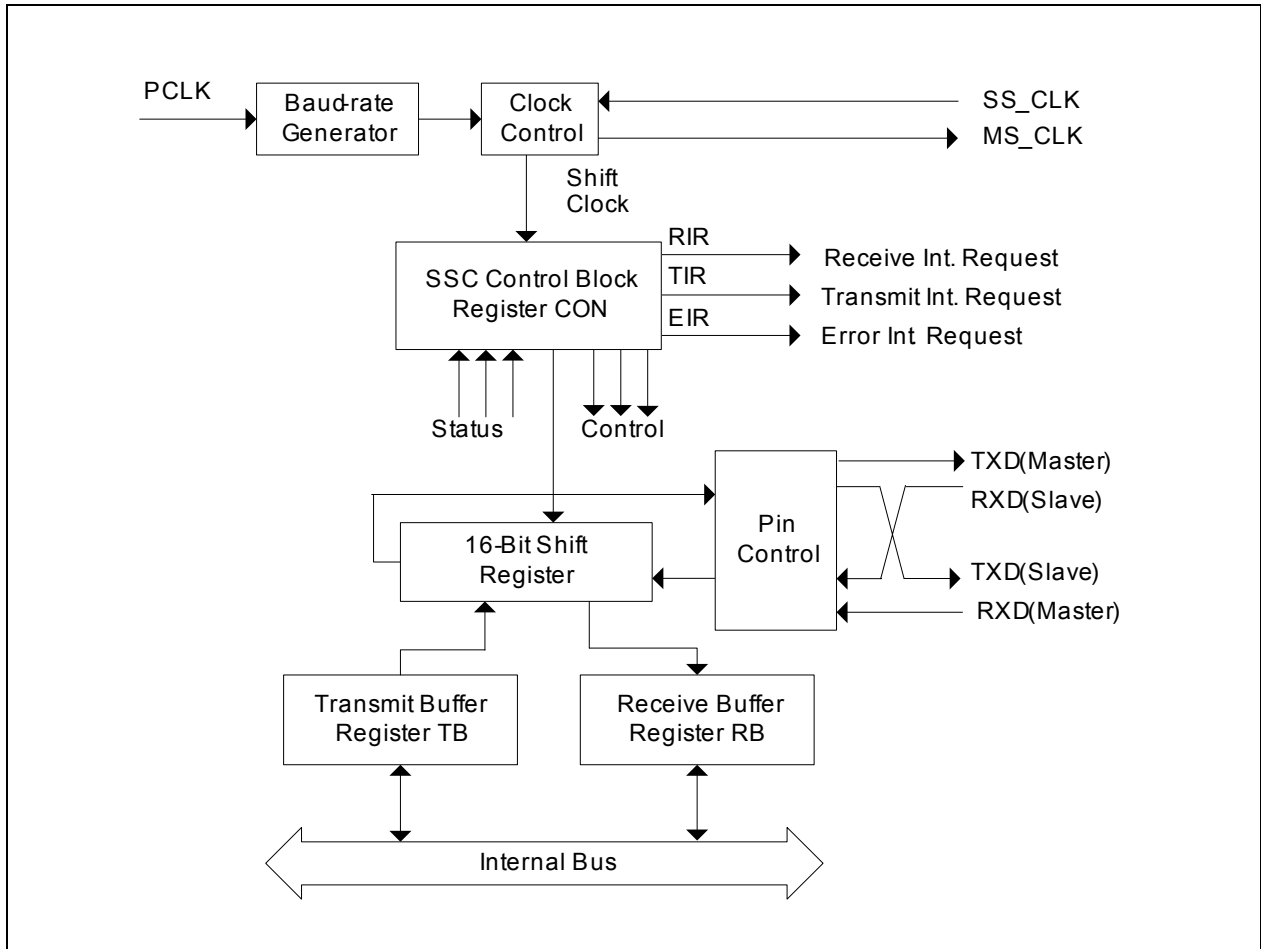


Figure 32 SSC Block Diagram

3.19 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Timer T12 Features

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Generation of center-aligned and edge-aligned PWM
- Supports single-shot mode
- Supports many interrupt request sources
- Hysteresis-like control mode

Timer T13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Supports single-shot mode

Additional Features

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The block diagram of the CCU6 module is shown in [Figure 33](#).

Electrical Parameters
Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage at XTAL1	V_{IHx}	SR	$0.7 \times V_{DDC}$	$V_{DDC} + 0.5$	V	
Pull-up current	I_{PU}	SR	–	-5	μA	$V_{IHP,min}$
			-50	–	μA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	5	μA	$V_{ILP,max}$
			50	–	μA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	μA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125^\circ C^2)$
Input current at XTAL1	I_{ILx}	CC	- 10	10	μA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma I_{OV} $	SR	–	25	mA	³⁾
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	⁴⁾
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M	SR SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma I_M $	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	³⁾
Maximum current out of V_{SS}	I_{MVSS}	SR	–	120	mA	³⁾

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INj}) will flow if an overload current flows through an adjacent pin. TMS pin and RESET pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

4.2.2 Supply Threshold Characteristics

Table 39 provides the characteristics of the supply threshold in the XC886/888.

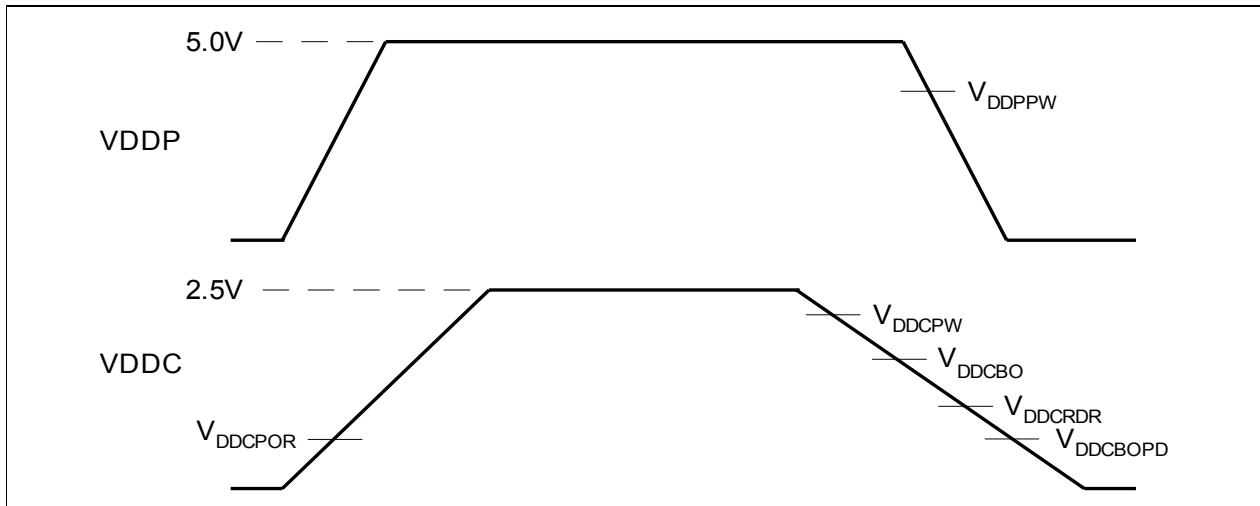


Figure 38 Supply Threshold Parameters

Table 39 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} prewarning voltage ¹⁾	V_{DDCPW}	CC	2.2	2.3	2.4	V
V_{DDC} brownout voltage in active mode ¹⁾	V_{DDCBO}	CC	2.0	2.1	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	0.9	1.0	1.1	V
V_{DDC} brownout voltage in power-down mode ²⁾	$V_{DDCBOPD}$	CC	1.3	1.5	1.7	V
V_{DDP} prewarning voltage ³⁾	V_{DDPPW}	CC	3.4	4.0	4.6	V
Power-on reset voltage ²⁾⁴⁾	V_{DDCPOR}	CC	1.3	1.5	1.7	V

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V.
Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 μ s typically after the VDDC reaches the power-on reset voltage.

4.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in [Figure 40](#), [Figure 41](#) and [Figure 42](#).

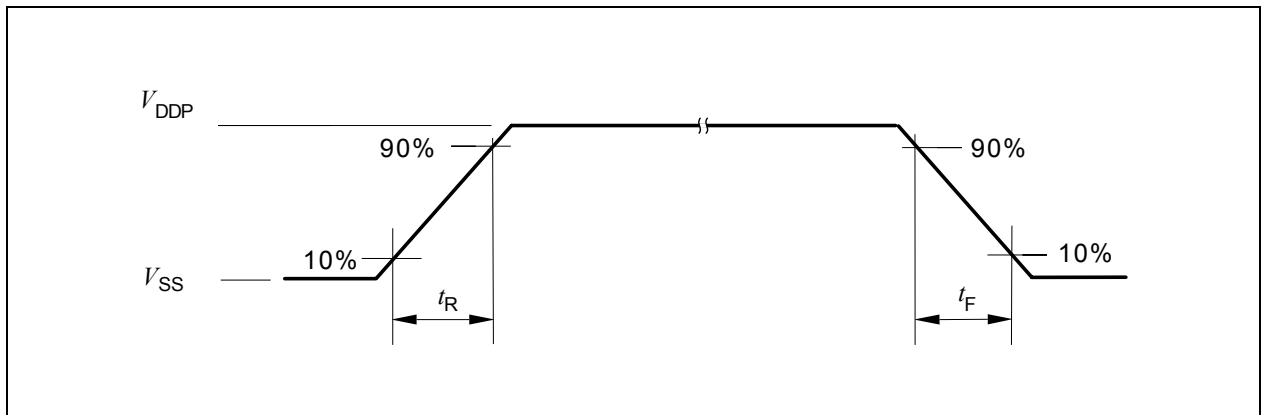


Figure 40 Rise/Fall Time Parameters

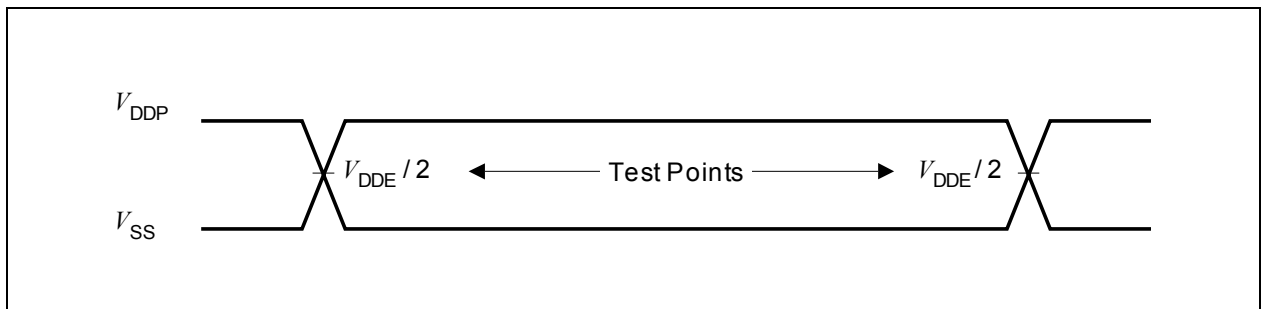


Figure 41 Testing Waveform, Output Delay

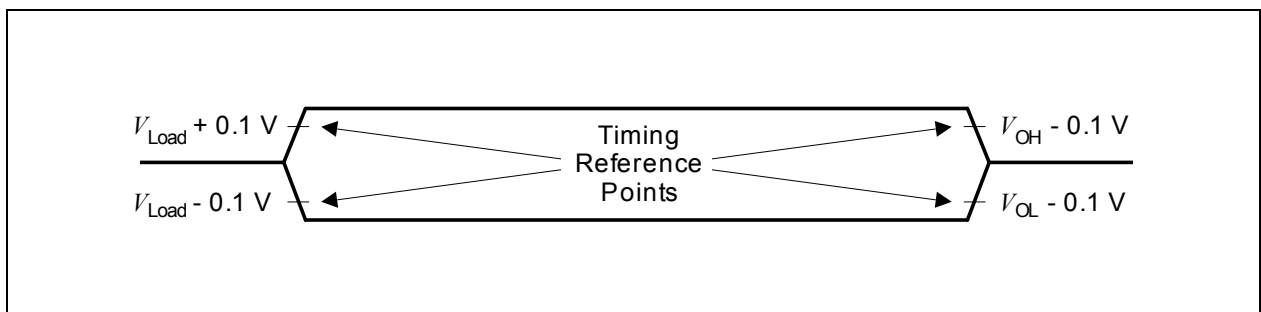


Figure 42 Testing Waveform, Output High Impedance

5.2 Package Outline

Figure 48 shows the package outlines of the XC886.

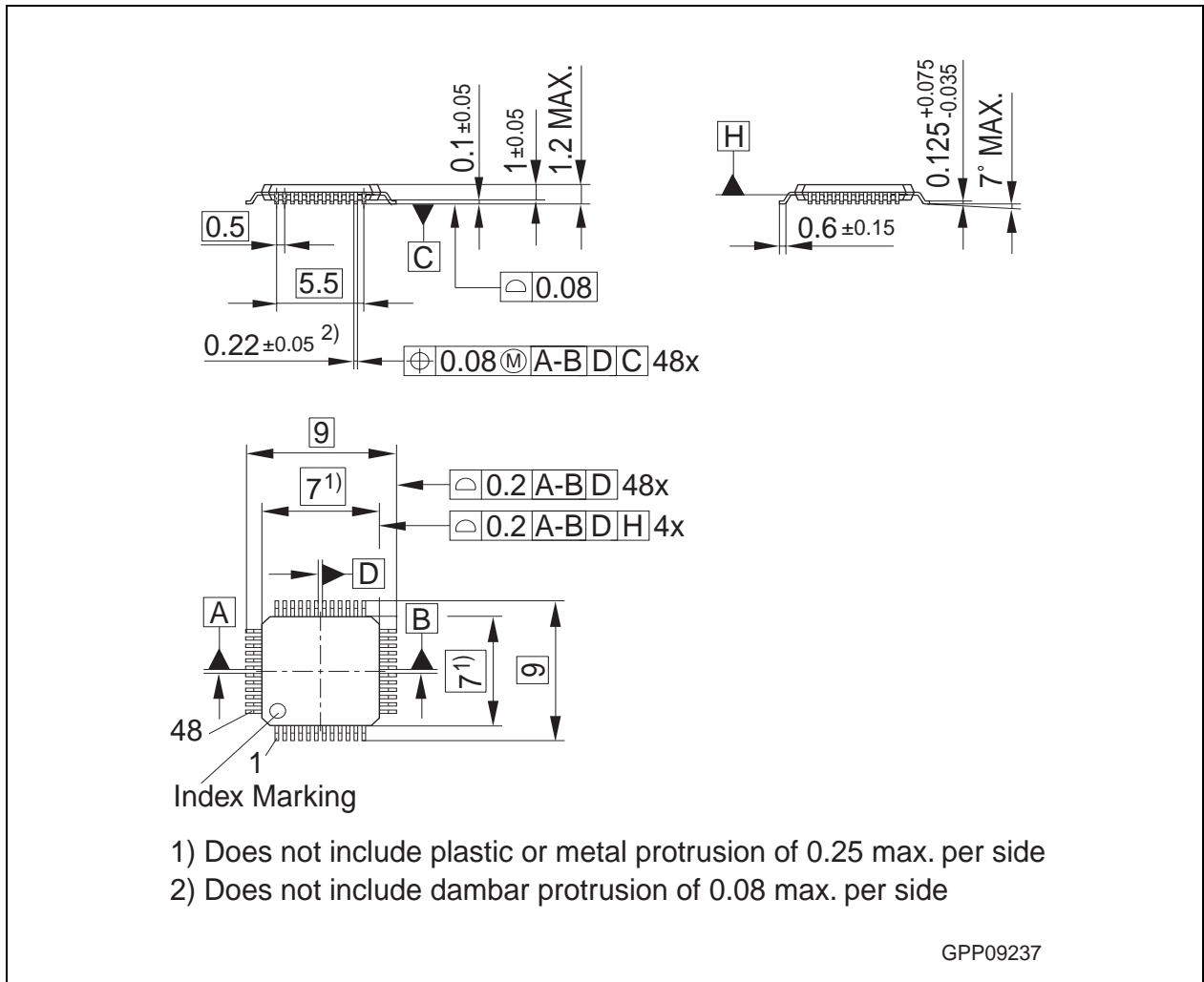


Figure 48 PG-TQFP-48 Package Outline