Infineon Technologies - SAF-XC888LM-8FFA 5V AC Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xc888lm-8ffa-5v-ac

2.2 Logic Symbol

The logic symbols of the XC886/888 are shown in **Figure 3**.

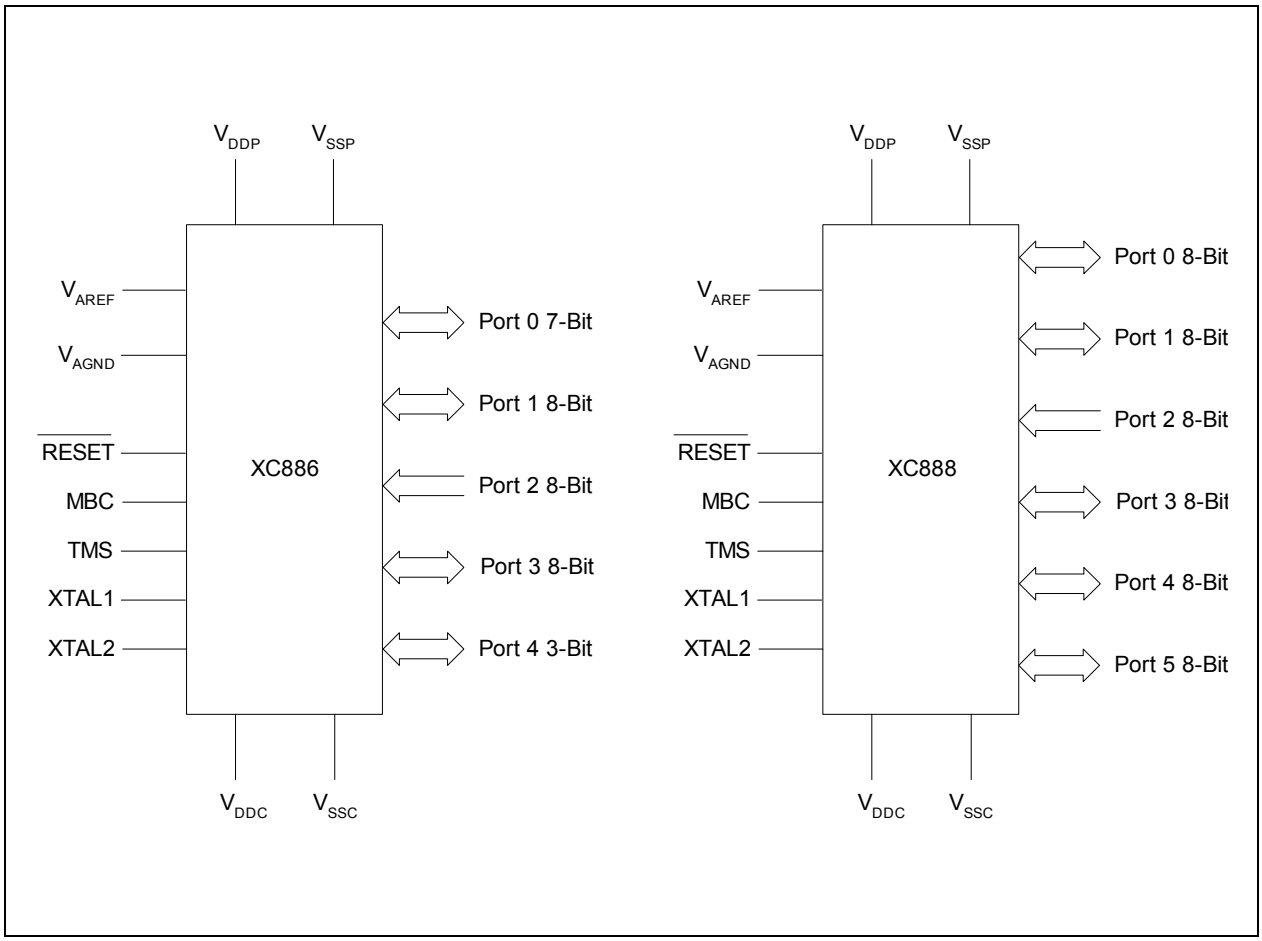


Figure 3 XC886/888 Logic Symbol

2.4 Pin Definitions and Functions

The functions and default states of the XC886/888 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P0		I/O		**Port 0** Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, Timer 2, Timer 21, MultiCAN and SSC.
P0.0	11/17		Hi-Z	TCK_0 JTAG Clock Input T12HR_1 CCU6 Timer 12 Hardware Run Input CC61_1 Input/Output of Capture/Compare channel 1 CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	13/21		Hi-Z	TDI_0 JTAG Serial Data Input T13HR_1 CCU6 Timer 13 Hardware Run Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input COUT61_1 Output of Capture/Compare channel 1 EXF2_1 Timer 2 External Flag Output
P0.2	12/18		PU	$\overline{\text{CTRAP}}$_2 CCU6 Trap Input TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output
P0.3	48/63		Hi-Z	SCK_1 SSC Clock Input/Output COUT63_1 Output of Capture/Compare channel 3 RXDO1_0 UART1 Transmit Data Output

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P1.6	8/10		PU	CCPOS1_1 CCU6 Hall Input 1 T12HR_0 CCU6 Timer 12 Hardware Run Input EXINT6_0 External Interrupt Input 6 RXDC0_2 MultiCAN Node 0 Receiver Input T21_1 Timer 21 Input
P1.7	9/11		PU	CCPOS2_1 CCU6 Hall Input 2 T13HR_0 CCU6 Timer 13 Hardware Run Input T2_1 Timer 2 Input TXDC0_2 MultiCAN Node 0 Transmitter Output P1.5 and P1.6 can be used as a software chip select output for the SSC.

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P3		I/O		**Port 3** Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 Input/Output of Capture/Compare channel 2 RXDC0_1 MultiCAN Node 0 Receiver Input T2EX1_0 Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 Output of Capture/Compare channel 2 EXF21_0 Timer 21 External Flag Output TXDC0_1 MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	$\overline{\text{CTRAP\_0}}$ CCU6 Trap Input

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
V_{DDP}	7, 17, 43/ 7, 25, 55	–	–	**I/O Port Supply (3.3 or 5.0 V)** Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	18, 42/26, 54	–	–	**I/O Port Ground** All pins must be connected.
V_{DDC}	6/6	–	–	**Core Supply Monitor (2.5 V)**
V_{SSC}	5/5	–	–	**Core Supply Ground**
V_{AREF}	24/32	–	–	**ADC Reference Voltage**
V_{AGND}	23/31	–	–	**ADC Reference Ground**
XTAL1	4/4	I	Hi-Z	**External Oscillator Input (backup for on-chip OSC, normally NC)**
XTAL2	3/3	O	Hi-Z	**External Oscillator Output (backup for on-chip OSC, normally NC)**
TMS	10/16	I	PD	**Test Mode Select**
RESET	41/53	I	PU	**Reset Input**
MBC[1)]	44/58	I	PU	**Monitor & BootStrap Loader Control**
NC	–/56, 57	–	–	**No Connection**

1) An external pull-up device in the range of 4.7 kΩ to 100 kΩ. is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

code or data. Therefore, even though the ROM device contains either a 24-Kbyte or 32-Kbyte ROM, the maximum size of code that can be placed in the ROM is the given size less four bytes.

3.2.1 Memory Protection Strategy

The XC886/888 memory protection strategy includes:

- Read-out protection: The user is able to protect the contents in the Flash (for Flash devices) and ROM (for ROM devices) memory from being read
  - Flash protection is enabled by programming a valid password (8-bit non-zero value) via BSL mode 6.
  - ROM protection is fixed with the ROM mask and is always enabled.
- Flash program and erase protection: This feature is available only for Flash devices.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

Table 4 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 4 of password = 0	Bit 4 of password = 1 MSB of password = 0	Bit 4 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible

- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

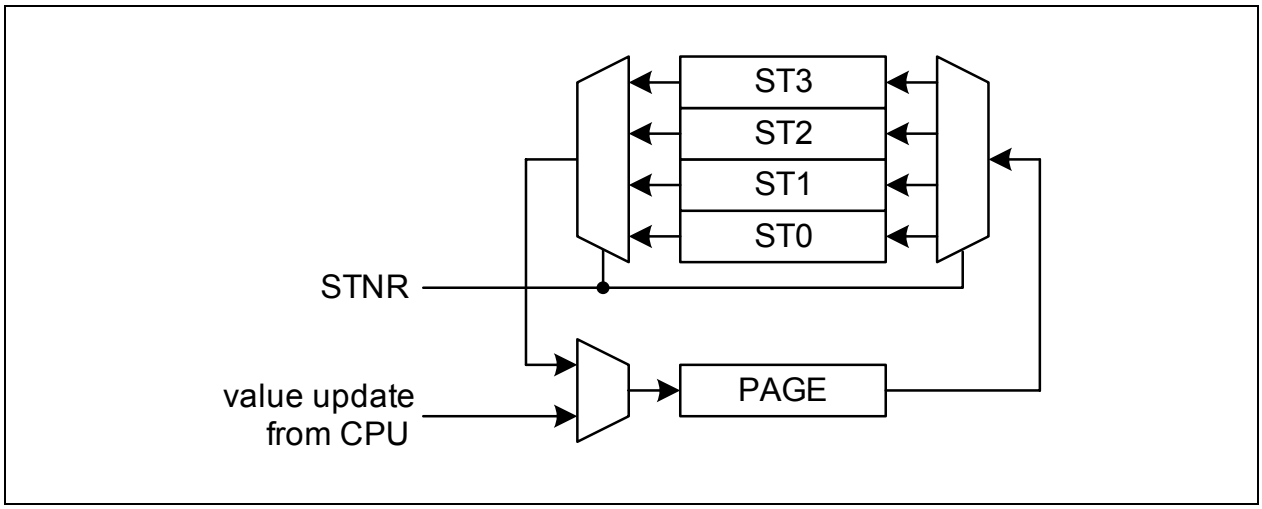


Figure 10 Storage Elements for Paging

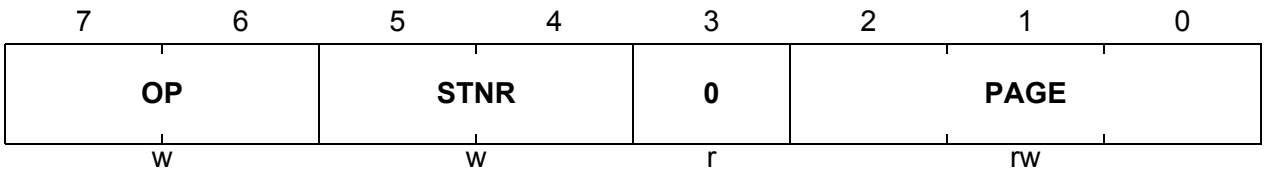
With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC886/888 supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

The page register has the following definition:

MOD_PAGE
Page Register for module MOD **Reset Value: 00_H**



Field	Bits	Type	Description
PAGE	[2:0]	rw	**Page Bits** When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	**Storage Number** This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10_B, the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11_B, the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. 00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.

3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 16 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A9_H$	**SSC_PISEL** **Reset: 00_H** Port Input Select Register	Bit Field	0					CIS	SIS	MIS
		Type	r					rw	rw	rw
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Programming Mode	Bit Field	LB	PO	PH	HB	BM			
		Type	rw	rw	rw	rw	rw			
AA_H	**SSC_CONL** **Reset: 00_H** Control Register Low Operating Mode	Bit Field	0				BC			
		Type	r				rh			
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Programming Mode	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
		Type	rw	rw	r	rw	rw	rw	rw	rw
AB_H	**SSC_CONH** **Reset: 00_H** Control Register High Operating Mode	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
		Type	rw	rw	r	rh	rwh	rwh	rwh	rwh
AC_H	**SSC_TBL** **Reset: 00_H** Transmitter Buffer Register Low	Bit Field	TB_VALUE							
		Type	rw							
AD_H	**SSC_RBL** **Reset: 00_H** Receiver Buffer Register Low	Bit Field	RB_VALUE							
		Type	rh							
AE_H	**SSC_BRL** **Reset: 00_H** Baud Rate Timer Reload Register Low	Bit Field	BR_VALUE							
		Type	rw							
AF_H	**SSC_BRH** **Reset: 00_H** Baud Rate Timer Reload Register High	Bit Field	BR_VALUE							
		Type	rw							

3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 17 CAN Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$D8_H$	**ADCON** **Reset: 00_H** CAN Address/Data Control Register	Bit Field	V3	V2	V1	V0	AUAD		BSY	RWEN
		Type	rw	rw	rw	rw	rw		rh	rw
$D9_H$	**ADL** **Reset: 00_H** CAN Address Register Low	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
DA_H	**ADH** **Reset: 00_H** CAN Address Register High	Bit Field	0				CA13	CA12	CA11	CA10
		Type	r				rwh	rwh	rwh	rwh

3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC886/888 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to **Figure 17** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

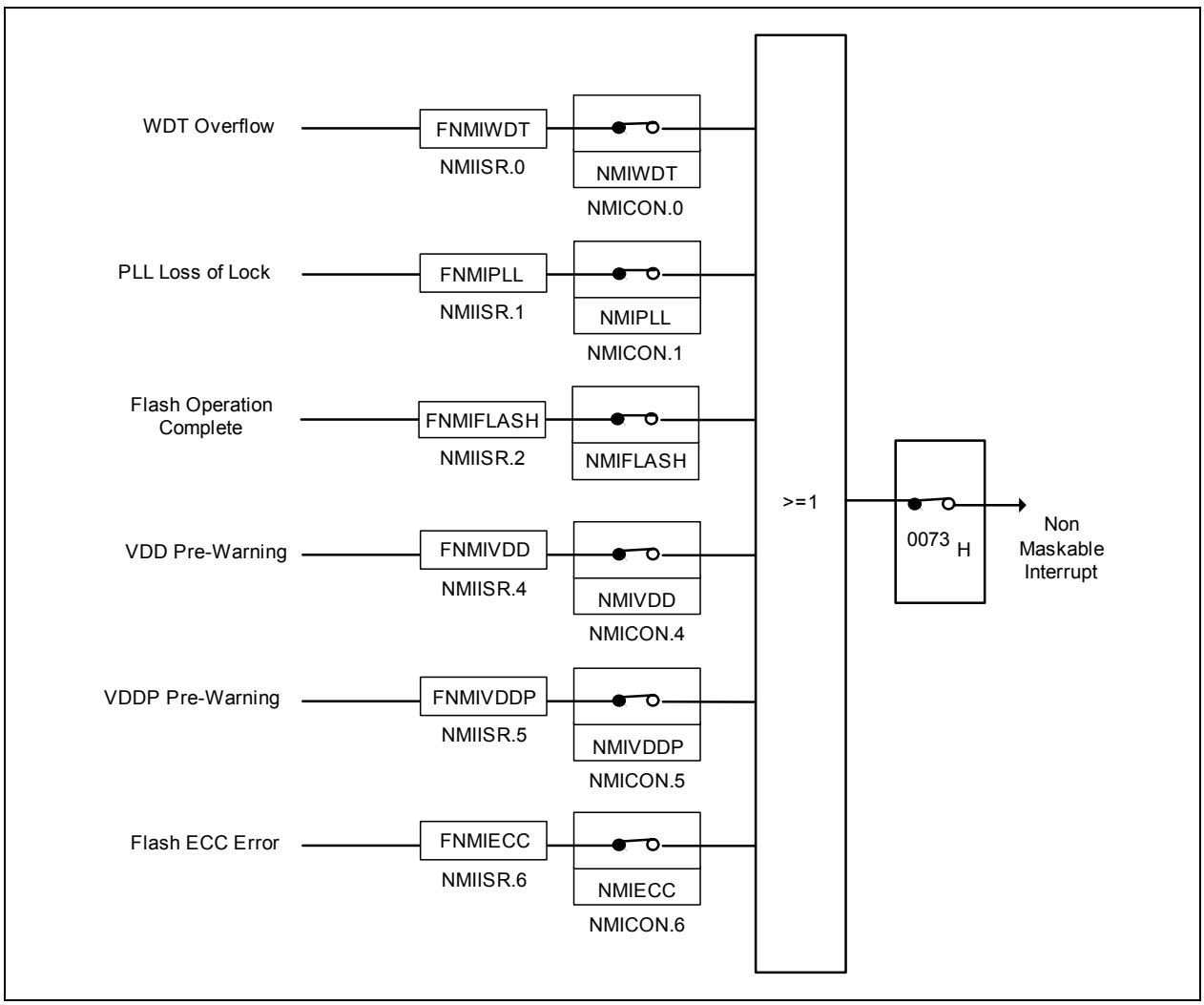


Figure 13 Non-Maskable Interrupt Request Sources

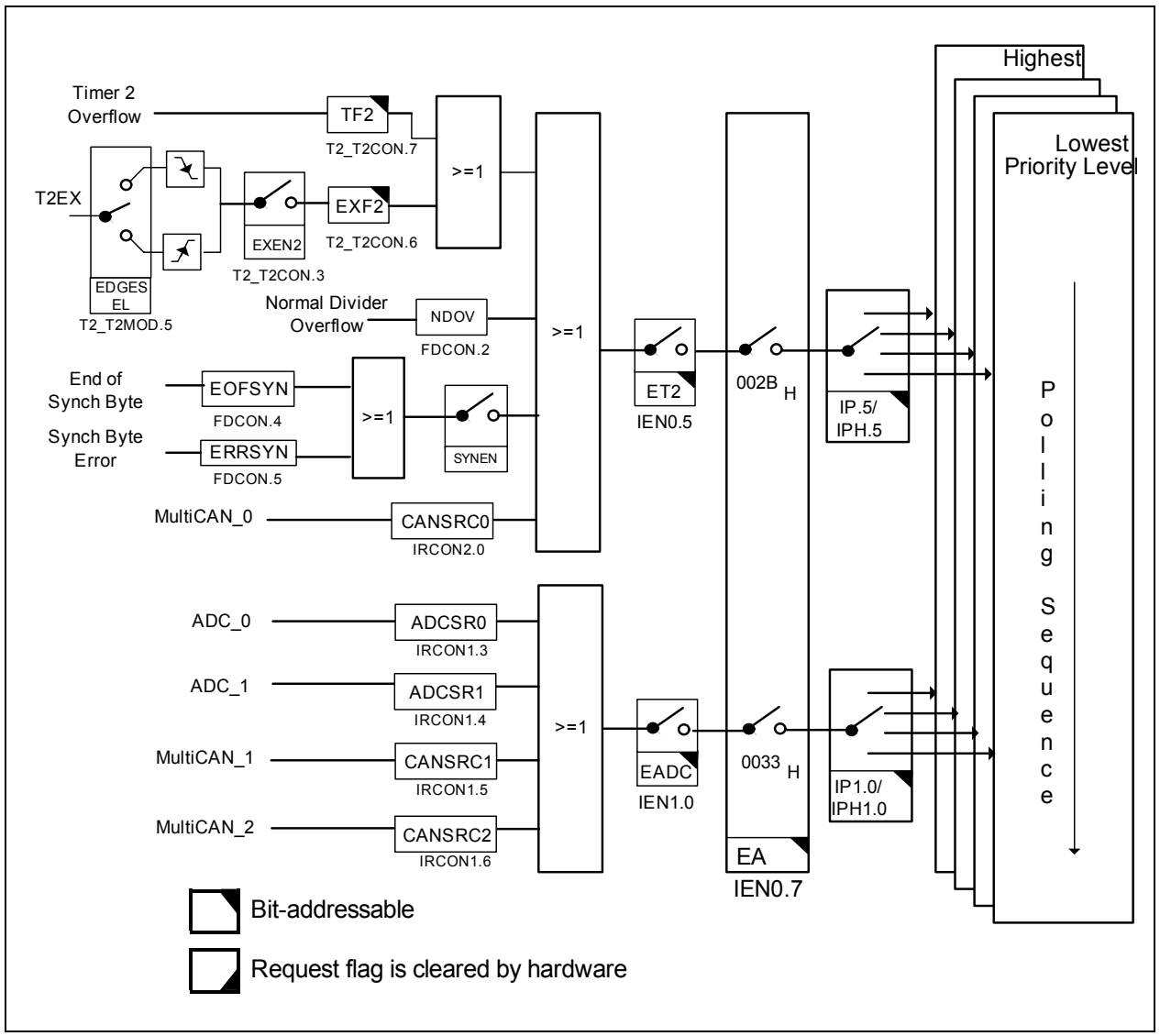


Figure 15 Interrupt Request Sources (Part 2)

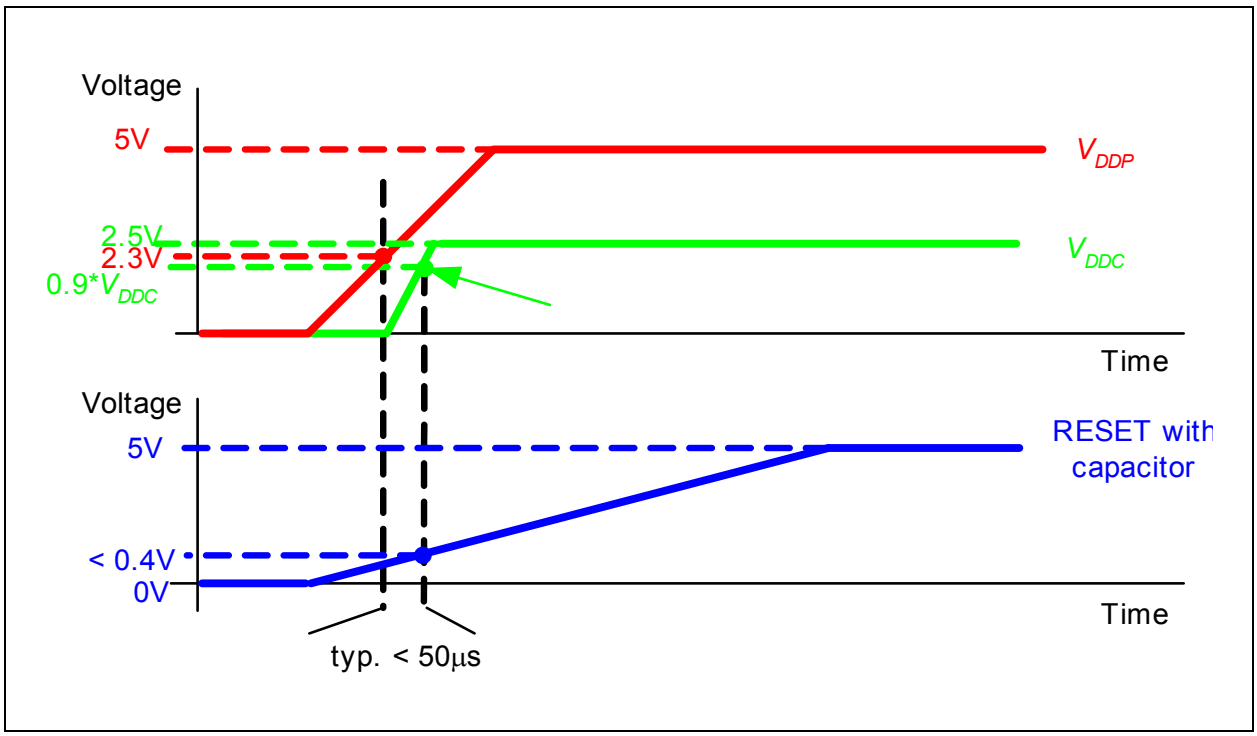


Figure 23 V_{DDP}, V_{DDC} and V_{RESET} during Power-on Reset

The second type of reset in XC886/888 is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin $\overline{\text{RESET}}$ is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.

3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, f_{sys}. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.

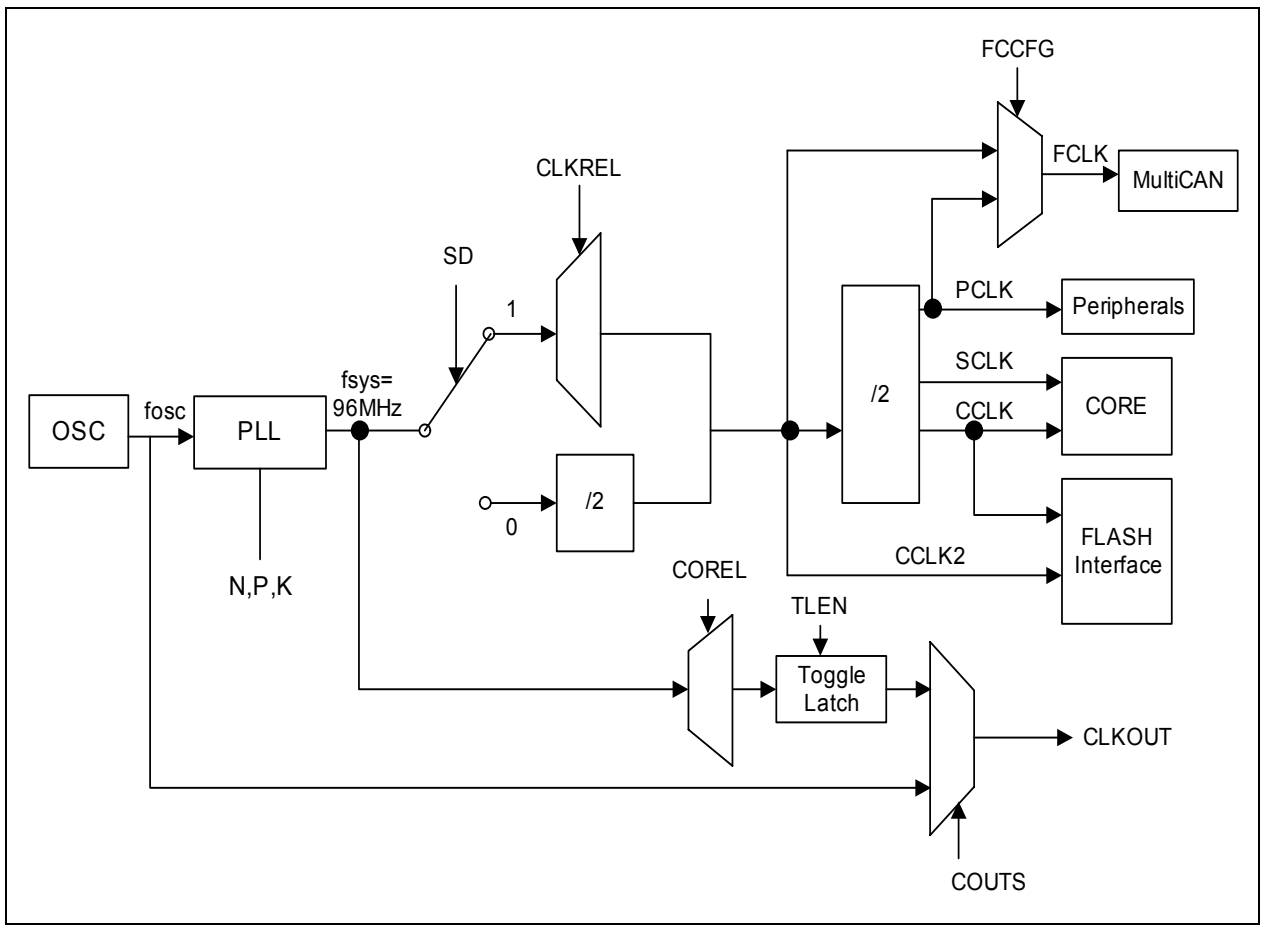


Figure 26 Clock Generation from f_{sys}

For power saving purposes, the clocks may be disabled or slowed down according to Table 26.

Table 26 System frequency (f_{sys} = 96 MHz)

Power Saving Mode	Action
Idle	Clock to the CPU is disabled.
Slow-down	Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL.
Power-down	Oscillator and PLL are switched off.

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC886/888 can be subjected to without permanent damage.

Table 4-1 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	under bias1)
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	1)
Voltage on any pin with respect to V_{SS}	V_{IN}	-0.5	V_{DDP} + 0.5 or max. 6	V	whichever is lower1)
Input current on any pin during overload condition	I_{IN}	-10	10	mA	1)
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	1)

1) Not subjected to production test, verified by design/characterization.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	–	-5	µA	$V_{IHP,min}$
			-50	–	µA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	5	µA	$V_{ILP,max}$
			50	–	µA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$ [2]
Input current at XTAL1	I_{ILX}	CC	- 10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	[3]
Maximum current out of V_{SS}	I_{MVSS}	SR	–	120	mA	[3]

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins (V_{SS}) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 40 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	V_{AREF}	SR	V_{AGND} + 1	V_{DDP}	V_{DDP} + 0.05	V	[1]
Analog reference ground	V_{AGND}	SR	V_{SS} - 0.05	V_{SS}	V_{AREF} - 1	V	[1]
Analog input voltage range	V_{AIN}	SR	V_{AGND}	–	V_{AREF}	V	
ADC clocks	f_{ADC}		–	24	25.8	MHz	module clock[1]
	f_{ADCI}		–	–	10	MHz	internal analog clock[1] See **Figure 35**
Sample time	t_S	CC	(2 + INPCR0.STC) × t_{ADCI}			µs	[1]
Conversion time	t_C	CC	See **Section 4.2.3.1**			µs	[1]
Total unadjusted error	|TUE|	CC	–	–	1	LSB	8-bit conversion[2]
			–	–	2	LSB	10-bit conversion[2]
Differential Nonlinearity	$\|EA_{DNL}\|$	CC	–	1	–	LSB	10-bit conversion[1]
Integral Nonlinearity	$\|EA_{INL}\|$	CC	–	1	–	LSB	10-bit conversion[1]
Offset	$\|EA_{OFF}\|$	CC	–	1	–	LSB	10-bit conversion[1]
Gain	$\|EA_{GAIN}\|$	CC	–	1	–	LSB	10-bit conversion[1]
Overload current coupling factor for analog inputs	K_{OVA}	CC	–	–	1.0 x 10^{-4}	–	$I_{OV} > 0$[1][3]
			–	–	1.5 x 10^{-3}	–	$I_{OV} < 0$[1][3]

4.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 40**, **Figure 41** and **Figure 42**.

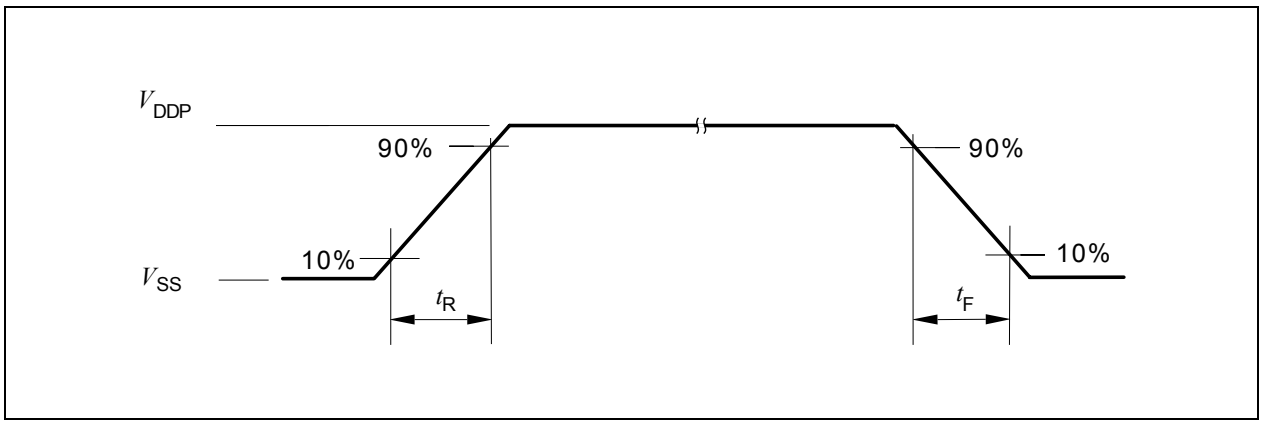


Figure 40 Rise/Fall Time Parameters

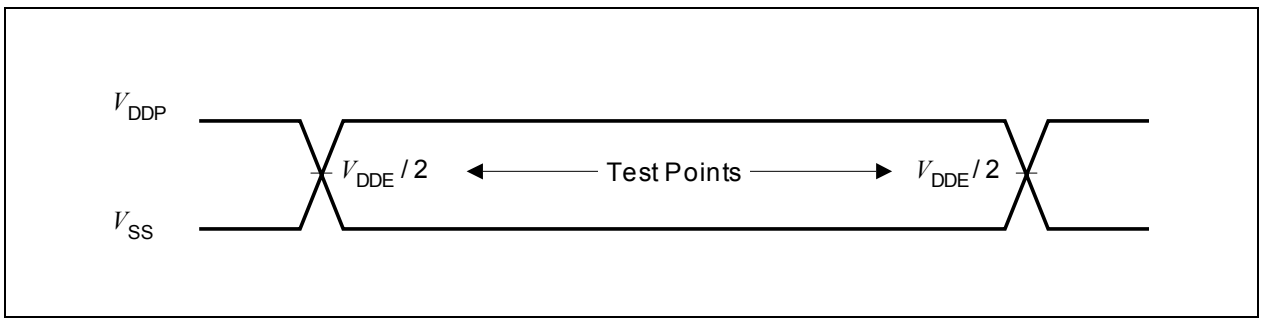


Figure 41 Testing Waveform, Output Delay

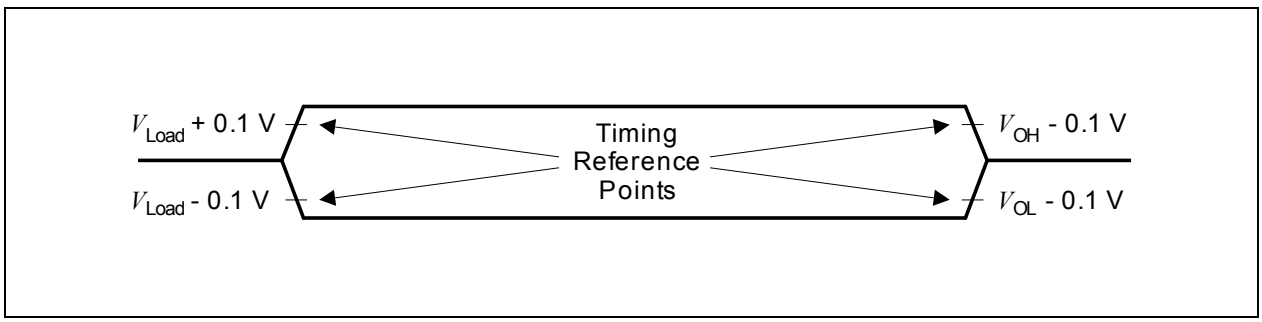


Figure 42 Testing Waveform, Output High Impedance

4.3.4 On-Chip Oscillator Characteristics

Table 47 provides the characteristics of the on-chip oscillator in the XC886/888.

Table 47 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	f_{NOM}	CC	9.36	9.6	9.84	MHz	under nominal conditions[1]
Long term frequency deviation	Δf_{LT}	CC	-5.0	–	5.0	%	with respect to f_{NOM}, over lifetime and temperature (-10°C to 125°C), for one given device after trimming
			-6.0	–	0	%	with respect to f_{NOM}, over lifetime and temperature (-40°C to -10°C), for one given device after trimming
Short term frequency deviation	Δf_{ST}	CC	-1.0	–	1.0	%	within one LIN message (<10 ms .... 100 ms)

1) Nominal condition: V_{DDC} = 2.5 V, T_A = + 25°C.