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Details

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886-6ffi-5v-ac

8-Bit

XC886/888CLM

8-Bit Single Chip Microcontroller

Data Sheet

V1.2 2009-07

Microcontrollers

XC886/888 Data Sheet

Revision History: V1.2 2009-07

Previous Versions: V1.0, V1.1

Page	Subjects (major changes since last revision)
Changes from V1.1 2009-01 to V1.2 2009-07	
89	Note on LIN baud rate detection is added.
92	RXD slave line in SSC block diagram is updated.
108	Electrical parameters are now valid for all variants, previous note on exclusion of ROM variants is removed.
116	Symbol for ADC error parameters are updated.
120	Power supply current parameters for ROM variants are updated.
128	Test condition for the on-chip oscillator short term deviation is updated.

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2.2 Logic Symbol

The logic symbols of the XC886/888 are shown in **Figure 3**.

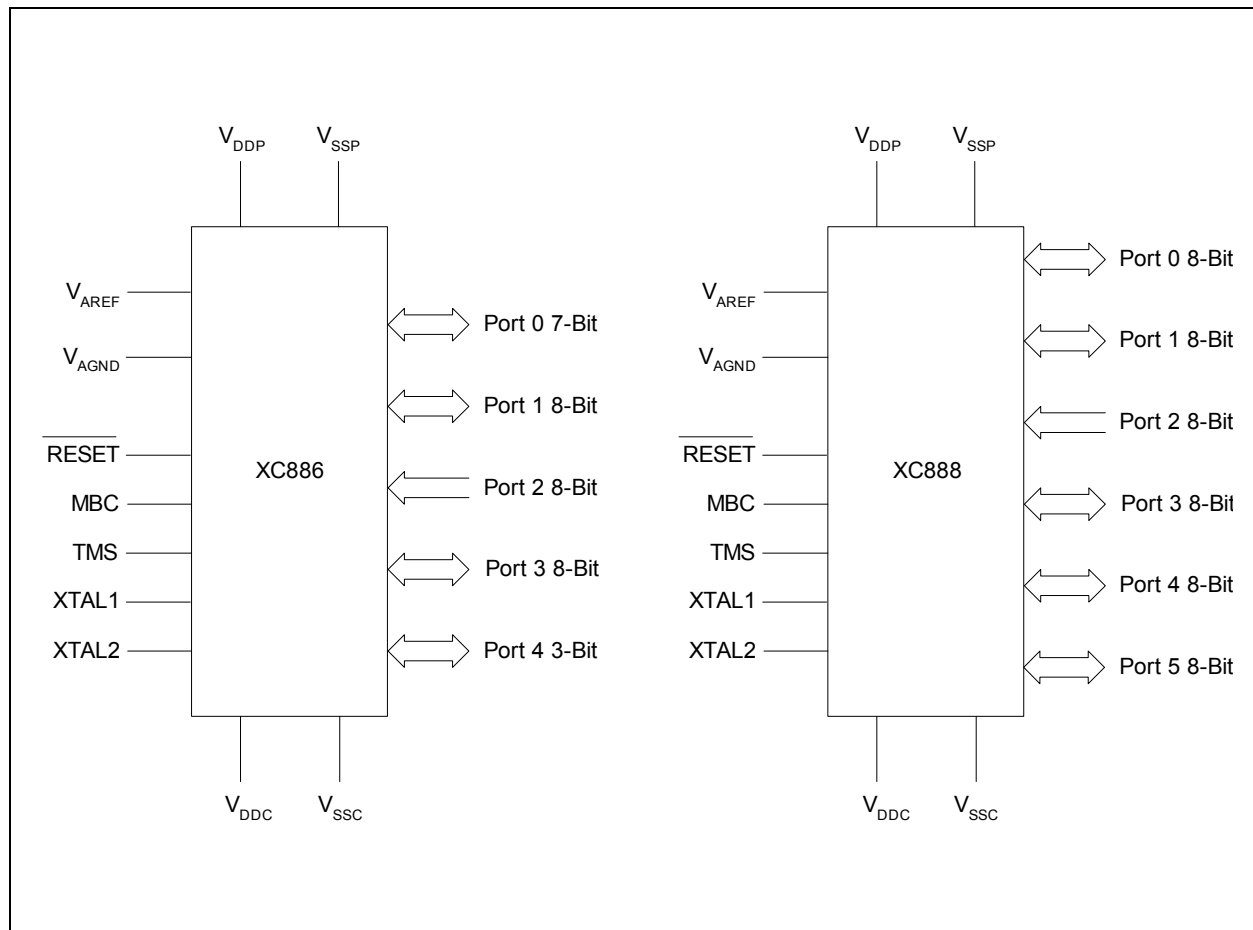


Figure 3 XC886/888 Logic Symbol

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.
P1.0	26/34		PU	RXD_0 UART Receive Data Input T2EX Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input
P1.1	27/35		PU	EXINT3 External Interrupt Input 3 T0_1 Timer 0 Input TDO_1 JTAG Serial Data Output TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output
P1.2	28/36		PU	SCK_0 SSC Clock Input/Output
P1.3	29/37		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input TXDC1_3 MultiCAN Node 1 Transmitter Output
P1.4	30/38		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input
P1.5	31/39		PU	CCPOS0_1 CCU6 Hall Input 0 EXINT5 External Interrupt Input 5 T1_1 Timer 1 Input EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output

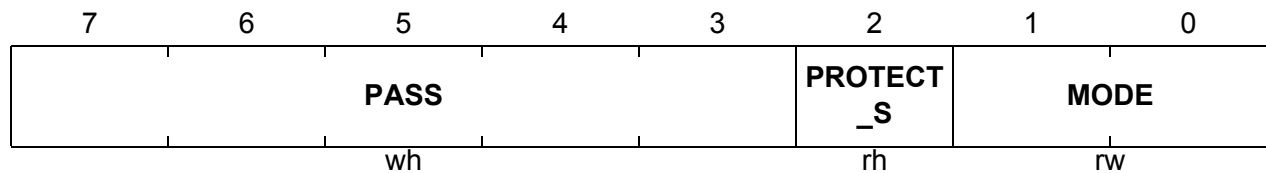
Functional Description

3.2.3.1 Password Register

PASSWD

Password Register

Reset Value: 07_H



Field	Bits	Type	Description
MODE	[1:0]	rw	Bit Protection Scheme Control Bits 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others: Scheme Enabled. These two bits cannot be written directly. To change the value between 11 _B and 00 _B , the bit field PASS must be written with 11000 _B ; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	Bit Protection Signal Status Bit This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits.
PASS	[7:3]	wh	Password Bits The Bit Protection Scheme only recognizes three patterns. 11000 _B Enables writing of the bit field MODE. 10011 _B Opens access to writing of all protected bits. 10101 _B Closes access to writing of all protected bits

Functional Description

Table 7 CORDIC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
A0 _H	CD_STATC Reset: 00 _H CORDIC Status and Data Control Register	Bit Field	KEEP Z	KEEP Y	KEEP X	DMAP	INT_EN	EOC	ERROR	BSY
		Type	rw	rw	rw	rw	rw	rwh	rh	rh
A1 _H	CD_CON Reset: 00 _H CORDIC Control Register	Bit Field	MPS		X_USIGN	ST_MODE	ROTV EC	MODE		ST
		Type	rw		rw	rw	rw	rw		rwh

3.2.4.4 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 8 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0 or 1										
8F _H	SYSCON0 Reset: 04_H System Control Register 0	Bit Field	0			IMOD E	0	1	0	RMAP
		Type	r			rw	r	r	r	rw
RMAP = 0										
BF _H	SCU_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
B3 _H	MODPISEL Reset: 00_H Peripheral Input Select Register	Bit Field	0	URRIS H	JTAGT DIS	JTAGT CKS	EXINT 2IS	EXINT 1IS	EXINT 0IS	URRIS
		Type	r	rw	rw	rw	rw	rw	rw	rw
B4 _H	IRCON0 Reset: 00_H Interrupt Request Register 0	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B5 _H	IRCON1 Reset: 00_H Interrupt Request Register 1	Bit Field	0	CANS RC2	CANS RC1	ADCS R1	ADCS R0	RIR	TIR	EIR
		Type	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
B6 _H	IRCON2 Reset: 00_H Interrupt Request Register 2	Bit Field	0			CANS RC3	0			CANS RC0
		Type	r			rwh	r			rwh
B7 _H	EXICON0 Reset: F0_H External Interrupt Control Register 0	Bit Field	EXINT3		EXINT2		EXINT1		EXINT0	
		Type	rw		rw		rw		rw	
BA _H	EXICON1 Reset: 3F_H External Interrupt Control Register 1	Bit Field	0		EXINT6		EXINT5		EXINT4	
		Type	r		rw		rw		rw	
BB _H	NMICON Reset: 00_H NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	NMI VDD	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT
		Type	r	rw	rw	rw	rw	rw	rw	rw

Functional Description
Table 9 WDT Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE _H	WDTL Reset: 00_H Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF _H	WDTH Reset: 00_H Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
B2 _H	PORT_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
80 _H	P0_DATA Reset: 00_H P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86 _H	P0_DIR Reset: 00_H P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_DATA Reset: 00_H P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91 _H	P1_DIR Reset: 00_H P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_DATA Reset: 00_H P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93 _H	P5_DIR Reset: 00_H P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
A0 _H	P2_DATA Reset: 00_H P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
A1 _H	P2_DIR Reset: 00_H P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_DATA Reset: 00_H P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_DIR Reset: 00_H P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_DATA Reset: 00_H P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_DIR Reset: 00_H P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Functional Description

Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
93 _H	P5_ALTSEL1 Reset: 00_H P5 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_ALTSEL0 Reset: 00_H P3 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B1 _H	P3_ALTSEL1 Reset: 00_H P3 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_ALTSEL0 Reset: 00_H P4 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C9 _H	P4_ALTSEL1 Reset: 00_H P4 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 3										
80 _H	P0_OD Reset: 00_H P0 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90 _H	P1_OD Reset: 00_H P1 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92 _H	P5_OD Reset: 00_H P5 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
B0 _H	P3_OD Reset: 00_H P3 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C8 _H	P4_OD Reset: 00_H P4 Open Drain Control Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.7 ADC Registers

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 11 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
D1 _H	ADC_PAGE Reset: 00_H Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
CA _H	ADC_GLOBCTR Reset: 30_H Global Control Register	Bit Field	ANON	DW	CTC		0			
		Type	rw	rw	rw		r			
CB _H	ADC_GLOBSTR Reset: 00_H Global Status Register	Bit Field	0		CHNR			0	SAMP LE	BUSY
		Type	r		rh			r	rh	rh
CC _H	ADC_PRAR Reset: 00_H Priority and Arbitration Register	Bit Field	ASEN 1	ASEN 0	0	ARBM	CSM1	PRI01	CSM0	PRI00
		Type	rw	rw	r	rw	rw	rw	rw	rw

Functional Description
Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CD _H	ADC_LCBR Reset: B7 _H Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE _H	ADC_INPCR0 Reset: 00 _H Input Class 0 Register	Bit Field	STC							
		Type	rw							
CF _H	ADC_ETRCR Reset: 00 _H External Trigger Control Register	Bit Field	SYNE N1	SYNE N0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, PAGE 1										
CA _H	ADC_CHCTR0 Reset: 00 _H Channel Control Register 0	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CB _H	ADC_CHCTR1 Reset: 00 _H Channel Control Register 1	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CC _H	ADC_CHCTR2 Reset: 00 _H Channel Control Register 2	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CD _H	ADC_CHCTR3 Reset: 00 _H Channel Control Register 3	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CE _H	ADC_CHCTR4 Reset: 00 _H Channel Control Register 4	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
CF _H	ADC_CHCTR5 Reset: 00 _H Channel Control Register 5	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D2 _H	ADC_CHCTR6 Reset: 00 _H Channel Control Register 6	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
D3 _H	ADC_CHCTR7 Reset: 00 _H Channel Control Register 7	Bit Field	0	LCC			0	RESRSEL		
		Type	r	rw			r	rw		
RMAP = 0, PAGE 2										
CA _H	ADC_RESR0L Reset: 00 _H Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB _H	ADC_RESR0H Reset: 00 _H Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC _H	ADC_RESR1L Reset: 00 _H Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD _H	ADC_RESR1H Reset: 00 _H Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE _H	ADC_RESR2L Reset: 00 _H Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF _H	ADC_RESR2H Reset: 00 _H Result Register 2 High	Bit Field	RESULT							
		Type	rh							
D2 _H	ADC_RESR3L Reset: 00 _H Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		

Functional Description

3.2.4.8 Timer 2 Registers

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
C0 _H	T2_T2CON Reset: 00_H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN 2	TR2	C/ $\overline{T2}$	CP/ RL2
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1 _H	T2_T2MOD Reset: 00_H Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H	T2_RC2L Reset: 00_H Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3 _H	T2_RC2H Reset: 00_H Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4 _H	T2_T2L Reset: 00_H Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
C5 _H	T2_T2H Reset: 00_H Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
C0 _H	T21_T2CON Reset: 00_H Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN 2	TR2	C/ $\overline{T2}$	CP/ RL2
		Type	rwh	rwh	r		rw	rwh	rw	rw
C1 _H	T21_T2MOD Reset: 00_H Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H	T21_RC2L Reset: 00_H Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
C3 _H	T21_RC2H Reset: 00_H Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
C4 _H	T21_T2L Reset: 00_H Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							

Functional Description

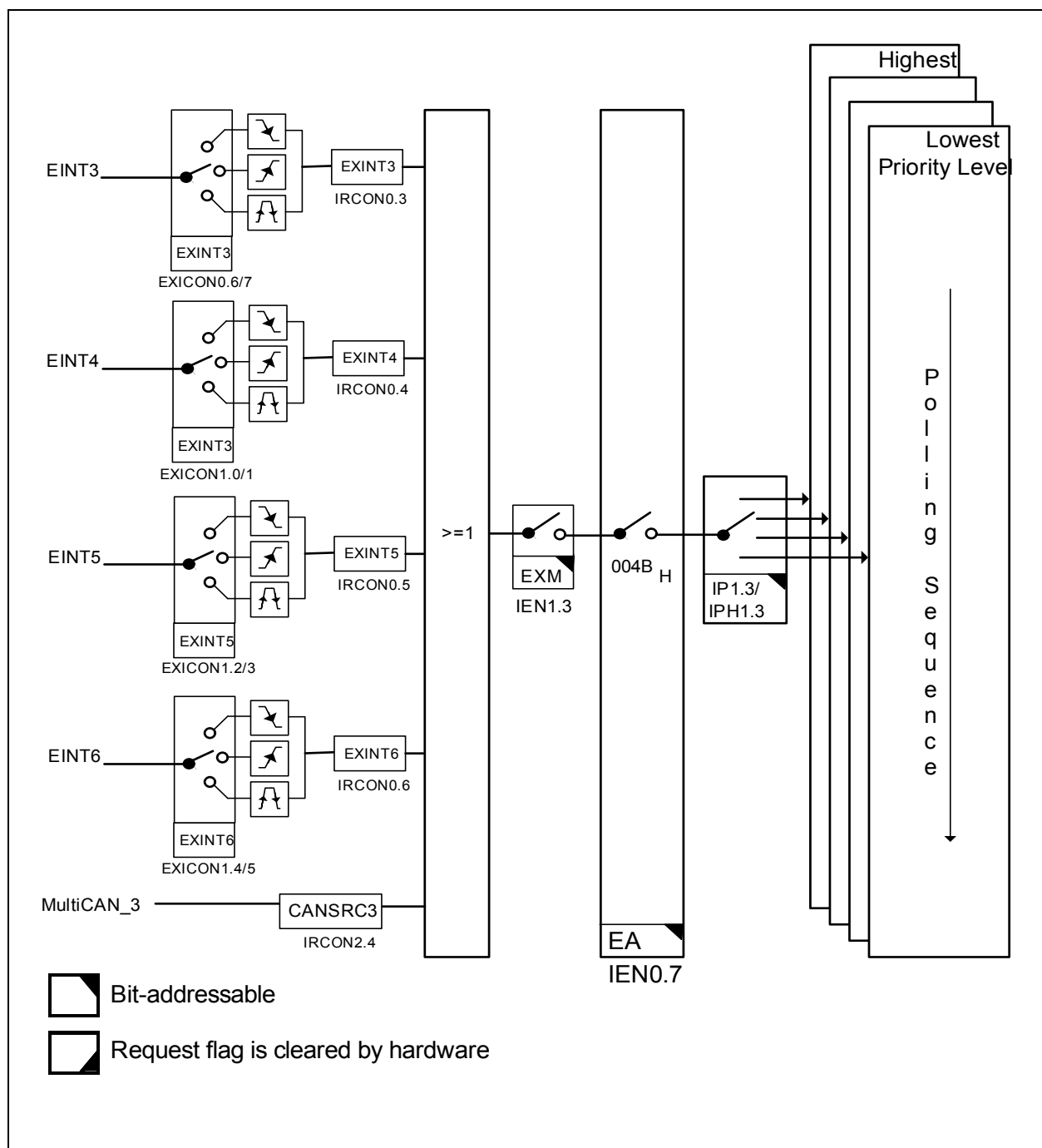


Figure 17 Interrupt Request Sources (Part 4)

Functional Description

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in [Table 21](#).

Table 21 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
Timer 2, UART Normal Divider Overflow, MultiCAN, LIN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
CCU6 Interrupt Node Pointer 0, MultiCAN interrupt	11
CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt	12
CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt	13
CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt	14

Functional Description

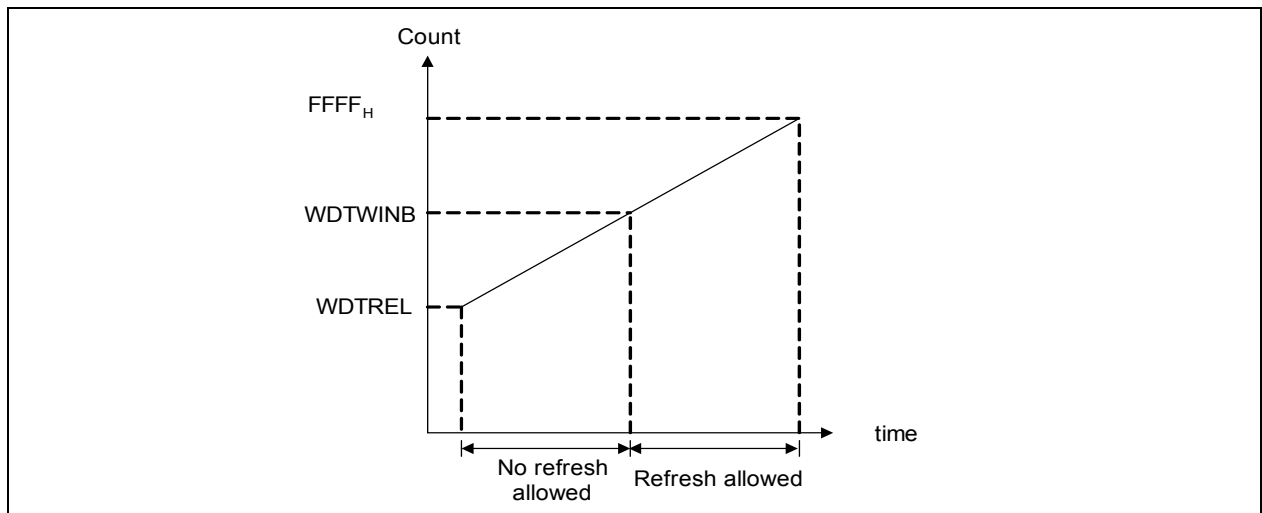


Figure 29 WDT Timing Diagram

Table 27 lists the possible watchdog time ranges that can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 27 Watchdog Time Ranges

Reload value In WDTREL	Prescaler for f_{PCLK}	
	2 (WDTIN = 0)	128 (WDTIN = 1)
	24 MHz	24 MHz
FF _H	21.3 μ s	1.37 ms
7F _H	2.75 ms	176 ms
00 _H	5.46 ms	350 ms

Functional Description

GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

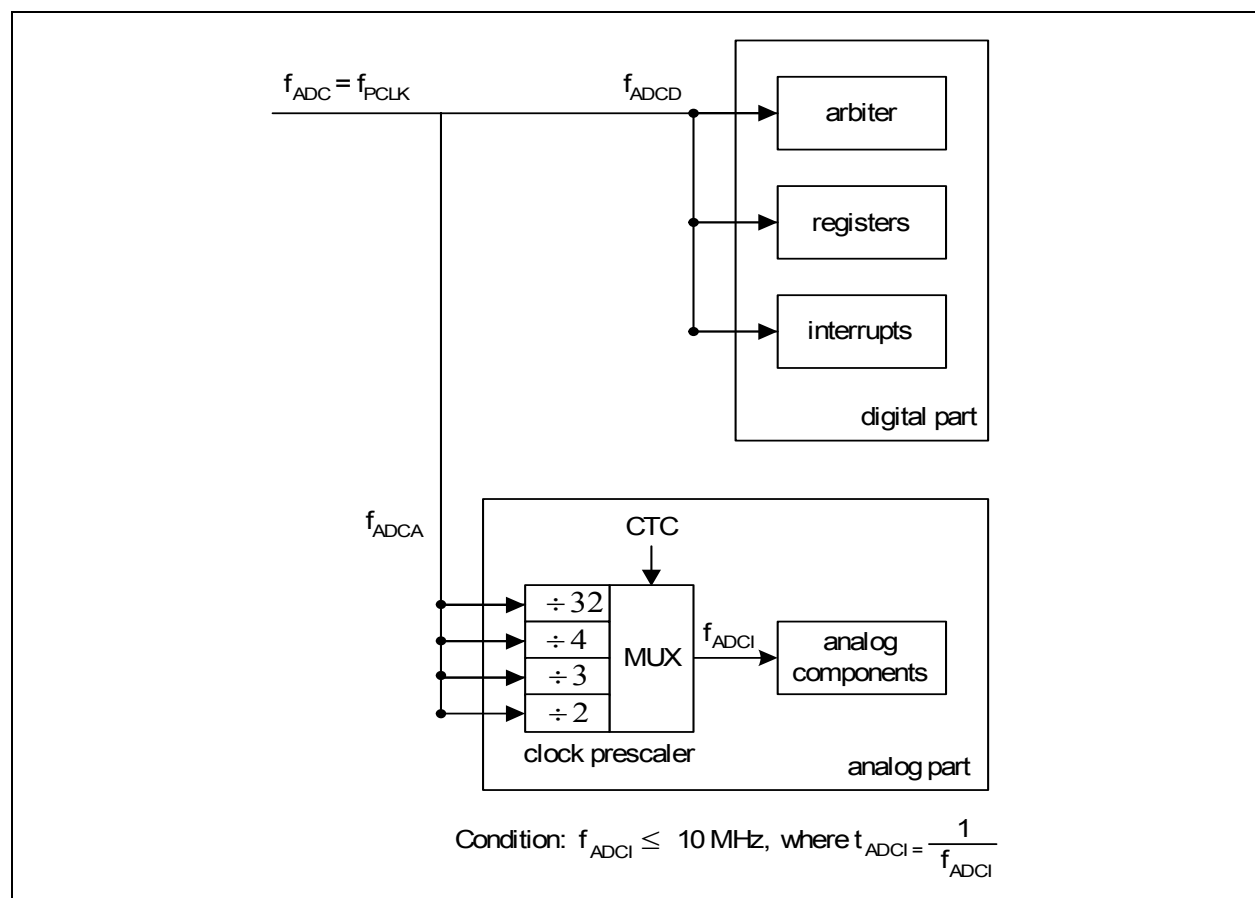


Figure 35 ADC Clocking Scheme

For module clock $f_{ADC} = 24 \text{ MHz}$, the analog clock f_{ADCI} frequency can be selected as shown in [Table 34](#).

Table 34 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00 _B	$\div 2$	12 MHz (N.A)
	01 _B	$\div 3$	8 MHz
	10 _B	$\div 4$	6 MHz
	11 _B (default)	$\div 32$	750 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 24 MHz. During slow-down mode where f_{ADC} may be reduced to 12 MHz, 6 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz.

Functional Description

Table 36 **Chip Identification Number (cont'd)**

Product Variant	Chip Identification Number		
	AA-Step	AB-Step	AC-Step
XC888CM-6RFA 5V	22891503 _H	-	-
XC886C-6RFA 5V	22891542 _H	-	-
XC888C-6RFA 5V	22891543 _H	-	-
XC886-6RFA 5V	22891562 _H	-	-
XC888-6RFA 5V	22891563 _H	-	-

4 Electrical Parameters

Chapter 4 provides the characteristics of the electrical parameters which are implementation-specific for the XC886/888.

4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in [Section 4.2](#) and [Section 4.3](#).

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC886/888 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC886/888 and must be regarded for a system design.
- **SR**
These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC886/888 is designed in.

Electrical Parameters

4.3.3 Power-on Reset and PLL Timing

Table 49 provides the characteristics of the power-on reset and PLL timing in the XC886/888.

Table 46 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Pad operating voltage	V_{PAD}	CC	2.3	–	–	V	¹⁾
On-Chip Oscillator start-up time	t_{OSCST}	CC	–	–	500	ns	¹⁾
Flash initialization time	t_{FINIT}	CC	–	160	–	μs	¹⁾
RESET hold time	t_{RST}	SR	–	500	–	μs	V_{DDP} rise time (10% – 90%) ≤ 500μs ¹⁾²⁾
PLL lock-in in time	t_{LOCK}	CC	–	–	200	μs	¹⁾
PLL accumulated jitter	D_P		–	–	0.7	ns	¹⁾³⁾

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) RESET signal has to be active (low) until V_{DDC} has reached 90% of its maximum value (typ. 2.5 V).

3) PLL lock at 96 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 48 and P = 1.

Electrical Parameters

Table 50 JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter	Symbol	Limits		Unit	Test Conditions
		min	max		
TDO high impedance to valid output from TCK	t_4 CC	-	27	ns	5V Device ¹⁾
		-	36	ns	3.3V Device ¹⁾
TDO valid output to high impedance from TCK	t_5 CC	-	22	ns	5V Device ¹⁾
		-	28	ns	3.3V Device ¹⁾

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

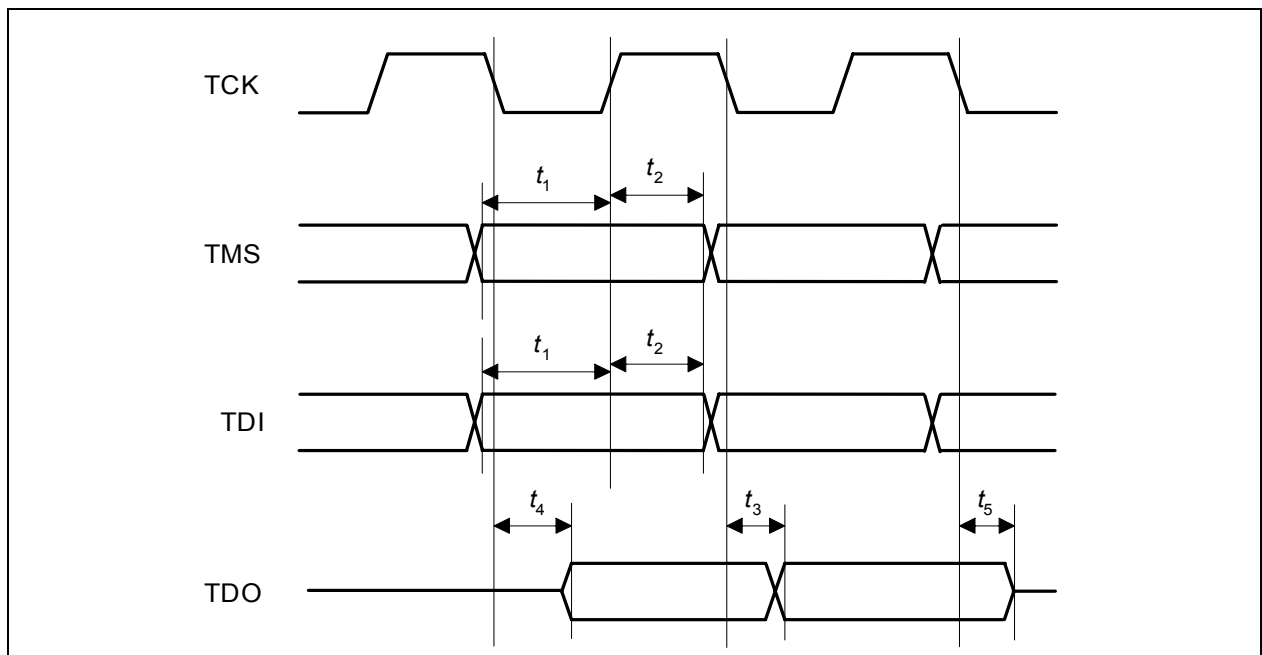


Figure 47 JTAG Timing

Package and Quality Declaration

Figure 49 shows the package outlines of the XC888.

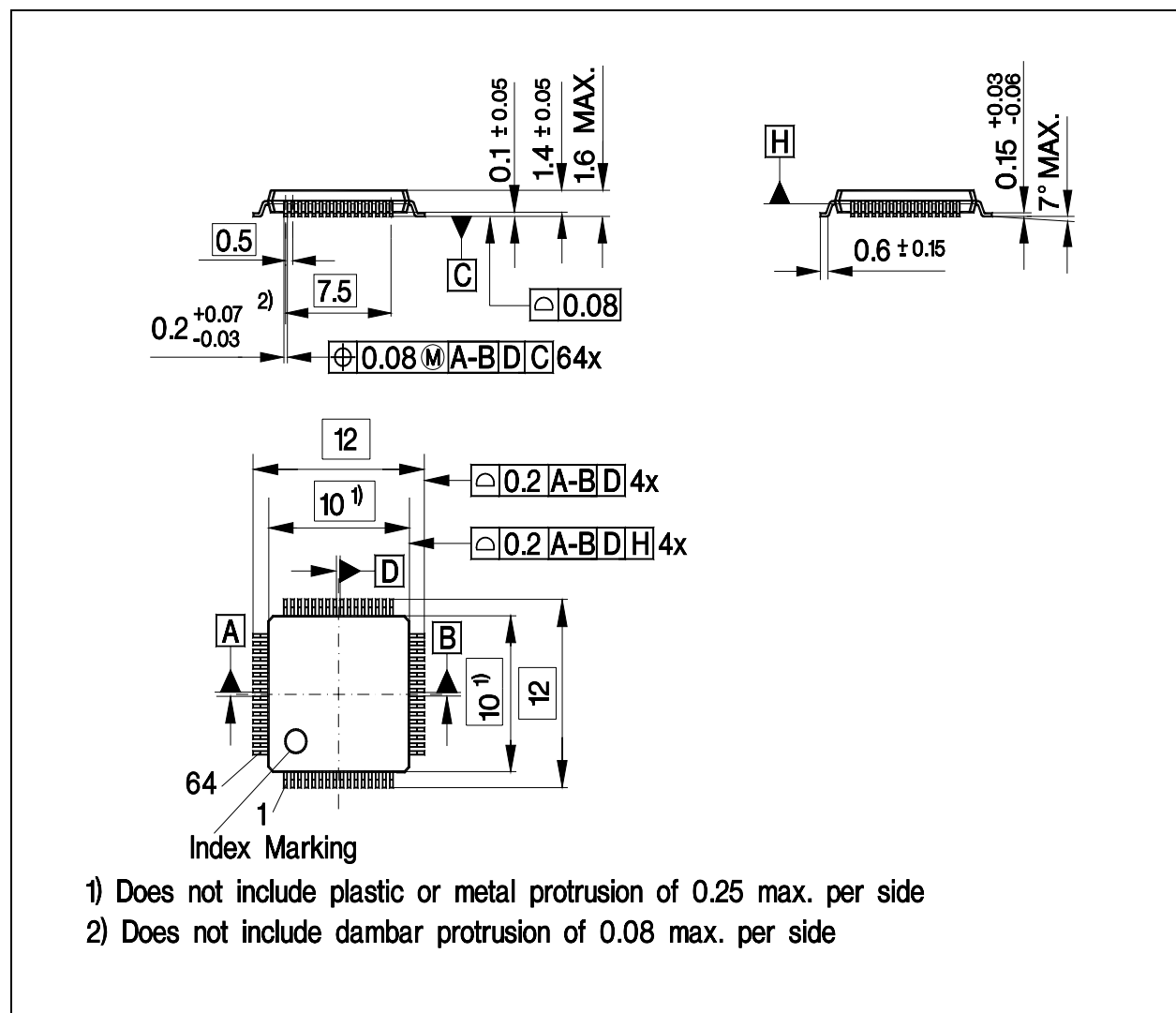


Figure 49 PG-TQFP-64 Package Outline