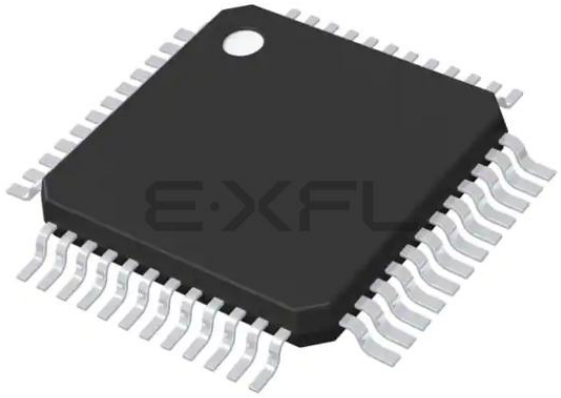
Infineon Technologies - SAK-XC886-8FFA 5V AC Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886-8ffa-5v-ac

Edition 2009-07

Published by
Infineon Technologies AG
81726 Munich, Germany

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Never stop thinking

8-Bit

XC886/888CLM

8-Bit Single Chip Microcontroller

Data Sheet

V1.2 2009-07

Microcontrollers

Table 2 Device Profile (cont'd)

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp-erature (°C)	Quality Profile
SAK-XC886*/888*-8FFA 3V3	Flash	32	3.3	-40 to 125	Automotive
SAK-XC886*/888*-6FFA 3V3	Flash	24	3.3	-40 to 125	Automotive
SAF-XC886*/888*-8FFA 3V3	Flash	32	3.3	-40 to 85	Automotive
SAF-XC886*/888*-6FFA 3V3	Flash	24	3.3	-40 to 85	Automotive
SAF-XC886*/888*-8FFI 3V3	Flash	32	3.3	-40 to 85	Industrial
SAF-XC886*/888*-6FFI 3V3	Flash	24	3.3	-40 to 85	Industrial

*Note: The asterisk (*) above denotes the device configuration letters from **Table 1**. Corresponding ROM derivatives will be available on request.*

Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC886/888 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC886/888, please refer to your responsible sales representative or your local distributor.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

2 General Device Information

Chapter 2 contains the block diagram, pin configurations, definitions and functions of the XC886/888.

2.1 Block Diagram

The block diagram of the XC886/888 is shown in **Figure 2**.

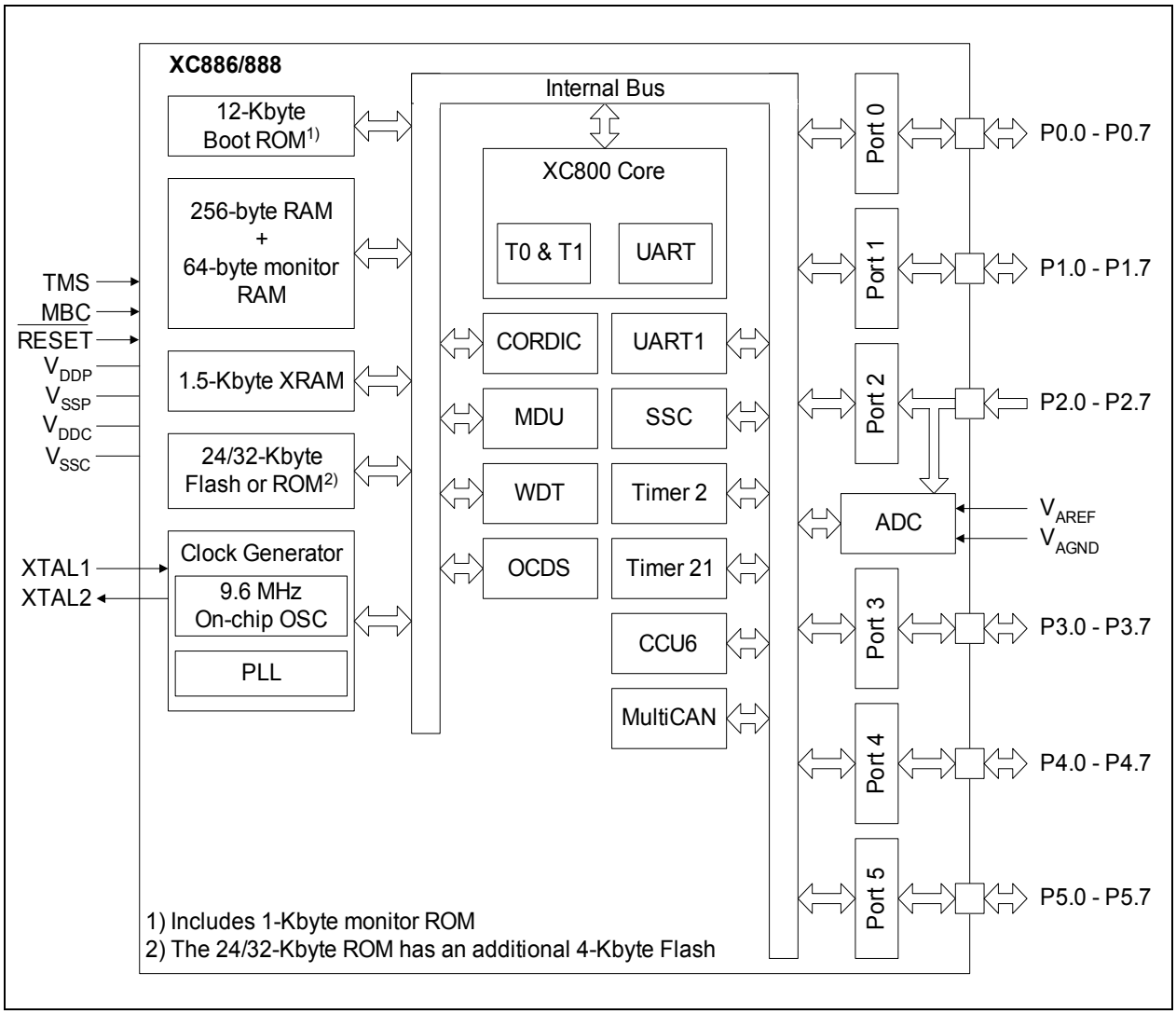

Figure 2 XC886/888 Block Diagram

2.4 Pin Definitions and Functions

The functions and default states of the XC886/888 external pins are provided in **Table 3**.

Table 3 Pin Definitions and Functions

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P0		I/O		**Port 0** Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, Timer 2, Timer 21, MultiCAN and SSC.
P0.0	11/17		Hi-Z	TCK_0 JTAG Clock Input T12HR_1 CCU6 Timer 12 Hardware Run Input CC61_1 Input/Output of Capture/Compare channel 1 CLKOUT_0 Clock Output RXDO_1 UART Transmit Data Output
P0.1	13/21		Hi-Z	TDI_0 JTAG Serial Data Input T13HR_1 CCU6 Timer 13 Hardware Run Input RXD_1 UART Receive Data Input RXDC1_0 MultiCAN Node 1 Receiver Input COUT61_1 Output of Capture/Compare channel 1 EXF2_1 Timer 2 External Flag Output
P0.2	12/18		PU	$\overline{\text{CTRAP}}$_2 CCU6 Trap Input TDO_0 JTAG Serial Data Output TXD_1 UART Transmit Data Output/Clock Output TXDC1_0 MultiCAN Node 1 Transmitter Output
P0.3	48/63		Hi-Z	SCK_1 SSC Clock Input/Output COUT63_1 Output of Capture/Compare channel 3 RXDO1_0 UART1 Transmit Data Output

3.2 Memory Organization

The XC886/888 CPU operates in the following five address spaces:

- 12 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 1.5 Kbytes of XRAM memory
  (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 24/32 Kbytes of Flash program memory (Flash devices); or
  24/32 Kbytes of ROM program memory, with additional 4 Kbytes of Flash
  (ROM devices)

Figure 7 illustrates the memory address spaces of the 32-Kbyte Flash devices. For the 24-Kbyte Flash devices, the shaded banks are not available.

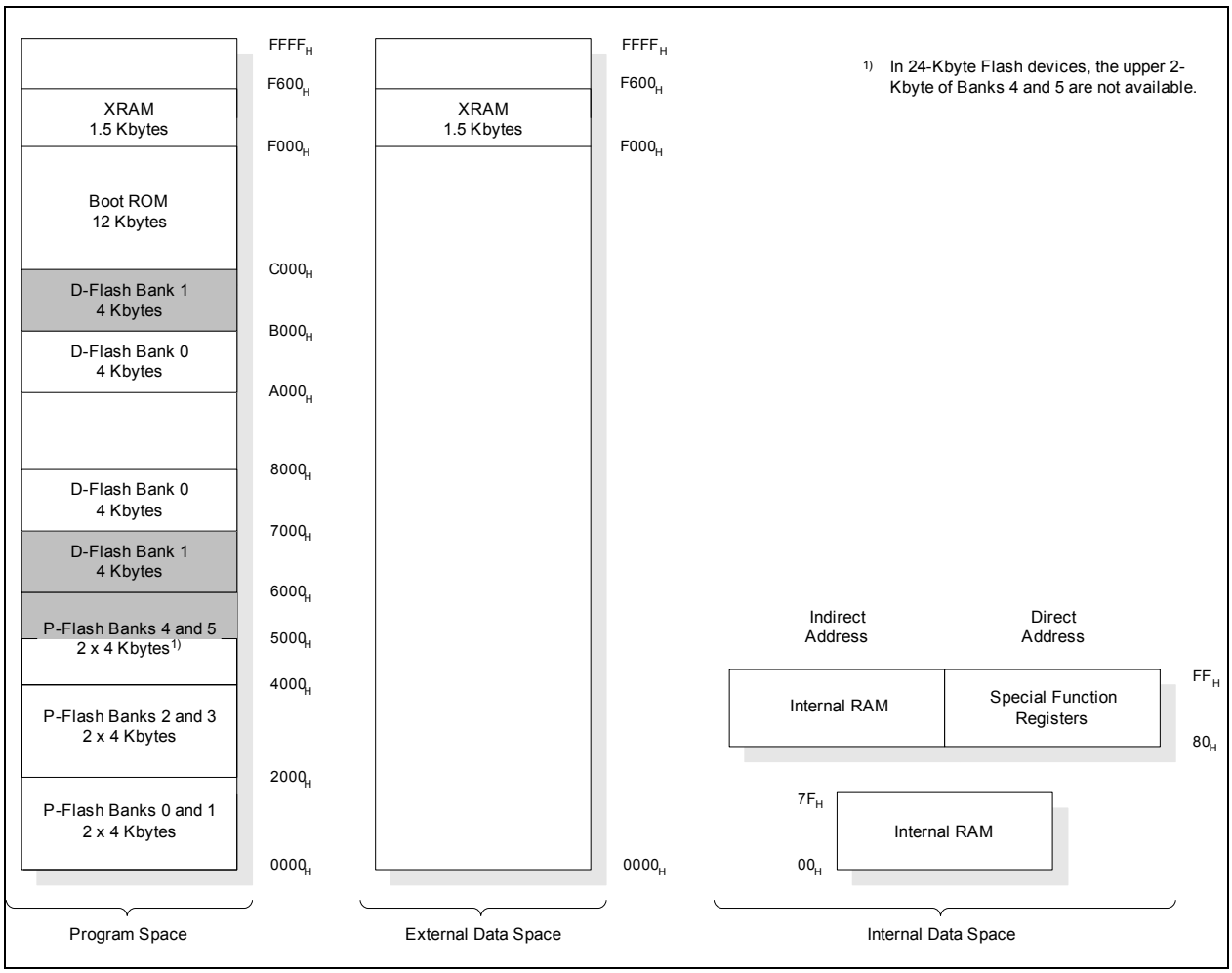

Figure 7 Memory Map of XC886/888 Flash Device

For both 24-Kbyte and 32-Kbyte ROM devices, the last four bytes of the ROM from $7FFC_H$ to $7FFF_H$ are reserved for the ROM signature and cannot be used to store user

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
CD_H	**ADC_LCBR Reset: $B7_H$** Limit Check Boundary Register	Bit Field	BOUND1				BOUND0			
		Type	rw				rw			
CE_H	**ADC_INPCR0 Reset: 00_H** Input Class 0 Register	Bit Field	STC							
		Type	rw							
CF_H	**ADC_ETRCR Reset: 00_H** External Trigger Control Register	Bit Field	SYNEN1	SYNEN0	ETRSEL1			ETRSEL0		
		Type	rw	rw	rw			rw		
RMAP = 0, PAGE 1										
CA_H	**ADC_CHCTR0 Reset: 00_H** Channel Control Register 0	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CB_H	**ADC_CHCTR1 Reset: 00_H** Channel Control Register 1	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CC_H	**ADC_CHCTR2 Reset: 00_H** Channel Control Register 2	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CD_H	**ADC_CHCTR3 Reset: 00_H** Channel Control Register 3	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CE_H	**ADC_CHCTR4 Reset: 00_H** Channel Control Register 4	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
CF_H	**ADC_CHCTR5 Reset: 00_H** Channel Control Register 5	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
$D2_H$	**ADC_CHCTR6 Reset: 00_H** Channel Control Register 6	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
$D3_H$	**ADC_CHCTR7 Reset: 00_H** Channel Control Register 7	Bit Field	0	LCC			0		RESRSEL	
		Type	r	rw			r		rw	
RMAP = 0, PAGE 2										
CA_H	**ADC_RESR0L Reset: 00_H** Result Register 0 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CB_H	**ADC_RESR0H Reset: 00_H** Result Register 0 High	Bit Field	RESULT							
		Type	rh							
CC_H	**ADC_RESR1L Reset: 00_H** Result Register 1 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CD_H	**ADC_RESR1H Reset: 00_H** Result Register 1 High	Bit Field	RESULT							
		Type	rh							
CE_H	**ADC_RESR2L Reset: 00_H** Result Register 2 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		
CF_H	**ADC_RESR2H Reset: 00_H** Result Register 2 High	Bit Field	RESULT							
		Type	rh							
$D2_H$	**ADC_RESR3L Reset: 00_H** Result Register 3 Low	Bit Field	RESULT		0	VF	DRC	CHNR		
		Type	rh		r	rh	rh	rh		

3.2.4.8 Timer 2 Registers

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$C0_H$	**T2_T2CON** **Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T2_T2MOD** **Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C2_H$	**T2_RC2L** **Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T2_RC2H** **Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T2_T2L** **Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							
$C5_H$	**T2_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C0_H$	**T21_T2CON** **Reset: 00_H** Timer 2 Control Register	Bit Field	TF2	EXF2	0		EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
		Type	rwh	rwh	r		rw	rwh	rw	rw
$C1_H$	**T21_T2MOD** **Reset: 00_H** Timer 2 Mode Register	Bit Field	T2REGS	T2RHEN	EDGESEL	PREN	T2PRE			DCEN
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C2_H$	**T21_RC2L** **Reset: 00_H** Timer 2 Reload/Capture Register Low	Bit Field	RC2							
		Type	rwh							
$C3_H$	**T21_RC2H** **Reset: 00_H** Timer 2 Reload/Capture Register High	Bit Field	RC2							
		Type	rwh							
$C4_H$	**T21_T2L** **Reset: 00_H** Timer 2 Register Low	Bit Field	THL2							
		Type	rwh							

Table 13 T21 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$C5_H$	**T21_T2H** **Reset: 00_H** Timer 2 Register High	Bit Field	THL2							
		Type	rwh							

3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$A3_H$	**CCU6_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
$9A_H$	**CCU6_CC63SRL** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 Low	Bit Field	CC63SL							
		Type	rw							
$9B_H$	**CCU6_CC63SRH** **Reset: 00_H** Capture/Compare Shadow Register for Channel CC63 High	Bit Field	CC63SH							
		Type	rw							
$9C_H$	**CCU6_TCTR4L** **Reset: 00_H** Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	0		DT RES	T12 RES	T12R S	T12R R
		Type	w	w	r		w	w	w	w
$9D_H$	**CCU6_TCTR4H** **Reset: 00_H** Timer Control Register 4 High	Bit Field	T13 STD	T13 STR	0			T13 RES	T13R S	T13R R
		Type	w	w	r			w	w	w
$9E_H$	**CCU6_MCMOUTSL** **Reset: 00_H** Multi-Channel Mode Output Shadow Register Low	Bit Field	STRM CM	0	MCMPS					
		Type	w	r	rw					
$9F_H$	**CCU6_MCMOUTSH** **Reset: 00_H** Multi-Channel Mode Output Shadow Register High	Bit Field	STRH P	0	CURHS			EXPHS		
		Type	w	r	rw			rw		
$A4_H$	**CCU6_ISRL** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register Low	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
		Type	w	w	w	w	w	w	w	w
$A5_H$	**CCU6_ISRH** **Reset: 00_H** Capture/Compare Interrupt Status Reset Register High	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
		Type	w	w	w	w	r	w	w	w
$A6_H$	**CCU6_CMPMODIFL** **Reset: 00_H** Compare State Modification Register Low	Bit Field	0	MCC6 3S	0			MCC6 2S	MCC6 1S	MCC6 0S
		Type	r	w	r			w	w	w
$A7_H$	**CCU6_CMPMODIFH** **Reset: 00_H** Compare State Modification Register High	Bit Field	0	MCC6 3R	0			MCC6 2R	MCC6 1R	MCC6 0R
		Type	r	w	r			w	w	w

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FA_H	**CCU6_CC60SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 Low	Bit Field	CC60SL							
		Type	rwh							
FB_H	**CCU6_CC60SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC60 High	Bit Field	CC60SH							
		Type	rwh							
FC_H	**CCU6_CC61SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 Low	Bit Field	CC61SL							
		Type	rwh							
FD_H	**CCU6_CC61SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC61 High	Bit Field	CC61SH							
		Type	rwh							
FE_H	**CCU6_CC62SRL Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 Low	Bit Field	CC62SL							
		Type	rwh							
FF_H	**CCU6_CC62SRH Reset: 00_H** Capture/Compare Shadow Register for Channel CC62 High	Bit Field	CC62SH							
		Type	rwh							
RMAP = 0, PAGE 1										
$9A_H$	**CCU6_CC63RL Reset: 00_H** Capture/Compare Register for Channel CC63 Low	Bit Field	CC63VL							
		Type	rh							
$9B_H$	**CCU6_CC63RH Reset: 00_H** Capture/Compare Register for Channel CC63 High	Bit Field	CC63VH							
		Type	rh							
$9C_H$	**CCU6_T12PRL Reset: 00_H** Timer T12 Period Register Low	Bit Field	T12PVL							
		Type	rwh							
$9D_H$	**CCU6_T12PRH Reset: 00_H** Timer T12 Period Register High	Bit Field	T12PVH							
		Type	rwh							
$9E_H$	**CCU6_T13PRL Reset: 00_H** Timer T13 Period Register Low	Bit Field	T13PVL							
		Type	rwh							
$9F_H$	**CCU6_T13PRH Reset: 00_H** Timer T13 Period Register High	Bit Field	T13PVH							
		Type	rwh							
$A4_H$	**CCU6_T12DTCL Reset: 00_H** Dead-Time Control Register for Timer T12 Low	Bit Field	DTM							
		Type	rw							
$A5_H$	**CCU6_T12DTCH Reset: 00_H** Dead-Time Control Register for Timer T12 High	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0
		Type	r	rh	rh	rh	r	rw	rw	rw
$A6_H$	**CCU6_TCTR0L Reset: 00_H** Timer Control Register 0 Low	Bit Field	CTM	CDIR	STE12	T12R	T12PRE	T12CLK		
		Type	rw	rh	rh	rh	rw	rw		
$A7_H$	**CCU6_TCTR0H Reset: 00_H** Timer Control Register 0 High	Bit Field	0		STE13	T13R	T13PRE	T13CLK		
		Type	r		rh	rh	rw	rw		
FA_H	**CCU6_CC60RL Reset: 00_H** Capture/Compare Register for Channel CC60 Low	Bit Field	CC60VL							
		Type	rh							

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FE_H	**CCU6_CMPSTATL Reset: 00_H** Compare State Register Low	Bit Field	0	CC63 ST	CC POS2	CC POS1	CC POS0	CC62 ST	CC61 ST	CC60 ST
		Type	r	rh	rh	rh	rh	rh	rh	rh
FF_H	**CCU6_CMPSTATH Reset: 00_H** Compare State Register High	Bit Field	T13IM	COUT 63PS	COUT 62PS	CC62 PS	COUT 61PS	CC61 PS	COUT 60PS	CC60 PS
		Type	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
$C8_H$	**SCON Reset: 00_H** Serial Channel Control Register	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
		Type	rw	rw	rw	rw	rw	rwh	rwh	rwh
$C9_H$	**SBUF Reset: 00_H** Serial Data Buffer Register	Bit Field	VAL							
		Type	rwh							
CA_H	**BCON Reset: 00_H** Baud Rate Control Register	Bit Field	0				BRPRE			R
		Type	r				rw			rw
CB_H	**BG Reset: 00_H** Baud Rate Timer/Reload Register	Bit Field	BR_VALUE							
		Type	rwh							
CC_H	**FDCON Reset: 00_H** Fractional Divider Control Register	Bit Field	0					NDOV	FDM	FDEN
		Type	r					rwh	rw	rw
CD_H	**FDSTEP Reset: 00_H** Fractional Divider Reload Register	Bit Field	STEP							
		Type	rw							
CE_H	**FDRES Reset: 00_H** Fractional Divider Result Register	Bit Field	RESULT							
		Type	rh							

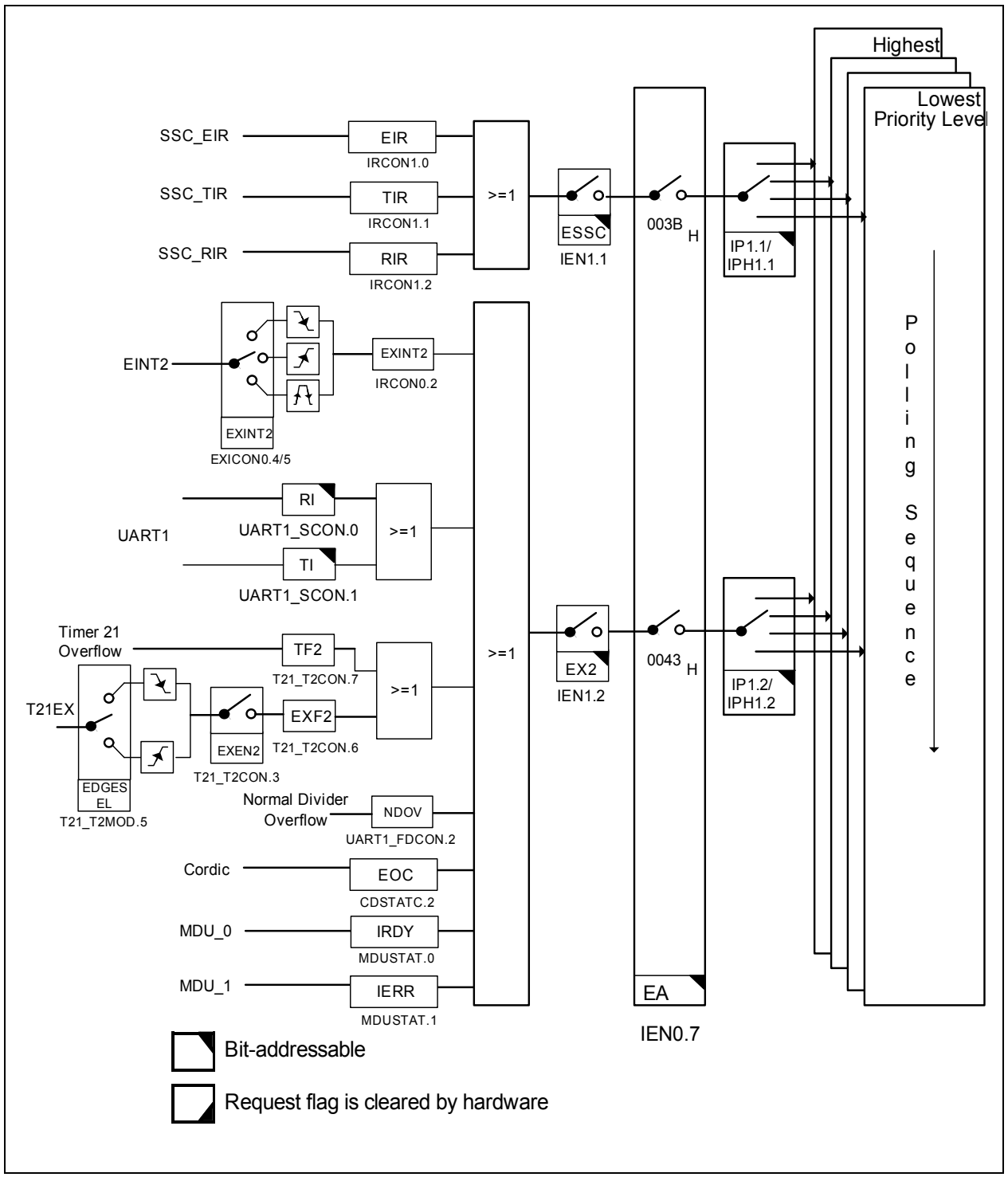

Figure 16 Interrupt Request Sources (Part 3)

Figure 20 shows the structure of an input-only port pin.

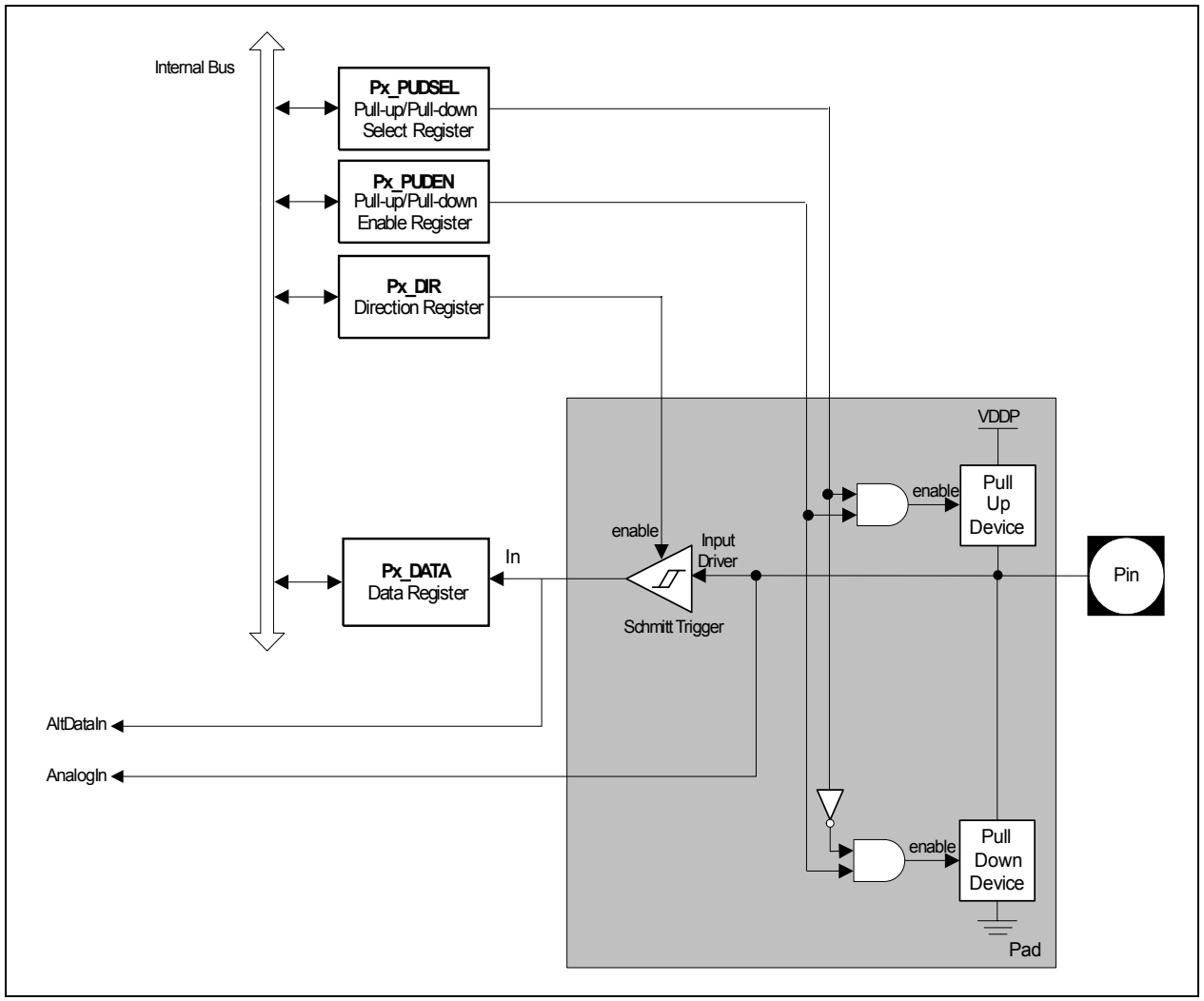

Figure 20 General Structure of Input Port

GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

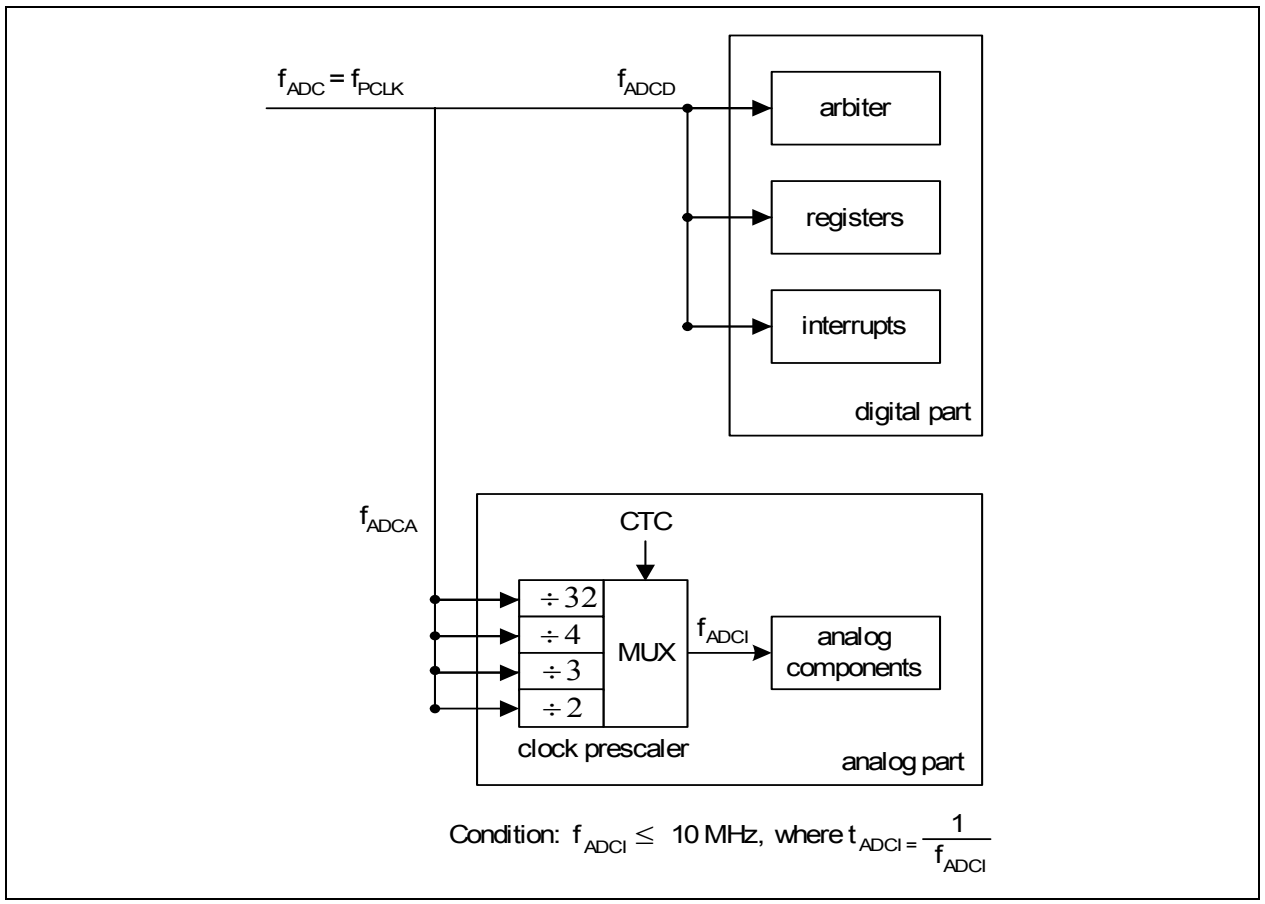

Figure 35 ADC Clocking Scheme

For module clock f_{ADC} = 24 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 34**.

Table 34 f_{ADCI} Frequency Selection

Module Clock f_{ADC}	CTC	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00_B	÷ 2	12 MHz (N.A)
	01_B	÷ 3	8 MHz
	10_B	÷ 4	6 MHz
	11_B (default)	÷ 32	750 kHz

As f_{ADCI} cannot exceed 10 MHz, bit field CTC should not be set to 00_B when f_{ADC} is 24 MHz. During slow-down mode where f_{ADC} may be reduced to 12 MHz, 6 MHz etc., CTC can be set to 00_B as long as the divided analog clock f_{ADCI} does not exceed 10 MHz.

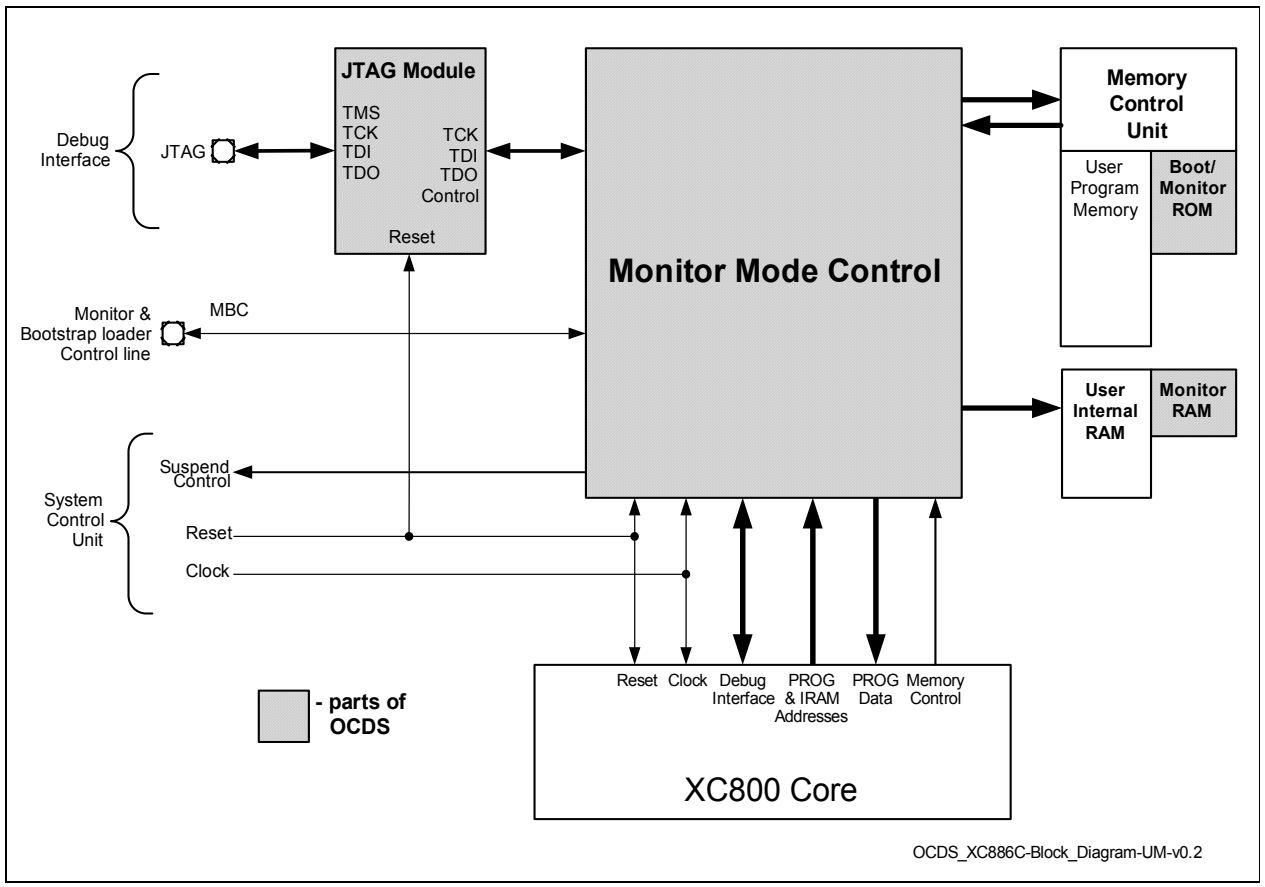

Figure 37 OCDS Block Diagram

3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC886/888 Flash devices are given in **Table 35**.

Table 35 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC886/888*-8FF	$1012\ 0083_H$
	XC886/888*-6FF	$1012\ 5083_H$
ROM	XC886/888*-8RF	$1013\ C083_H$
	XC886/888*-6RF	$1013\ D083_H$

Note: The asterisk (*) above denotes all possible device configurations.

Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	**AB-Step**	**AC-Step**
XC886-6FFA 3V3	-	$095D1562_H$	$0B5D1562_H$
XC888-6FFA 3V3	-	$095D1563_H$	$0B5D1563_H$
XC886CLM-8FFA 5V	-	09900102_H	$0B900102_H$
XC888CLM-8FFA 5V	-	09900103_H	$0B900103_H$
XC886LM-8FFA 5V	-	09900122_H	$0B900122_H$
XC888LM-8FFA 5V	-	09900123_H	$0B900123_H$
XC886CLM-6FFA 5V	-	09951502_H	$0B951502_H$
XC888CLM-6FFA 5V	-	09951503_H	$0B951503_H$
XC886LM-6FFA 5V	-	09951522_H	$0B951522_H$
XC888LM-6FFA 5V	-	09951523_H	$0B951523_H$
XC886CM-8FFA 5V	-	09980102_H	$0B980102_H$
XC888CM-8FFA 5V	-	09980103_H	$0B980103_H$
XC886C-8FFA 5V	-	09980142_H	$0B980142_H$
XC888C-8FFA 5V	-	09980143_H	$0B980143_H$
XC886-8FFA 5V	-	09980162_H	$0B980162_H$
XC888-8FFA 5V	-	09980163_H	$0B980163_H$
XC886CM-6FFA 5V	-	$099D1502_H$	$0B9D1502_H$
XC888CM-6FFA 5V	-	$099D1503_H$	$0B9D1503_H$
XC886C-6FFA 5V	-	$099D1542_H$	$0B9D1542_H$
XC888C-6FFA 5V	-	$099D1543_H$	$0B9D1543_H$
XC886-6FFA 5V	-	$099D1562_H$	$0B9D1562_H$
XC888-6FFA 5V	-	$099D1563_H$	$0B9D1563_H$
ROM Devices			
XC886CLM-8RFA 3V3	22400502_H	-	-
XC888CLM-8RFA 3V3	22400503_H	-	-
XC886LM-8RFA 3V3	22400522_H	-	-
XC888LM-8RFA 3V3	22400523_H	-	-
XC886CLM-6RFA 3V3	22411502_H	-	-
XC888CLM-6RFA 3V3	22411503_H	-	-

4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC886/888. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

Table 37 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes/ Conditions
		min.	max.		
Digital power supply voltage	V_{DDP}	4.5	5.5	V	5V Device
Digital power supply voltage	V_{DDP}	3.0	3.6	V	3.3V Device
Digital ground voltage	V_{SS}	0		V	
Digital core supply voltage	V_{DDC}	2.3	2.7	V	
System Clock Frequency[1)]	f_{SYS}	88.8	103.2	MHz	
Ambient temperature	T_A	-40	85	°C	SAF-XC886/888...
		-40	125	°C	SAK-XC886/888...

1) f_{SYS} is the PLL output clock. During normal operating mode, CPU clock is f_{SYS} / 4. Please refer to **Figure 26** for detailed description.

Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	–	-5	µA	$V_{IHP,min}$
			-50	–	µA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	5	µA	$V_{ILP,max}$
			50	–	µA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$ [2]
Input current at XTAL1	I_{ILX}	CC	- 10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	[3]
Maximum current out of V_{SS}	I_{MVSS}	SR	–	120	mA	[3]

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 40 ADC Characteristics (Operating Conditions apply; V_{DDP} = 5V Range)

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Overload current coupling factor for digital I/O pins	K_{OVD}	CC	–	–	5.0 x 10^{-3}	–	$I_{OV} > 0$ 1)3)
			–	–	1.0 x 10^{-2}	–	$I_{OV} < 0$ 1)3)
Switched capacitance at the reference voltage input	C_{AREFSW}	CC	–	10	20	pF	1)4)
Switched capacitance at the analog voltage inputs	C_{AINSW}	CC	–	5	7	pF	1)5)
Input resistance of the reference input	R_{AREF}	CC	–	1	2	kΩ	1)
Input resistance of the selected analog channel	R_{AIN}	CC	–	1	1.5	kΩ	1)

1) Not subjected to production test, verified by design/characterization

2) TUE is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DDP} = 5.0 V.

3) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ1}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

4) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

5) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

4.3.3 Power-on Reset and PLL Timing

Table 49 provides the characteristics of the power-on reset and PLL timing in the XC886/888.

Table 46 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Pad operating voltage	V_{PAD}	CC	2.3	–	–	V	1)
On-Chip Oscillator start-up time	t_{OSCST}	CC	–	–	500	ns	1)
Flash initialization time	t_{FINIT}	CC	–	160	–	µs	1)
$\overline{\text{RESET}}$ hold time	t_{RST}	SR	–	500	–	µs	V_{DDP} rise time (10% – 90%) ≤ 500µs 1)2)
PLL lock-in in time	t_{LOCK}	CC	–	–	200	µs	1)
PLL accumulated jitter	D_P		–	–	0.7	ns	1)3)

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) $\overline{\text{RESET}}$ signal has to be active (low) until V_{DDC} has reached 90% of its maximum value (typ. 2.5 V).

3) PLL lock at 96 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 48 and P = 1.