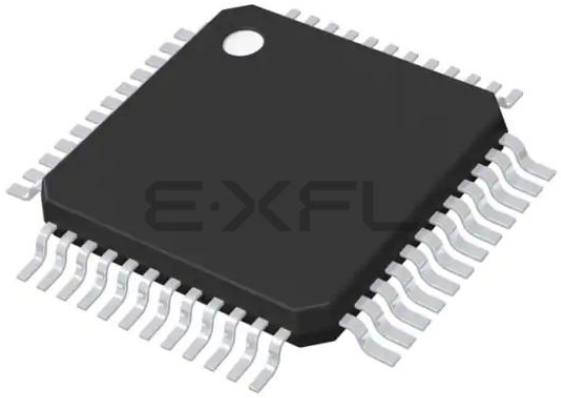
# Infineon Technologies - SAK-XC886C-6FFI 5V AC Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 24KB (24K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.75K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | PG-TQFP-48 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886c-6ffi-5v-ac |

### XC886/888 Variant Devices

The XC886/888 product family features devices with different configurations, program memory sizes, package options, power supply voltage, temperature and quality profiles (Automotive or Industrial), to offer cost-effective solutions for different application requirements.

The list of XC886/888 device configurations are summarized in **Table 1**. For each configuration, 2 types of packages are available:

- PG-TQFP-48, which is denoted by XC886 and;
- PG-TQFP-64, which is denoted by XC888.

**Table 1 Device Configuration**

| Device Name | CAN Module | LIN BSL Support | MDU Module |
|---|---|---|---|
| XC886/888 | No | No | No |
| XC886/888C | Yes | No | No |
| XC886/888CM | Yes | No | Yes |
| XC886/888LM | No | Yes | Yes |
| XC886/888CLM | Yes | Yes | Yes |

*Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.*

From these 10 different combinations of configuration and package type, each are further made available in many sales types, which are grouped according to device type, program memory sizes, power supply voltage, temperature and quality profile (Automotive or Industrial), as shown in **Table 2**.

**Table 2 Device Profile**

| Sales Type | Device Type | Program Memory (Kbytes) | Power Supply (V) | Temp-erature (°C) | Quality Profile |
|---|---|---|---|---|---|
| SAK-XC886*/888*-8FFA 5V | Flash | 32 | 5.0 | -40 to 125 | Automotive |
| SAK-XC886*/888*-6FFA 5V | Flash | 24 | 5.0 | -40 to 125 | Automotive |
| SAF-XC886*/888*-8FFA 5V | Flash | 32 | 5.0 | -40 to 85 | Automotive |
| SAF-XC886*/888*-6FFA 5V | Flash | 24 | 5.0 | -40 to 85 | Automotive |
| SAF-XC886*/888*-8FFI 5V | Flash | 32 | 5.0 | -40 to 85 | Industrial |
| SAF-XC886*/888*-6FFI 5V | Flash | 24 | 5.0 | -40 to 85 | Industrial |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P3.7 | 34/42 | | Hi-Z | EXINT4<br>COUT63_0 | External Interrupt Input 4<br>Output of Capture/Compare channel 3 |

**Table 8 SCU Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $BE_H$ | **COCON** **Reset: $00_H$** Clock Output Control Register | Bit Field | 0 | | TLEN | COUTS | COREL | | | |
| | | Type | r | | rw | rw | rw | | | |
| $E9_H$ | **MISC_CON** **Reset: $00_H$** Miscellaneous Control Register | Bit Field | 0 | | | | | | | DFLASHEN |
| | | Type | r | | | | | | | rwh |
| RMAP = 0, PAGE 3 | | | | | | | | | | |
| $B3_H$ | **XADDRH** **Reset: $F0_H$** On-chip XRAM Address Higher Order | Bit Field | ADDRH | | | | | | | |
| | | Type | rw | | | | | | | |
| $B4_H$ | **IRCON3** **Reset: $00_H$** Interrupt Request Register 3 | Bit Field | 0 | | CANSRC5 | CCU6SR1 | 0 | | CANSRC4 | CCU6SR0 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B5_H$ | **IRCON4** **Reset: $00_H$** Interrupt Request Register 4 | Bit Field | 0 | | CANSRC7 | CCU6SR3 | 0 | | CANSRC6 | CCU6SR2 |
| | | Type | r | | rwh | rwh | r | | rwh | rwh |
| $B7_H$ | **MODPISEL1** **Reset: $00_H$** Peripheral Input Select Register 1 | Bit Field | EXINT6IS | 0 | | UR1RIS | | T21EXIS | JTAGTDIS1 | JTAGTCKS1 |
| | | Type | rw | r | | rw | | rw | rw | rw |
| $BA_H$ | **MODPISEL2** **Reset: $00_H$** Peripheral Input Select Register 2 | Bit Field | 0 | | | | T21IS | T2IS | T1IS | T0IS |
| | | Type | r | | | | rw | rw | rw | rw |
| $BB_H$ | **PMCON2** **Reset: $00_H$** Power Mode Control Register 2 | Bit Field | 0 | | | | | | UART1_DIS | T21_DIS |
| | | Type | r | | | | | | rw | rw |
| $BD_H$ | **MODSUSP** **Reset: $01_H$** Module Suspend Control Register | Bit Field | 0 | | | T21SUSP | T2SUSP | T13SUSP | T12SUSP | WDTSUSP |
| | | Type | r | | | rw | rw | rw | rw | rw |

### 3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 9 WDT Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| $BB_H$ | **WDTCON** **Reset: $00_H$** Watchdog Timer Control Register | Bit Field | 0 | | WINBEN | WDTPR | 0 | WDTEN | WDTRS | WDTIN |
| | | Type | r | | rw | rh | r | rw | rwh | rw |
| $BC_H$ | **WDTREL** **Reset: $00_H$** Watchdog Timer Reload Register | Bit Field | WDTREL | | | | | | | |
| | | Type | rw | | | | | | | |
| $BD_H$ | **WDTWINB** **Reset: $00_H$** Watchdog Window-Boundary Count Register | Bit Field | WDTWINB | | | | | | | |
| | | Type | rw | | | | | | | |

**Table 11 ADC Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $CD_H$ | **ADC_LCBR Reset: $B7_H$** Limit Check Boundary Register | Bit Field | BOUND1 | | | | BOUND0 | | | |
| | | Type | rw | | | | rw | | | |
| $CE_H$ | **ADC_INPCR0 Reset: $00_H$** Input Class 0 Register | Bit Field | STC | | | | | | | |
| | | Type | rw | | | | | | | |
| $CF_H$ | **ADC_ETRCR Reset: $00_H$** External Trigger Control Register | Bit Field | SYNEN1 | SYNEN0 | ETRSEL1 | | | ETRSEL0 | | |
| | | Type | rw | rw | rw | | | rw | | |
| RMAP = 0, PAGE 1 | | | | | | | | | | |
| $CA_H$ | **ADC_CHCTR0 Reset: $00_H$** Channel Control Register 0 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $CB_H$ | **ADC_CHCTR1 Reset: $00_H$** Channel Control Register 1 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $CC_H$ | **ADC_CHCTR2 Reset: $00_H$** Channel Control Register 2 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $CD_H$ | **ADC_CHCTR3 Reset: $00_H$** Channel Control Register 3 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $CE_H$ | **ADC_CHCTR4 Reset: $00_H$** Channel Control Register 4 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $CF_H$ | **ADC_CHCTR5 Reset: $00_H$** Channel Control Register 5 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $D2_H$ | **ADC_CHCTR6 Reset: $00_H$** Channel Control Register 6 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| $D3_H$ | **ADC_CHCTR7 Reset: $00_H$** Channel Control Register 7 | Bit Field | 0 | LCC | | | 0 | | RESRSEL | |
| | | Type | r | rw | | | r | | rw | |
| RMAP = 0, PAGE 2 | | | | | | | | | | |
| $CA_H$ | **ADC_RESR0L Reset: $00_H$** Result Register 0 Low | Bit Field | RESULT | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CB_H$ | **ADC_RESR0H Reset: $00_H$** Result Register 0 High | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |
| $CC_H$ | **ADC_RESR1L Reset: $00_H$** Result Register 1 Low | Bit Field | RESULT | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CD_H$ | **ADC_RESR1H Reset: $00_H$** Result Register 1 High | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |
| $CE_H$ | **ADC_RESR2L Reset: $00_H$** Result Register 2 Low | Bit Field | RESULT | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |
| $CF_H$ | **ADC_RESR2H Reset: $00_H$** Result Register 2 High | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |
| $D2_H$ | **ADC_RESR3L Reset: $00_H$** Result Register 3 Low | Bit Field | RESULT | | 0 | VF | DRC | CHNR | | |
| | | Type | rh | | r | rh | rh | rh | | |

**Table 14 CCU6 Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $FE_H$ | **CCU6_CMPSTATL Reset: $00_H$** Compare State Register Low | Bit Field | 0 | CC63 ST | CC POS2 | CC POS1 | CC POS0 | CC62 ST | CC61 ST | CC60 ST |
| | | Type | r | rh | rh | rh | rh | rh | rh | rh |
| $FF_H$ | **CCU6_CMPSTATH Reset: $00_H$** Compare State Register High | Bit Field | T13IM | COUT 63PS | COUT 62PS | CC62 PS | COUT 61PS | CC61 PS | COUT 60PS | CC60 PS |
| | | Type | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

### 3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 15 UART1 Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| **$C8_H$** | **SCON Reset: $00_H$** Serial Channel Control Register | Bit Field | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| | | Type | rw | rw | rw | rw | rw | rwh | rwh | rwh |
| $C9_H$ | **SBUF Reset: $00_H$** Serial Data Buffer Register | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $CA_H$ | **BCON Reset: $00_H$** Baud Rate Control Register | Bit Field | 0 | | | | BRPRE | | | R |
| | | Type | r | | | | rw | | | rw |
| $CB_H$ | **BG Reset: $00_H$** Baud Rate Timer/Reload Register | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rwh | | | | | | | |
| $CC_H$ | **FDCON Reset: $00_H$** Fractional Divider Control Register | Bit Field | 0 | | | | | NDOV | FDM | FDEN |
| | | Type | r | | | | | rwh | rw | rw |
| $CD_H$ | **FDSTEP Reset: $00_H$** Fractional Divider Reload Register | Bit Field | STEP | | | | | | | |
| | | Type | rw | | | | | | | |
| $CE_H$ | **FDRES Reset: $00_H$** Fractional Divider Result Register | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |

### 3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 21**.

**Table 21 Priority Structure within Interrupt Level**

| Source | Level |
|---|---|
| Non-Maskable Interrupt (NMI) | (highest) |
| External Interrupt 0 | 1 |
| Timer 0 Interrupt | 2 |
| External Interrupt 1 | 3 |
| Timer 1 Interrupt | 4 |
| UART Interrupt | 5 |
| Timer 2,UART Normal Divider Overflow, MultiCAN, LIN Interrupt | 6 |
| ADC, MultiCAN Interrupt | 7 |
| SSC Interrupt | 8 |
| External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt | 9 |
| External Interrupt [6:3], MultiCAN Interrupt | 10 |
| CCU6 Interrupt Node Pointer 0, MultiCAN interrupt | 11 |
| CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt | 12 |
| CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt | 13 |
| CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt | 14 |

## 3.5 Parallel Ports

The XC886 has 34 port pins organized into five parallel ports, Port 0 (P0) to Port 4 (P4), while the XC888 has 48 port pins organized into six parallel ports, Port 0 (P0) to Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. Ports P0, P1, P3, P4 and P5 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. Port P2 is an input-only port, providing general purpose input functions, alternate input functions for the on-chip peripherals, and also analog inputs for the Analog-to-Digital Converter (ADC).

**Bidirectional Port Features**

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

**Input Port Features**

- Configurable input driver
- Configurable pull-up/pull-down devices
- Receive of data through digital input (general purpose input)
- Alternate input for on-chip peripherals
- Analog input for ADC module

**Figure 19** shows the structure of a bidirectional port pin.

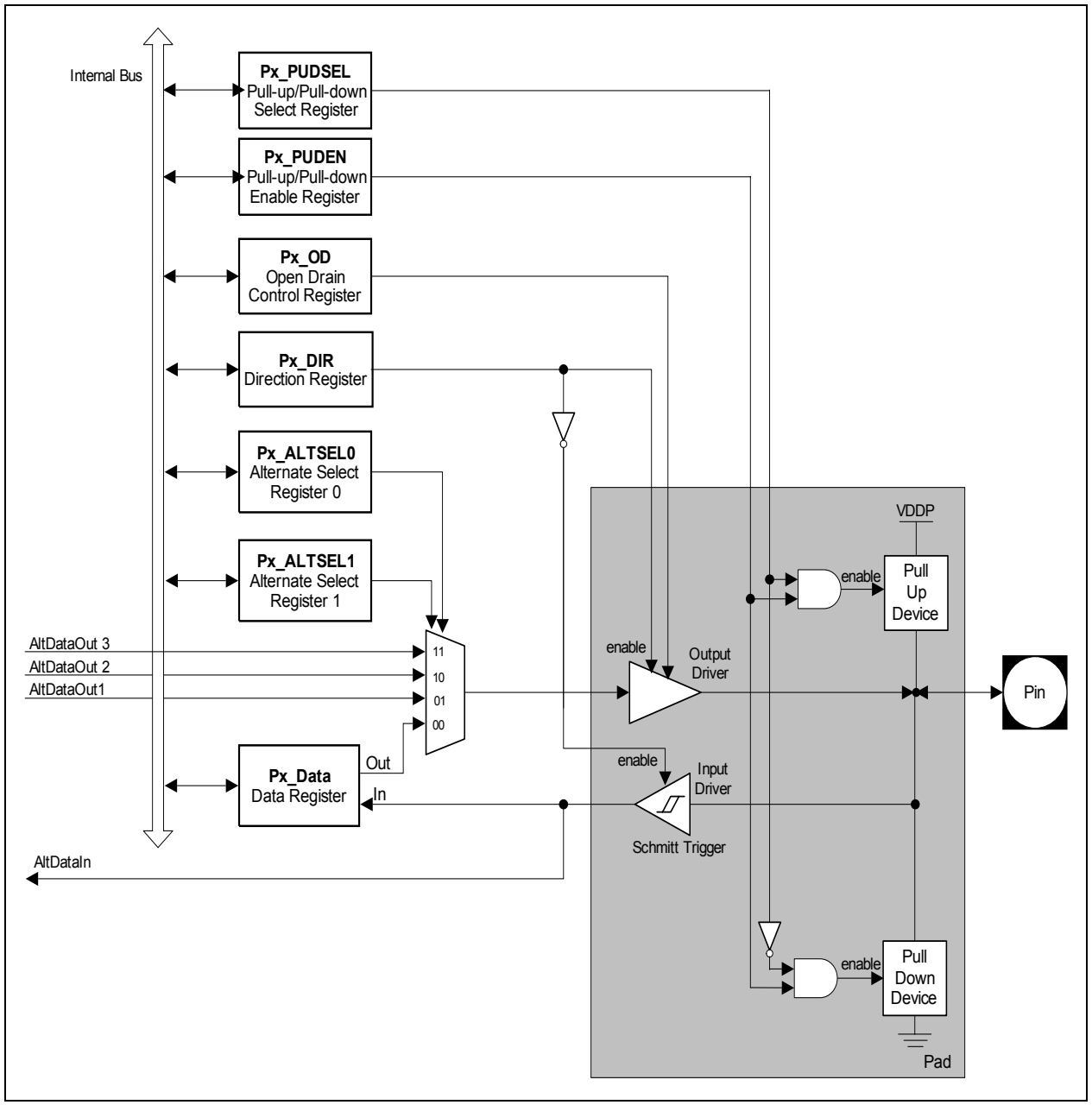


**Figure 19 General Structure of Bidirectional Port**

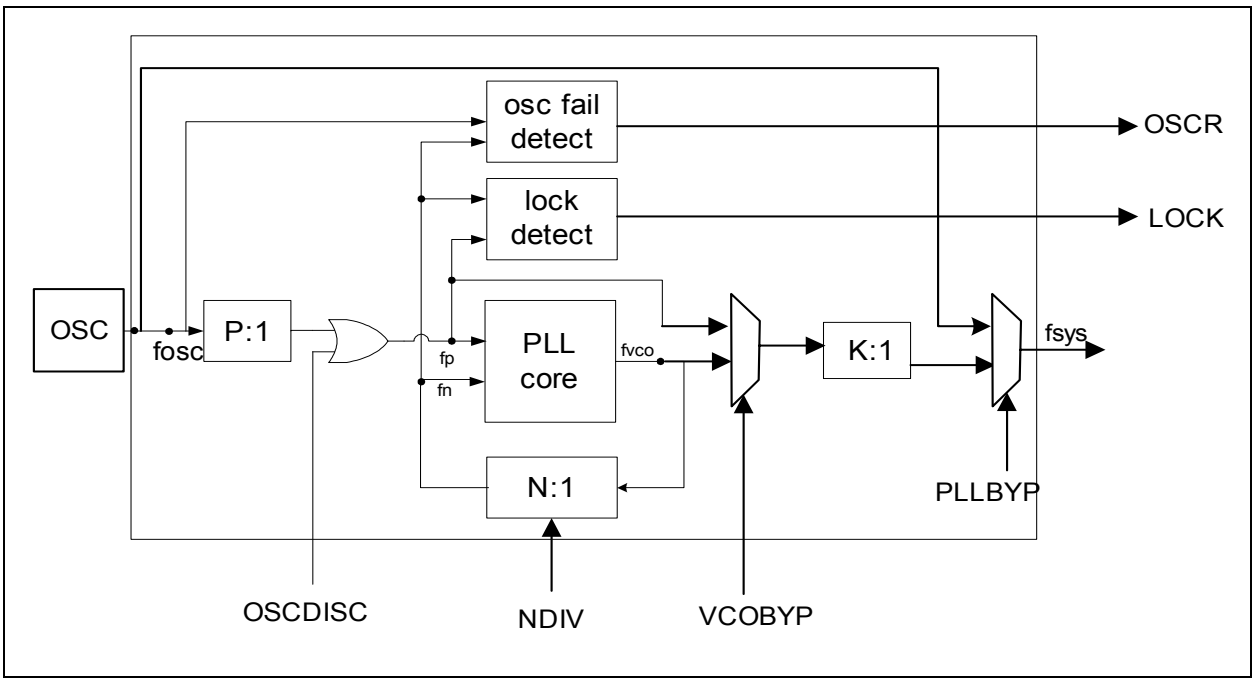


**Figure 24 CGU Block Diagram**

### PLL Base Mode

When the oscillator is disconnected from the PLL, the system clock is derived from the VCO base (free running) frequency clock (**Table 25**) divided by the K factor.

$$f_{SYS} = f_{VCObase} \times \frac{1}{K} \tag{3.1}$$

### Prescaler Mode (VCO Bypass Operation)

In VCO bypass operation, the system clock is derived from the oscillator clock, divided by the P and K factors.

$$f_{SYS} = f_{OSC} \times \frac{1}{P \times K} \tag{3.2}$$

### PLL Mode

The system clock is derived from the oscillator clock, multiplied by the N factor, and divided by the P and K factors. Both VCO bypass and PLL bypass must be inactive for this PLL mode. The PLL mode is used during normal system operation.

$$f_{SYS} = f_{OSC} \times \frac{N}{P \times K} \quad (3.3)$$

### System Frequency Selection

For the XC886/888, the value of P is fixed to 1. In order to obtain the required fsys, the value of N and K can be selected by bits NDIV and KDIV respectively for different oscillator inputs. The output frequency must always be configured for 96 MHz. **Table 24** provides examples on how $f_{sys}$ = 96 MHz can be obtained for the different oscillator sources.

**Table 24 System frequency ($f_{sys}$ = 96 MHz)**

| Oscillator | Fosc | N | P | K | Fsys |
|---|---|---|---|---|---|
| On-chip | 9.6 MHz | 20 | 1 | 2 | 96 MHz |
| External | 8 MHz | 24 | 1 | 2 | 96 MHz |
| | 6 MHz | 32 | 1 | 2 | 96 MHz |
| | 4 MHz | 48 | 1 | 2 | 96 MHz |

### 3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock, $f_{sys}$. During normal system operation, the typical frequencies of the different modules are as follow:

- CPU clock: CCLK, SCLK = 24 MHz
- Fast clock (used by MultiCAN): FCLK = 24 or 48 MHz
- Peripheral clock: PCLK = 24 MHz
- Flash Interface clock: CCLK2 = 48 MHz and CCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 26** shows the clock distribution of the XC886/888.

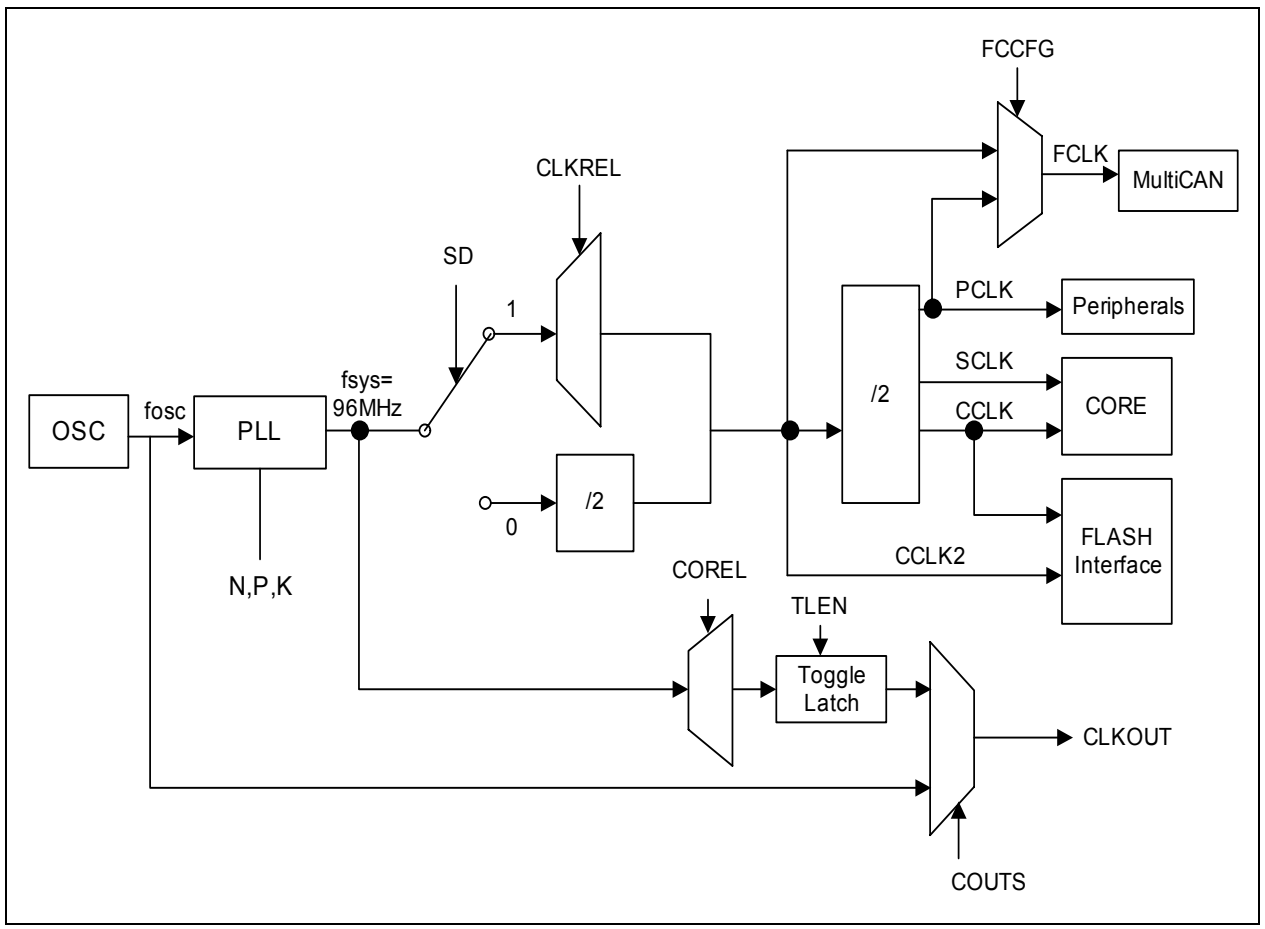


**Figure 26 Clock Generation from $f_{sys}$**

For power saving purposes, the clocks may be disabled or slowed down according to Table 26.

**Table 26 System frequency ($f_{sys}$ = 96 MHz)**

| Power Saving Mode | Action |
|---|---|
| Idle | Clock to the CPU is disabled. |
| Slow-down | Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL. |
| Power-down | Oscillator and PLL are switched off. |

## 3.9 Power Saving Modes

The power saving modes of the XC886/888 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 27**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

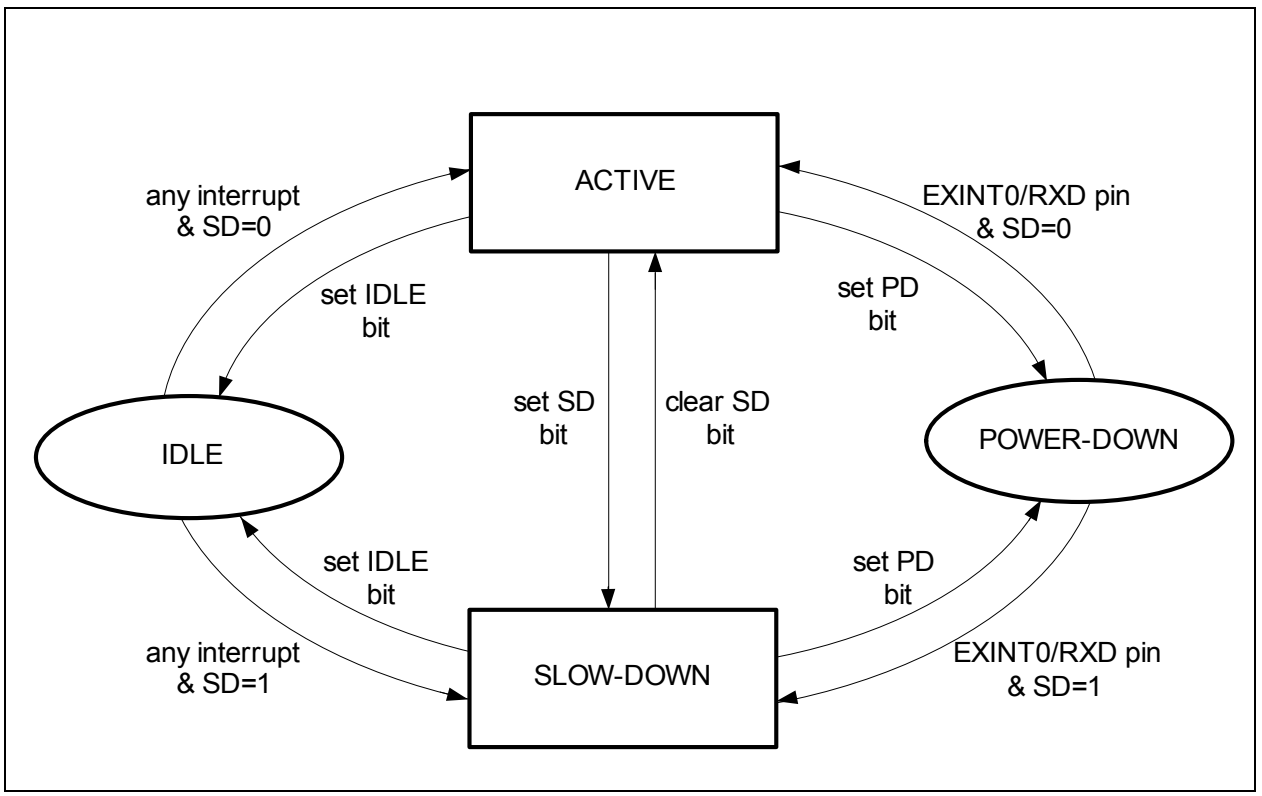


**Figure 27 Transition between Power Saving Modes**

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

# 4 Electrical Parameters

**Chapter 4** provides the characteristics of the electrical parameters which are implementation-specific for the XC886/888.

## 4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

### 4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC886/888 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC886/888 and must be regarded for a system design.
- **SR**
  These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC886/888 is designed in.

**Table 38 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 120 | mA | [3] |
| **$V_{DDP}$ = 3.3 V Range** | | | | | | |
| Output low voltage | $V_{OL}$ | CC | – | 1.0 | V | $I_{OL}$ = 8 mA |
| | | | – | 0.4 | V | $I_{OL}$ = 2.5 mA |
| Output high voltage | $V_{OH}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -8 mA |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -2.5 mA |
| Input low voltage on port pins (all except P0.0 & P0.1) | $V_{ILP}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on P0.0 & P0.1 | $V_{ILP0}$ | SR | -0.2 | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on RESET pin | $V_{ILR}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on TMS pin | $V_{ILT}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on port pins (all except P0.0 & P0.1) | $V_{IHP}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on P0.0 & P0.1 | $V_{IHP0}$ | SR | 0.7 × $V_{DDP}$ | $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on RESET pin | $V_{IHR}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on TMS pin | $V_{IHT}$ | SR | 0.75 × $V_{DDP}$ | – | V | CMOS Mode |
| Input Hysteresis | $HYS$ | CC | 0.03 × $V_{DDP}$ | – | V | CMOS Mode[1] |
| Input Hysteresis on XTAL1 | $HYSX$ | CC | 0.07 × $V_{DDC}$ | – | V | [1] |
| Input low voltage at XTAL1 | $V_{ILX}$ | SR | $V_{SS}$ - 0.5 | 0.3 × $V_{DDC}$ | V | |

**Table 38 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| Input high voltage at XTAL1 | $V_{IHX}$ | SR | 0.7 × $V_{DDC}$ | $V_{DDC}$ + 0.5 | V | |
| Pull-up current | $I_{PU}$ | SR | – | -5 | µA | $V_{IHP,min}$ |
| | | | -50 | – | µA | $V_{ILP,max}$ |
| Pull-down current | $I_{PD}$ | SR | – | 5 | µA | $V_{ILP,max}$ |
| | | | 50 | – | µA | $V_{IHP,min}$ |
| Input leakage current | $I_{OZ1}$ | CC | -1 | 1 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$ [2] |
| Input current at XTAL1 | $I_{ILX}$ | CC | - 10 | 10 | µA | |
| Overload current on any pin | $I_{OV}$ | SR | -5 | 5 | mA | |
| Absolute sum of overload currents | $\Sigma\|I_{OV}\|$ | SR | – | 25 | mA | [3] |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [4] |
| Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$) | $I_M$ SR | SR | – | 15 | mA | |
| Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$) | $\Sigma\|I_M\|$ | SR | – | 90 | mA | |
| Maximum current into $V_{DDP}$ | $I_{MVDDP}$ | SR | – | 120 | mA | [3] |
| Maximum current out of $V_{SS}$ | $I_{MVSS}$ | SR | – | 120 | mA | [3] |

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current ($I_{INJ}$) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when $V_{DDP}$ is powered off.

**Table 40 ADC Characteristics (Operating Conditions apply; $V_{DDP}$ = 5V Range)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions/ Remarks |
|---|---|---|---|---|---|---|---|
| | | | min. | typ . | max. | | |
| Overload current coupling factor for digital I/O pins | $K_{OVD}$ | CC | – | – | 5.0 x $10^{-3}$ | – | $I_{OV} > 0$ 1)3) |
| | | | – | – | 1.0 x $10^{-2}$ | – | $I_{OV} < 0$ 1)3) |
| Switched capacitance at the reference voltage input | $C_{AREFSW}$ | CC | – | 10 | 20 | pF | 1)4) |
| Switched capacitance at the analog voltage inputs | $C_{AINSW}$ | CC | – | 5 | 7 | pF | 1)5) |
| Input resistance of the reference input | $R_{AREF}$ | CC | – | 1 | 2 | kΩ | 1) |
| Input resistance of the selected analog channel | $R_{AIN}$ | CC | – | 1 | 1.5 | kΩ | 1) |

1) Not subjected to production test, verified by design/characterization

2) TUE is tested at $V_{AREF}$ = 5.0 V, $V_{AGND}$ = 0 V, $V_{DDP}$ = 5.0 V.

3) An overload current ($I_{OV}$) through a pin injects a certain error current ($I_{INJ}$) into the adjacent pins. This error current adds to the respective pin's leakage current ($I_{OZ}$). The amount of error current depends on the overload current and is defined by the overload coupling factor $K_{OV}$. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it. The total current through a pin is $|I_{TOT}| = |I_{OZ1}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

4) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.

5) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than $V_{AREF}/2$.

**Table 50 JTAG Timing (Operating Conditions apply; CL = 50 pF)** (cont'd)

| Parameter | Symbol | | Limits | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min | max | | |
| TDO high impedance to valid output from TCK | $t_4$ | CC | - | 27 | ns | 5V Device[1)] |
| | | | - | 36 | ns | 3.3V Device[1)] |
| TDO valid output to high impedance from TCK | $t_5$ | CC | - | 22 | ns | 5V Device[1)] |
| | | | - | 28 | ns | 3.3V Device[1)] |

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

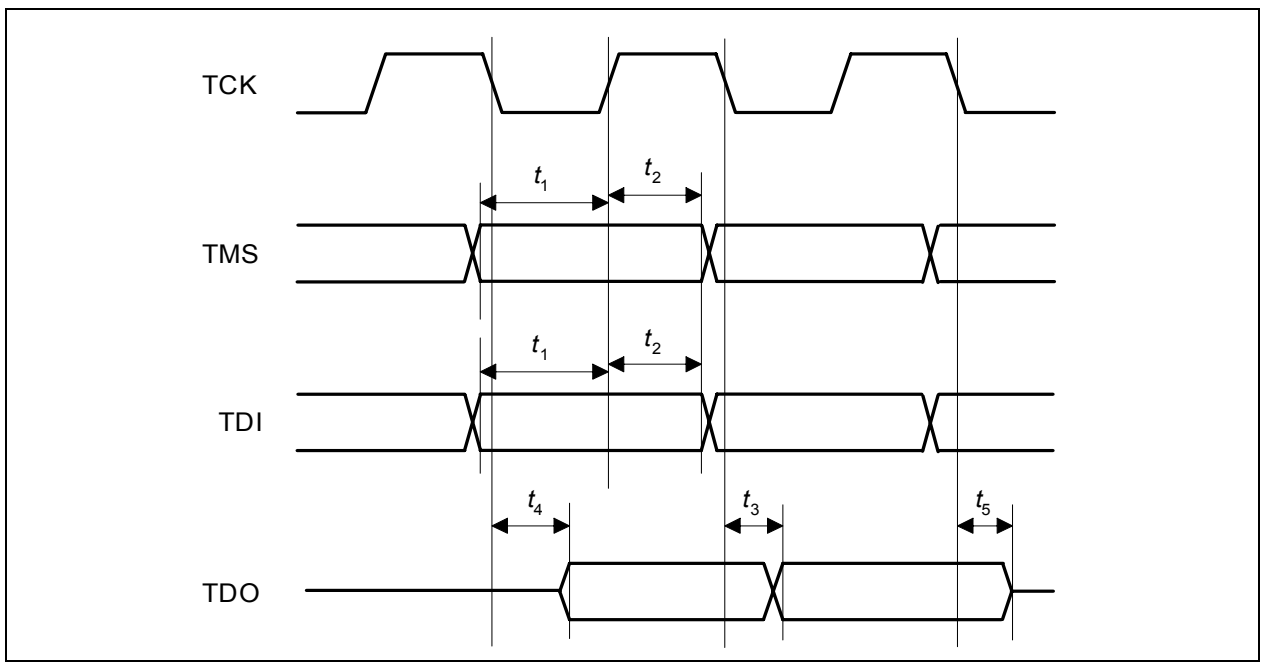


**Figure 47 JTAG Timing**

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