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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XE

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886clm-6ffi-5v-ac

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Summary of Features

Table 2 Device Frome (cont d)	Table 2	Device Profile (cont'd)
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Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp- erature (°C)	Quality Profile
SAK-XC886*/888*-8FFA 3V3	Flash	32	3.3	-40 to 125	Automotive
SAK-XC886*/888*-6FFA 3V3	Flash	24	3.3	-40 to 125	Automotive
SAF-XC886*/888*-8FFA 3V3	Flash	32	3.3	-40 to 85	Automotive
SAF-XC886*/888*-6FFA 3V3	Flash	24	3.3	-40 to 85	Automotive
SAF-XC886*/888*-8FFI 3V3	Flash	32	3.3	-40 to 85	Industrial
SAF-XC886*/888*-6FFI 3V3	Flash	24	3.3	-40 to 85	Industrial

- Note: The asterisk (*) above denotes the device configuration letters from **Table 1**. Corresponding ROM derivatives will be available on request.
- Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC886/888 throughout this document.

Ordering Information

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC886/888, please refer to your responsible sales representative or your local distributor.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.



General Device Information

2.2 Logic Symbol

The logic symbols of the XC886/888 are shown in Figure 3.



Figure 3 XC886/888 Logic Symbol



XC886/888CLM

General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function	
P3		I/O		Port 3 Port 3 is an 8 I/O port. It ca for CCU6, U/	B-bit bidirectional general purpose on be used as alternate functions ART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CC61_2 COUT60_0	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare
				TXD1_1	UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 TXDC1_1	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 RXDC0_1 T2EX1_0	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 EXF21_0 TXDC0_1	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	CTRAP 0	CCU6 Trap Input

Table 3Pin Definitions and Functions (cont'd)



3 Functional Description

Chapter 3 provides an overview of the XC886/888 functional description.

3.1 **Processor Architecture**

The XC886/888 is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC886/888 CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. Access to the Flash memory, however, requires an additional wait state (one machine cycle). The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC886/888 CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 6 shows the CPU functional blocks.



Figure 6 CPU Block Diagram



Table 11ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
cc ^H	ADC_CHINSR Reset: 00 _H Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Туре	w	w	w	w	w	w	w	w
CD _H	ADC_CHINPR Reset: 00 _H Channel Interrupt Node Pointer	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
	Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
CeH	ADC_EVINFR Reset: 00 _H Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4	(0	EVINF 1	EVINF 0
		Туре	rh	rh	rh	rh		r	rh	rh
CF _H	ADC_EVINCR Reset: 00 _H Event Interrupt Clear Flag	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4	(0	EVINC 1	EVINC 0
	Register	Туре	w	w	w	w		r v		w
D2 _H	ADC_EVINSR Reset: 00 _H Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	(D	EVINS 1	EVINS 0
		Туре	w	w	w	w		r	w	w
D3 _H	ADC_EVINPR Reset: 00 _H Event Interrupt Node Pointer	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4	0 EVINP EVI 1 (EVINP 0	
	Register		rw	rw	rw	rw		r	rw	rw
RMAP =	= 0, PAGE 6	_	-							
са _Н	CA _H ADC_CRCR1 Reset: 00 _H		CH7	CH6	CH5	CH4	0			
	Register 1	Туре	rwh	rwh	rwh	rwh		I	r	
св _Н	ADC_CRPR1 Reset: 00 _H	Bit Field	CHP7	CHP6	CHP5	CHP4	0 r			
	Register 1	Туре	rwh	rwh	rwh	rwh				
cc ^H	ADC_CRMR1 Reset: 00 _H Conversion Request Mode	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
	Register 1	Туре	r	w	w	rw	rw	rw	r	rw
CDH	ADC_QMR0 Reset: 00 _H Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Туре	w	w	w	w	r	rw	r	rw
CEH	ADC_QSR0 Reset: 20 _H Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	0 FILL		LL	
			r	r	rh	rh		r	r	h
CFH	ADC_Q0R0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHN	२
		Туре	rh	rh	rh	rh	r		rh	
D2 _H	ADC_QBUR0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHN	२
	Queue Dackup Register U	Туре	rh	rh	rh	rh	r		rh	
D2 _H	ADC_QINR0 Reset: 00 _H	Bit Field	EXTR	ENSI	RF	()	F	REQCHN	ર
		Туре	w	w	w		r		w	



3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC886/888 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to **Figure 17** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.



Figure 13 Non-Maskable Interrupt Request Sources





Figure 18 Interrupt Request Sources (Part 5)







Figure 20 General Structure of Input Port



 Table 25 shows the VCO range for the XC886/888.

Table 25 VCC Ralige	Table	25	VCO	Range
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<i>f</i> _{VCOmin}	f _{vcomax}	$f_{\sf VCOFREEmin}$	<i>f</i> _{VCOFREEmax}	Unit
150	200	20	80	MHz
100	150	10	80	MHz

3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 4 MHz to 12 MHz. Additionally, it is necessary to have two load capacitances C_{X1} and C_{X2} , and depending on the crystal type, a series resistor R_{X2} , to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal vendor. The C_{X1} and C_{X2} values shown in **Figure 25** can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor. **Figure 25** shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.



3.9 Power Saving Modes

The power saving modes of the XC886/888 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 27**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode



Figure 27 Transition between Power Saving Modes



needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data. The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

- STEP 4: Enter for Master Request Frame or for Slave Response Frame
- Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.



3.16 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Features

- Master and slave mode operation
 - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
 - Programmable number of data bits: 2 to 8 bits
 - Programmable shift direction: LSB or MSB shift first
 - Programmable clock polarity: idle low or high state for the shift clock
 - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 32 shows the block diagram of the SSC.



GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.



Figure 35 ADC Clocking Scheme

For module clock f_{ADC} = 24 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 34**.

Table 34	f _{ADCI} Frequency Selection
----------	---------------------------------------

$\frac{f_{ADC}}{Module Clock f_{ADC}}$	СТС	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00 _B	÷ 2	12 MHz (N.A)
	01 _B	÷ 3	8 MHz
	10 _B	÷ 4	6 MHz
	11 _B (default)	÷ 32	750 kHz

As $f_{\rm ADCI}$ cannot exceed 10 MHz, bit field CTC should not be set to $00_{\rm B}$ when $f_{\rm ADC}$ is 24 MHz. During slow-down mode where $f_{\rm ADC}$ may be reduced to 12 MHz, 6 MHz etc., CTC can be set to $00_{\rm B}$ as long as the divided analog clock $f_{\rm ADCI}$ does not exceed 10 MHz.



Table 36Chip Identification Number (cont'd)

Product Variant	Chip	Identification Nur	nber
	AA-Step	AB-Step	AC-Step
XC886-6FFA 3V3	-	095D1562 _H	0B5D1562 _H
XC888-6FFA 3V3	-	095D1563 _H	0B5D1563 _H
XC886CLM-8FFA 5V	-	09900102 _H	0B900102 _H
XC888CLM-8FFA 5V	-	09900103 _H	0B900103 _H
XC886LM-8FFA 5V	-	09900122 _H	0B900122 _H
XC888LM-8FFA 5V	-	09900123 _H	0B900123 _H
XC886CLM-6FFA 5V	-	09951502 _H	0B951502 _H
XC888CLM-6FFA 5V	-	09951503 _н	0B951503 _Н
XC886LM-6FFA 5V	-	09951522 _н	0B951522 _H
XC888LM-6FFA 5V	-	09951523 _н	0B951523 _Н
XC886CM-8FFA 5V	-	09980102 _H	0B980102 _H
XC888CM-8FFA 5V	-	09980103 _H	0B980103 _H
XC886C-8FFA 5V	-	09980142 _H	0B980142 _H
XC888C-8FFA 5V	-	09980143 _H	0B980143 _H
XC886-8FFA 5V	-	09980162 _H	0B980162 _H
XC888-8FFA 5V	-	09980163 _н	0B980163 _H
XC886CM-6FFA 5V	-	099D1502 _H	0B9D1502 _H
XC888CM-6FFA 5V	-	099D1503 _H	0B9D1503 _H
XC886C-6FFA 5V	-	099D1542 _H	0B9D1542 _H
XC888C-6FFA 5V	-	099D1543 _H	0B9D1543 _H
XC886-6FFA 5V	-	099D1562 _H	0B9D1562 _H
XC888-6FFA 5V	-	099D1563 _H	0B9D1563 _H
ROM Devices			
XC886CLM-8RFA 3V3	22400502 _H	-	-
XC888CLM-8RFA 3V3	22400503 _H	-	-
XC886LM-8RFA 3V3	22400522 _H	-	-
XC888LM-8RFA 3V3	22400523 _H	-	-
XC886CLM-6RFA 3V3	22411502 _H	-	-
XC888CLM-6RFA 3V3	22411503 _H	-	-



Table 36Chip Identification Number (cont'd)

Product Variant	C	hip Identification	Number
	AA-Step	AB-Step	AC-Step
XC888CM-6RFA 5V	22891503 _H	-	-
XC886C-6RFA 5V	22891542 _H	-	-
XC888C-6RFA 5V	22891543 _H	-	-
XC886-6RFA 5V	22891562 _H	-	-
XC888-6RFA 5V	22891563 _H	-	-



Electrical Parameters

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Characteristics

Table 38 provides the characteristics of the input/output pins of the XC886/888.

Table 38	Input/Output Characteristics	(Operating	Conditions	apply)
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Parameter	Symbol		Limit Values		Unit	Test Conditions	
			min.	max.			
V _{DDP} = 5 V Range							
Output low voltage	V _{OL}	CC	-	1.0	V	I _{OL} = 15 mA	
			-	1.0	V	I_{OL} = 5 mA, current into all pins > 60 mA	
			-	0.4	V	$I_{\rm OL}$ = 5 mA, current into all pins \leq 60 mA	
Output high voltage	V _{OH}	CC	V _{DDP} - 1.0	-	V	I _{ОН} = -15 mA	
			V _{DDP} - 1.0	-	V	$I_{\rm OH}$ = -5 mA, current from all pins > 60 mA	
			V _{DDP} - 0.4	-	V	$I_{\rm OH}$ = -5 mA, current from all pins ≤ 60 mA	
Input low voltage on port pins (all except P0.0 & P0.1)	V _{ILP}	SR	-	$0.3 \times V_{ m DDP}$	V	CMOS Mode	
Input low voltage on P0.0 & P0.1	V _{ILP0}	SR	-0.2	$0.3 \times V_{\text{DDP}}$	V	CMOS Mode	
Input low voltage on RESET pin	V _{ILR}	SR	-	$0.3 \times V_{\text{DDP}}$	V	CMOS Mode	
Input low voltage on TMS pin	V _{ILT}	SR	-	$0.3 \times V_{ m DDP}$	V	CMOS Mode	
Input high voltage on port pins (all except P0.0 & P0.1)	V _{IHP}	SR	$0.7 \times V_{\text{DDP}}$	_	V	CMOS Mode	
Input high voltage on P0.0 & P0.1	V _{IHP0}	SR	$0.7 \times V_{\text{DDP}}$	V _{DDP}	V	CMOS Mode	



Electrical Parameters

Table 43Power Supply Current Parameters (Operating Conditions apply;
 V_{DDP} = 3.3V range)

Parameter	Symbol	Limit	Values	Unit	Test Condition
		typ. ¹⁾	max. ²⁾		
V_{DDP} = 3.3V Range					
Active Mode	I _{DDP}	25.6	31.0	mA	Flash Device ³⁾
		23.4	28.6	mA	ROM Device ³⁾
Idle Mode	I _{DDP}	19.9	24.7	mA	Flash Device ⁴⁾
		17.5	20.7	mA	ROM Device ⁴⁾
Active Mode with slow-down	I _{DDP}	13.3	16.2	mA	Flash Device ⁵⁾
enabled		11.5	13.7	mA	ROM Device ⁵⁾
Idle Mode with slow-down	I _{DDP}	11.1	14.4	mA	Flash Device ⁶⁾
enabled		9.3	11.4	mA	ROM Device ⁶⁾

1) The typical I_{DDP} values are periodically measured at T_{A} = + 25 °C and V_{DDP} = 3.3 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_{A} = + 125 °C and V_{DDP} = 3.6 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to 1001_B), RESET = V_{DDP} , no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, RESET = V_{DDP} , no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to 0110_B, RESET = V_{DDP} , no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to 0110_B,, RESET = V_{DDP} , no load on ports.



XC886/888CLM

Electrical Parameters



Figure 44 Power-on Reset Timing



Electrical Parameters

Table 50 JTAG Timing (O	nditions a	litions apply; CL = 50 pF) (cont'd)				
Parameter	Symbol		Limits		Unit	Test
			min	max		Conditions
TDO high impedance to valid output from TCK	t ₄	CC	-	27	ns	5V Device ¹⁾
			-	36	ns	3.3V Device ¹⁾
TDO valid output to high impedance from TCK	<i>t</i> ₅	CC	-	22	ns	5V Device ¹⁾
			-	28	ns	3.3V Device ¹⁾

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.



