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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, LINbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886clm-8ffi-5v-ac

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



General Device Information

2.3 Pin Configuration

The pin configuration of the XC886, which is based on the PG-TQFP-48 package, is shown in **Figure 4**, while that of the XC888, which is based on the PG-TQFP-64 package, is shown in **Figure 5**.



Figure 4 XC886 Pin Configuration, PG-TQFP-48 Package (top view)



XC886/888CLM

General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function	
P3		I/O		Port 3 Port 3 is an 8 I/O port. It ca for CCU6, U/	B-bit bidirectional general purpose on be used as alternate functions ART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CC61_2 COUT60_0	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare
				TXD1_1	UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 TXDC1_1	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 RXDC0_1 T2EX1_0	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 EXF21_0 TXDC0_1	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	CTRAP 0	CCU6 Trap Input

Table 3Pin Definitions and Functions (cont'd)



3.2 Memory Organization

The XC886/888 CPU operates in the following five address spaces:

- 12 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 1.5 Kbytes of XRAM memory (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 24/32 Kbytes of Flash program memory (Flash devices); or 24/32 Kbytes of ROM program memory, with additional 4 Kbytes of Flash (ROM devices)

Figure 7 illustrates the memory address spaces of the 32-Kbyte Flash devices. For the 24-Kbyte Flash devices, the shaded banks are not available.



Figure 7 Memory Map of XC886/888 Flash Device

For both 24-Kbyte and 32-Kbyte ROM devices, the last four bytes of the ROM from $7FFC_{H}$ to $7FFF_{H}$ are reserved for the ROM signature and cannot be used to store user



3.2.4 XC886/888 Register Overview

The SFRs of the XC886/888 are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in **Chapter 3.2.4.1** to **Chapter 3.2.4.14**.

Note: The addresses of the bitaddressable SFRs appear in bold typeface.

3.2.4.1 CPU Registers

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	0 or 1									
81 _H	SP Reset: 07 _H	Bit Field				S	P			
	Stack Pointer Register	Туре	rw							
82 _H	DPL Reset: 00 _H	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
	Data Pointer Register Low	Туре	rw	rw	rw	rw	rw	rw	rw	rw
83 _H	DPH Reset: 00 _H	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
	Data Pointer Register High	Туре	rw	rw	rw	rw	rw	rw	rw	rw
87 _H	PCON Reset: 00 _H	Bit Field	SMOD		0		GF1	GF0	0	IDLE
	Power Control Register	Туре	rw		r		rw	rw	r	rw
⁸⁸ H	TCON Reset: 00 _H	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
	Timer Control Register	Туре	rwh	rw	rwh	rw	rwh	rw	rwh	rw
89 _H	89 _H TMOD Reset: 00_H Timer Mode Register		GATE 1	T1S	T1M		GATE 0	TOS	том	
		Туре	rw	rw	r	rw		rw	r	w
8A _H	TL0 Reset: 00 _H	Bit Field		•		V	AL			
	Timer 0 Register Low	Туре	rwh							
8B _H	TL1 Reset: 00 _H	Bit Field	JAV VAL							
	Timer 1 Register Low	Туре				rv	vh			
8C _H	THO Reset: 00 _H	Bit Field				V	AL			
	Timer U Register High	Туре	rwh							
8D _H	TH1 Reset: 00 _H	Bit Field				V	AL			
	limer 1 Register High	Туре				rv	vh			
98 _H	SCON Reset: 00 _H	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
	Serial Channel Control Register	Туре	rw	rw	rw	rw	rw	rwh	rwh	rwh
99 _H	SBUF Reset: 00 _H	Bit Field				V	AL			
	Serial Data Butter Register	Туре				rv	vh			
A2 _H	EO Reset: 00 _H Extended Operation Register	Bit Field		0		TRAP_ EN		0		DPSE L0
		Туре		r		rw		r		rw

Table 5 CPU Register Overview



3.2.4.8 Timer 2 Registers

The Timer 2 SFRs can be accessed in the standard memory area (RMAP = 0).

		1								1
Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	= 0									
с₀Н	T2_T2CONReset: 00Timer 2 Control Register	Bit Field	TF2	EXF2	(0	EXEN 2	TR2	C/T2	CP/ RL2
		Туре	rwh	rwh		r	rw	rwh	rw	rw
C1 _H	T2_T2MODReset: 00Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN		T2PRE		DCEN
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H T2_RC2L	T2_RC2L Reset: 00 _H	Bit Field				R	C2			
	Register Low	Туре	rwh							
C3 _H	T2_RC2H Reset: 00 _H	Bit Field	RC2							
	Register High	Туре	rwh							
C4 _H	T2_T2L Reset: 00 _H	Bit Field				T⊦	IL2			
	Timer 2 Register Low	Туре				rv	vh			
C5 _H	T2_T2H Reset: 00 _H	Bit Field	THL2							
	i imer 2 Register High	Туре				rv	vh			

Table 12T2 Register Overview

3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: : 1			•	•	•				
c₀ _H	T21_T2CONReset: 00HTimer 2 Control Register	Bit Field	TF2	EXF2	()	EXEN 2	TR2	C/T2	<u>CP/</u> RL2
		Туре	rwh	rwh		r	rw	rwh	rw	rw
C1 _H	T21_T2MODReset: 00Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN	T2PRE			DCEN
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
C2 _H	T21_RC2L Reset: 00 _H	Bit Field	RC2							
	Timer 2 Reload/Capture Register Low	Туре		rwh						
C3 _H	T21_RC2H Reset: 00 _H	Bit Field				R	C2			
	Timer 2 Reload/Capture Register High	Туре	rwh							
C4 _H	T21_T2L Reset: 00 _H	Bit Field	THL2							
	Timer 2 Register Low					rv	/h			



3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

∆ddr	Register Name	Bit	7	6	5	4	3	2	1	0
		ы	'	Ŭ	Ŭ	-	0	-	•	v
RMAP =	: 0									
А9 _Н	SSC_PISEL Reset: 00 _H	Bit Field			0			CIS	SIS	MIS
	Port Input Select Register	Туре			r			rw	rw	rw
AA _H	SSC_CONL Reset: 00 _H	Bit Field	LB	PO	PH	HB		В	М	
	Control Register Low Programming Mode	Туре	rw	rw	rw	rw	rw			
AA _H	SSC_CONL Reset: 00 _H	Bit Field		()			В	С	
	Control Register Low Operating Mode				r			r	h	
AB _H SSC_CONH Rese Control Register High Programming Mode	SSC_CONH Reset: 00 _H	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
	Control Register High Programming Mode	Туре	rw	rw	r	rw	rw	rw	rw	rw
ab _H	SSC_CONH Reset: 00 _H	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
	Control Register High Operating Mode	Туре	rw	rw	r	rh	rwh	rwh	rwh	rwh
ac _h	SSC_TBL Reset: 00 _H	Bit Field	TB_VALUE							
	I ransmitter Buffer Register Low	Туре	rw							
ad _H	SSC_RBL Reset: 00 _H	Bit Field				RB_V	ALUE			
	Receiver Buffer Register Low	Туре	rh							
AE _H	SSC_BRL Reset: 00 _H	Bit Field				BR_V	ALUE			
	Baud Rate Timer Reload Register Low	Туре				r	N			
af _h	SSC_BRH Reset: 00 _H	Bit Field				BR_V	ALUE			
	Register High	Туре				r	N			

Table 16 SSC Register Overview

3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 17	CAN R	egister	Overview
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Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	= 0	-								
D8 _H	08 _H ADCON Reset: 00 _H	Bit Field	V3	V2	V1	V0	AU	AUAD		RWEN
CAN Address/Data Co Register	CAN Address/Data Control Register	Туре	rw	rw	rw	rw	rw		rh	rw
D9 _H	ADL Reset: 00 _H	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2
	CAN Address Register Low	Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
da _h	ADH Reset: 00 _H CAN Address Register High	Bit Field	0				CA13	CA12	CA11	CA10
		Туре	r				rwh	rwh	rwh	rwh



3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC886/888 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to **Figure 17** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.



Figure 13 Non-Maskable Interrupt Request Sources





Figure 23 V_{DDP} , V_{DDC} and V_{RESET} during Power-on Reset

The second type of reset in XC886/888 is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin RESET is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.



PLL Mode

The system clock is derived from the oscillator clock, multiplied by the N factor, and divided by the P and K factors. Both VCO bypass and PLL bypass must be inactive for this PLL mode. The PLL mode is used during normal system operation.

$$f_{SYS} = f_{OSC} \times \frac{N}{P \times K}$$

(3.3)

System Frequency Selection

For the XC886/888, the value of P is fixed to 1. In order to obtain the required fsys, the value of N and K can be selected by bits NDIV and KDIV respectively for different oscillator inputs. The output frequency must always be configured for 96 MHz. Table 24 provides examples on how $f_{\rm sys}$ = 96 MHz can be obtained for the different oscillator sources.

Table 24	System frequency (<i>f</i> _{svs} = 96 MHz)
----------	--

Oscillator	Fosc	Ν	Ρ	κ	Fsys	
On-chip	9.6 MHz	20	1	2	96 MHz	
External	8 MHz	24	1	2	96 MHz	
	6 MHz	32	1	2	96 MHz	
	4 MHz	48	1	2	96 MHz	



3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC886/888 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC886/888 will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{\rm PCLK}/2$ or $f_{\rm PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 28** shows the block diagram of the WDT unit.



Figure 28 WDT Block Diagram



If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for $30_{\rm H}$ count, after which the system is reset (assert WDTRST).

The WDT has a "programmable window boundary" which disallows any refresh during the WDT's count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_{\rm H}$ to the value obtained from the concatenation of WDTWINB and $00_{\rm H}$.

After being serviced, the WDT continues counting up from the value ($\langle WDTREL \rangle * 2^8$). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{\rm PCLK}/2$ or $f_{\rm PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, $P_{\rm WDT}$, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

(3.4)

If the Window-Boundary Refresh feature of the WDT is enabled, the period $P_{\rm WDT}$ between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 29**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.





Figure 29 WDT Timing Diagram

Table 27 lists the possible watchdog time ranges that can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 27Watchdog Time Ranges

Reload value In WDTREL	Prescaler for f_{PCLK}	Prescaler for f_{PCLK}							
	2 (WDTIN = 0)	128 (WDTIN = 1)							
	24 MHz	24 MHz							
FF _H	21.3 μs	1.37 ms							
7F _H	2.75 ms	176 ms							
00 _H	5.46 ms	350 ms							



3.12 CORDIC Coprocessor

The CORDIC Coprocessor provides CPU with hardware support for the solving of circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions.

Features

- Modes of operation
 - Supports all CORDIC operating modes for solving circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions
 - Integrated look-up tables (LUTs) for all operating modes
- Circular vectoring mode: Extended support for values of initial X and Y data up to full range of [-2¹⁵,(2¹⁵-1)] for solving angle and magnitude
- Circular rotation mode: Extended support for values of initial Z data up to full range of $[-2^{15},(2^{15}-1)]$, representing angles in the range $[-\pi,((2^{15}-1)/2^{15})\pi]$ for solving trigonometry
- Implementation-dependent operational frequency of up to 80 MHz
- Gated clock input to support disabling of module
- 16-bit accessible data width
 - 24-bit kernel data width plus 2 overflow bits for X and Y each
 - 20-bit kernel data width plus 1 overflow bit for Z
 - With KEEP bit to retain the last value in the kernel register for a new calculation
- 16 iterations per calculation: Approximately 41 clock-cycles or less, from set of start (ST) bit to set of end-of-calculation flag, excluding time taken for write and read access of data bytes.
- Twos complement data processing
- Only exception: X result data with user selectable option for unsigned result
- X and Y data generally accepted as integer or rational number; X and Y must be of the same data form
- Entries of LUTs are 20-bit signed integers
 - Entries of atan and atanh LUTs are integer representations (S19) of angles with the scaling such that $[-2^{15},(2^{15}-1)]$ represents the range $[-\pi,((2^{15}-1)/2^{15})\pi]$
 - Accessible Z result data for circular and hyperbolic functions is integer in data form of S15
- Emulated LUT for linear function
 - Data form is 1 integer bit and 15-bit fractional part (1.15)
 - Accessible Z result data for linear function is rational number with fixed data form of S4.11 (signed 4Q16)
- Truncation Error
 - The result of a CORDIC calculation may return an approximation due to truncation of LSBs
 - Good accuracy of the CORDIC calculated result data, especially in circular mode
- Interrupt
 - On completion of a calculation



3.19 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Timer T12 Features

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- · Generation of center-aligned and edge-aligned PWM
- Supports single-shot mode
- Supports many interrupt request sources
- Hysteresis-like control mode

Timer T13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Supports single-shot mode

Additional Features

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- · Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The block diagram of the CCU6 module is shown in **Figure 33**.



3.21 Analog-to-Digital Converter

The XC886/888 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features

- Successive approximation
- 8-bit or 10-bit resolution (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- · Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- · Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- · Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register







3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC886/888 Flash devices are given in Table 35.

Device Type	Device Name	JTAG ID	
Flash	XC886/888*-8FF	1012 0083 _H	
	XC886/888*-6FF	1012 5083 _H	
ROM	XC886/888*-8RF	1013 C083 _H	
	XC886/888*-6RF	1013 D083 _H	

Table 35JTAG ID Summary

Note: The asterisk (*) above denotes all possible device configurations.

103



Electrical Parameters

4.2.2 Supply Threshold Characteristics

 Table 39 provides the characteristics of the supply threshold in the XC886/888.



Figure 38 Supply Threshold Parameters

Table 39	Supply Threshold Para	ameters (Operating Conditions ap	ply)
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Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
$V_{\rm DDC}$ prewarning voltage ¹⁾	V _{DDCPW}	CC	2.2	2.3	2.4	V
$V_{\rm DDC}$ brownout voltage in active mode ¹⁾	V _{DDCBO}	CC	2.0	2.1	2.2	V
RAM data retention voltage	V _{DDCRDR}	CC	0.9	1.0	1.1	V
$V_{\rm DDC}$ brownout voltage in power-down mode ²⁾	V _{DDCBOPD}	CC	1.3	1.5	1.7	V
$V_{\rm DDP}$ prewarning voltage ³⁾	V _{DDPPW}	CC	3.4	4.0	4.6	V
Power-on reset voltage ²⁾⁴⁾	V _{DDCPOR}	CC	1.3	1.5	1.7	V

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

 Detection is enabled for external power supply of 5.0V. Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 µs typically after the VDDC reaches the power-on reset voltage.



Electrical Parameters

4.2.4 **Power Supply Current**

 Table 41, Table 42, Table 43 and Table 44 provide the characteristics of the power supply current in the XC886/888.

Table 41Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit	Values	Unit	Test Condition	
		typ. ¹⁾	max. ²⁾			
V _{DDP} = 5V Range						
Active Mode	I _{DDP}	27.2	32.8	mA	Flash Device ³⁾	
		24.3	29.8	mA	ROM Device ³⁾	
Idle Mode	I _{DDP}	21.1	25.3	mA	Flash Device ⁴⁾	
		18.2	21.6	mA	ROM Device ⁴⁾	
Active Mode with slow-down	I _{DDP}	14.1	17.0	mA	Flash Device ⁵⁾	
enabled		11.9	14.3	mA	ROM Device ⁵⁾	
Idle Mode with slow-down	I _{DDP}	11.7	15.0	mA	Flash Device ⁶⁾	
enabled		9.7	11.9	mA	ROM Device ⁶⁾	

1) The typical I_{DDP} values are periodically measured at T_{A} = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_{A} = + 125 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to 1001_B), RESET = V_{DDP} , no load on ports.

4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, RESET = V_{DDP} , no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to 0110_B, RESET = V_{DDP} , no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to 0110_B, RESET = V_{DDP} , no load on ports.



Electrical Parameters

4.3.7 SSC Master Mode Timing

Table 51 provides the characteristics of the SSC timing in the XC886/888.

Table 51	SSC Master Mode Timing	(Operating Conditions	apply; $CL = 50 pF$)
	J		

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min. max.			
SCLK clock period	t ₀	CC	2*T _{SSC}	_	ns	1)2)
MTSR delay from SCLK	t ₁	CC	0	8	ns	2)
MRST setup to SCLK	<i>t</i> ₂	SR	24	-	ns	2)
MRST hold from SCLK	<i>t</i> ₃	SR	0	-	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 83.3$ ns. T_{CPU} is the CPU clock period.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.



Figure 52 SSC Master Mode Timing



Package and Quality Declaration

5.3 Quality Declaration

Table 2 shows the characteristics of the quality parameters in the XC886/888.

Table 2Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V _{HBM}	-	2000	V	Conforming to EIA/JESD22- A114-B ¹⁾
ESD susceptibility according to Charged Device Model (CDM) pins	V _{CDM}	-	500	V	Conforming to JESD22-C101-C ¹⁾

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.