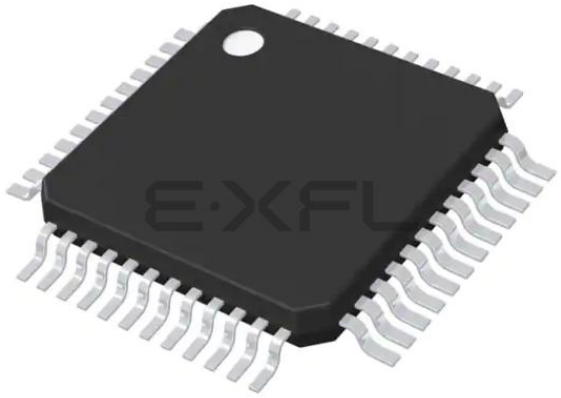
Infineon Technologies - SAK-XC886CM-6FFA 5V AC Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	CANbus, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc886cm-6ffa-5v-ac

2.2 Logic Symbol

The logic symbols of the XC886/888 are shown in **Figure 3**.

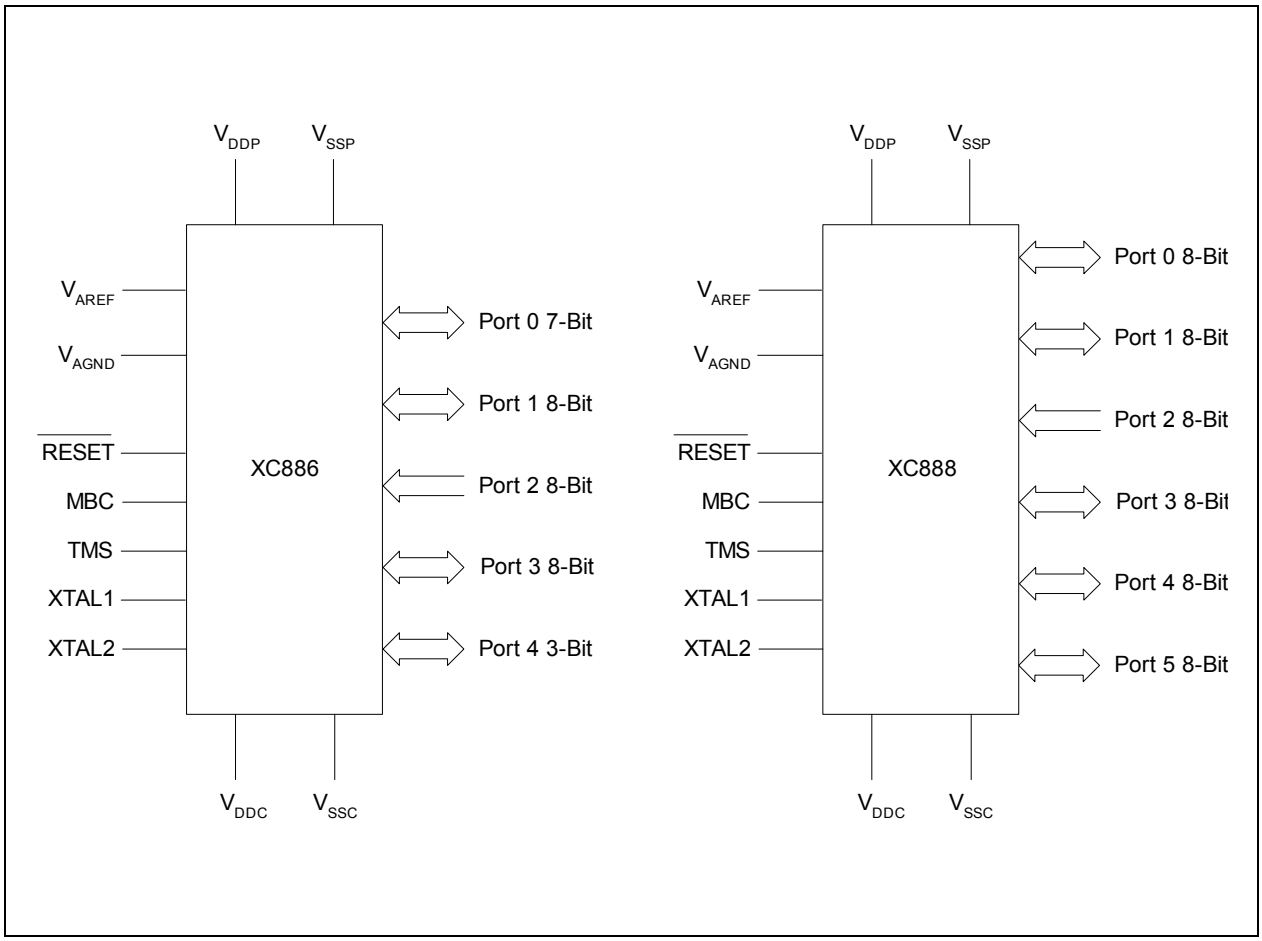


Figure 3 XC886/888 Logic Symbol

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P4		I/O		**Port 4** Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, Timer 21 and MultiCAN.	
P4.0	45/59		Hi-Z	RXDC0_3 CC60_1	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0
P4.1	46/60		Hi-Z	TXDC0_3 COUT60_1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0
P4.2	–/61		PU	EXINT6_1 T21_0	External Interrupt Input 6 Timer 21 Input
P4.3	32/40		Hi-Z	EXF21_1 COUT63_2	Timer 21 External Flag Output Output of Capture/Compare channel 3
P4.4	–/45		Hi-Z	CCPOS0_3 T0_0 CC61_4	CCU6 Hall Input 0 Timer 0 Input Output of Capture/Compare channel 1
P4.5	–/46		Hi-Z	CCPOS1_3 T1_0 COUT61_2	CCU6 Hall Input 1 Timer 1 Input Output of Capture/Compare channel 1
P4.6	–/47		Hi-Z	CCPOS2_3 T2_0 CC62_2	CCU6 Hall Input 2 Timer 2 Input Output of Capture/Compare channel 2
P4.7	–/48		Hi-Z	$\overline{\text{CTRAP}}$_3 COUT62_2	CCU6 Trap Input Output of Capture/Compare channel 2

code or data. Therefore, even though the ROM device contains either a 24-Kbyte or 32-Kbyte ROM, the maximum size of code that can be placed in the ROM is the given size less four bytes.

3.2.1 Memory Protection Strategy

The XC886/888 memory protection strategy includes:

- Read-out protection: The user is able to protect the contents in the Flash (for Flash devices) and ROM (for ROM devices) memory from being read
  - Flash protection is enabled by programming a valid password (8-bit non-zero value) via BSL mode 6.
  - ROM protection is fixed with the ROM mask and is always enabled.
- Flash program and erase protection: This feature is available only for Flash devices.

3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

Table 4 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection	
Hardware Protection Mode	-	0	1
Activation	Program a valid password via BSL mode 6		
Selection	Bit 4 of password = 0	Bit 4 of password = 1 MSB of password = 0	Bit 4 of password = 1 MSB of password = 1
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D-Flash
External access to P-Flash	Not possible	Not possible	Not possible

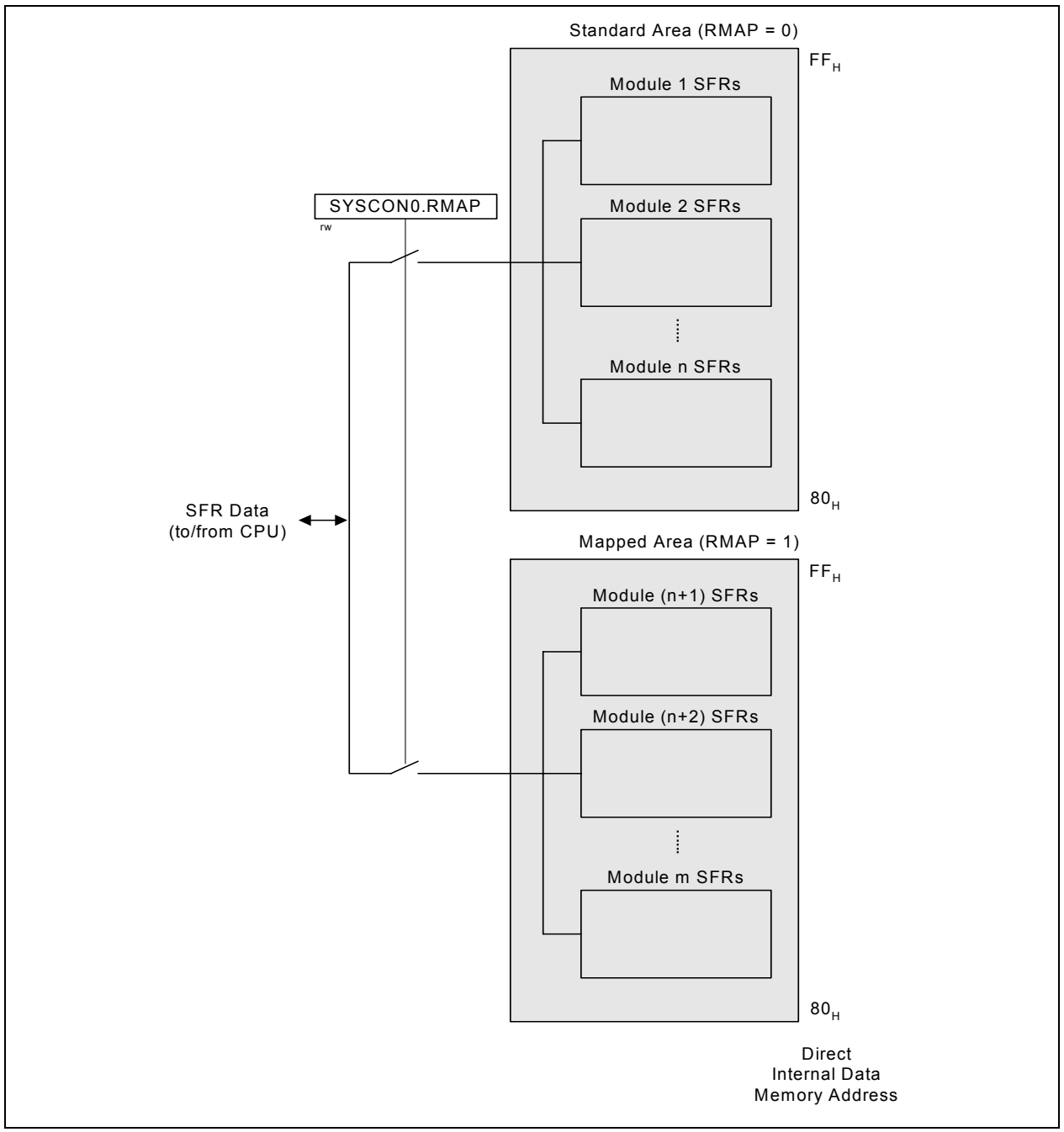
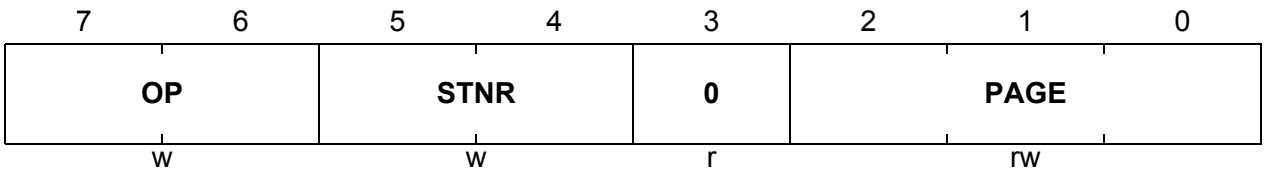


Figure 8 Address Extension by Mapping

The page register has the following definition:

MOD_PAGE
Page Register for module MOD **Reset Value: 00_H**



Field	Bits	Type	Description
PAGE	[2:0]	rw	**Page Bits** When written, the value indicates the new page. When read, the value indicates the currently active page.
STNR	[5:4]	w	**Storage Number** This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10_B, the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11_B, the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored. 00 ST0 is selected. 01 ST1 is selected. 10 ST2 is selected. 11 ST3 is selected.

Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
$D3_H$	**ADC_RESR3H Reset: 00_H** Result Register 3 High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 3										
CA_H	**ADC_RESRA0L Reset: 00_H** Result Register 0, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CB_H	**ADC_RESRA0H Reset: 00_H** Result Register 0, View A High	Bit Field	RESULT							
		Type	rh							
CC_H	**ADC_RESRA1L Reset: 00_H** Result Register 1, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CD_H	**ADC_RESRA1H Reset: 00_H** Result Register 1, View A High	Bit Field	RESULT							
		Type	rh							
CE_H	**ADC_RESRA2L Reset: 00_H** Result Register 2, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
CF_H	**ADC_RESRA2H Reset: 00_H** Result Register 2, View A High	Bit Field	RESULT							
		Type	rh							
$D2_H$	**ADC_RESRA3L Reset: 00_H** Result Register 3, View A Low	Bit Field	RESULT			VF	DRC	CHNR		
		Type	rh			rh	rh	rh		
$D3_H$	**ADC_RESRA3H Reset: 00_H** Result Register 3, View A High	Bit Field	RESULT							
		Type	rh							
RMAP = 0, PAGE 4										
CA_H	**ADC_RCR0 Reset: 00_H** Result Control Register 0	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CB_H	**ADC_RCR1 Reset: 00_H** Result Control Register 1	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CC_H	**ADC_RCR2 Reset: 00_H** Result Control Register 2	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CD_H	**ADC_RCR3 Reset: 00_H** Result Control Register 3	Bit Field	VFCTR	WFR	0	IEN	0			DRCTR
		Type	rw	rw	r	rw	r			rw
CE_H	**ADC_VFCR Reset: 00_H** Valid Flag Clear Register	Bit Field	0				VFC3	VFC2	VFC1	VFC0
		Type	r				w	w	w	w
RMAP = 0, PAGE 5										
CA_H	**ADC_CHINFR Reset: 00_H** Channel Interrupt Flag Register	Bit Field	CHINF7	CHINF6	CHINF5	CHINF4	CHINF3	CHINF2	CHINF1	CHINF0
		Type	rh	rh	rh	rh	rh	rh	rh	rh
CB_H	**ADC_CHINCR Reset: 00_H** Channel Interrupt Clear Register	Bit Field	CHINC7	CHINC6	CHINC5	CHINC4	CHINC3	CHINC2	CHINC1	CHINC0
		Type	w	w	w	w	w	w	w	w

Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FB_H	**CCU6_TCTR2H Reset: 00_H** Timer Control Register 2 High	Bit Field	0				T13RSEL		T12RSEL	
		Type	r				rw		rw	
FC_H	**CCU6_MODCTRL Reset: 00_H** Modulation Control Register Low	Bit Field	MCM EN	0	T12MODEN					
		Type	rw	r	rw					
FD_H	**CCU6_MODCTRH Reset: 00_H** Modulation Control Register High	Bit Field	ECT13O	0	T13MODEN					
		Type	rw	r	rw					
FE_H	**CCU6_TRPCTRL Reset: 00_H** Trap Control Register Low	Bit Field	0					TRPM2	TRPM1	TRPM0
		Type	r					rw	rw	rw
FF_H	**CCU6_TRPCTRH Reset: 00_H** Trap Control Register High	Bit Field	TRPPEN	TRPEN13	TRPEN					
		Type	rw	rw	rw					
RMAP = 0, PAGE 3										
$9A_H$	**CCU6_MCMOUTL Reset: 00_H** Multi-Channel Mode Output Register Low	Bit Field	0	R	MCMP					
		Type	r	rh	rh					
$9B_H$	**CCU6_MCMOUTH Reset: 00_H** Multi-Channel Mode Output Register High	Bit Field	0		CURH			EXPH		
		Type	r		rh			rh		
$9C_H$	**CCU6_ISL Reset: 00_H** Capture/Compare Interrupt Status Register Low	Bit Field	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9D_H$	**CCU6_ISH Reset: 00_H** Capture/Compare Interrupt Status Register High	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM
		Type	rh	rh	rh	rh	rh	rh	rh	rh
$9E_H$	**CCU6_PISEL0L Reset: 00_H** Port Input Select Register 0 Low	Bit Field	ISTRP		ISCC62		ISCC61		ISCC60	
		Type	rw		rw		rw		rw	
$9F_H$	**CCU6_PISEL0H Reset: 00_H** Port Input Select Register 0 High	Bit Field	IST12HR		ISPOS2		ISPOS1		ISPOS0	
		Type	rw		rw		rw		rw	
$A4_H$	**CCU6_PISEL2 Reset: 00_H** Port Input Select Register 2	Bit Field	0						IST13HR	
		Type	r						rw	
FA_H	**CCU6_T12L Reset: 00_H** Timer T12 Counter Register Low	Bit Field	T12CVL							
		Type	rwh							
FB_H	**CCU6_T12H Reset: 00_H** Timer T12 Counter Register High	Bit Field	T12CVH							
		Type	rwh							
FC_H	**CCU6_T13L Reset: 00_H** Timer T13 Counter Register Low	Bit Field	T13CVL							
		Type	rwh							
FD_H	**CCU6_T13H Reset: 00_H** Timer T13 Counter Register High	Bit Field	T13CVH							
		Type	rwh							

Table 18 OCDS Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
EC_H	**MMWR2** **Reset: 00_H** Monitor Work Register 2	Bit Field	MMWR2							
		Type	rw							

3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC886/888 interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

3.4.1 Interrupt Source

Figure 13 to **Figure 17** give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

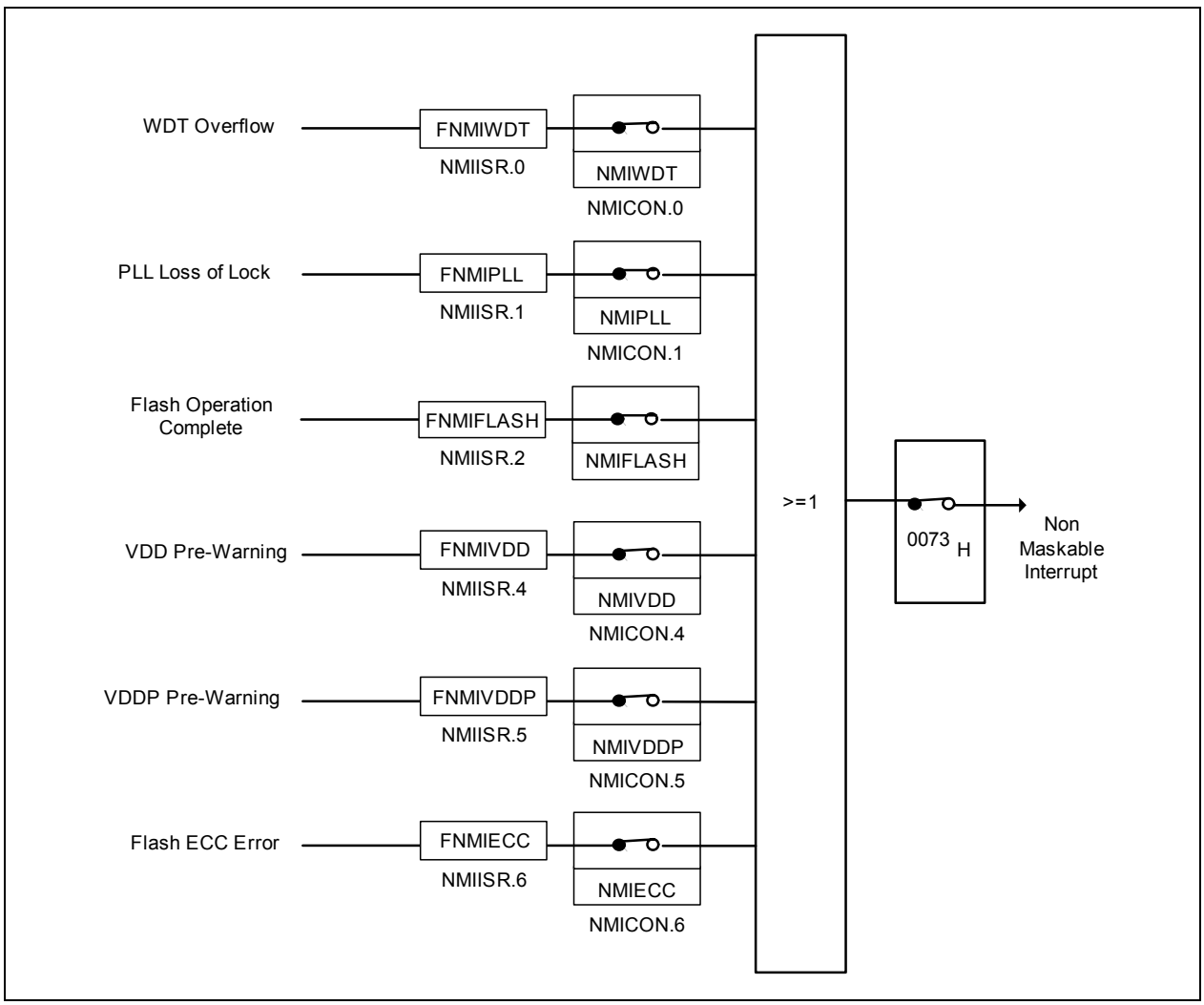


Figure 13 Non-Maskable Interrupt Request Sources

3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 21**.

Table 21 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
Timer 2,UART Normal Divider Overflow, MultiCAN, LIN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
CCU6 Interrupt Node Pointer 0, MultiCAN interrupt	11
CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt	12
CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt	13
CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt	14

Figure 20 shows the structure of an input-only port pin.

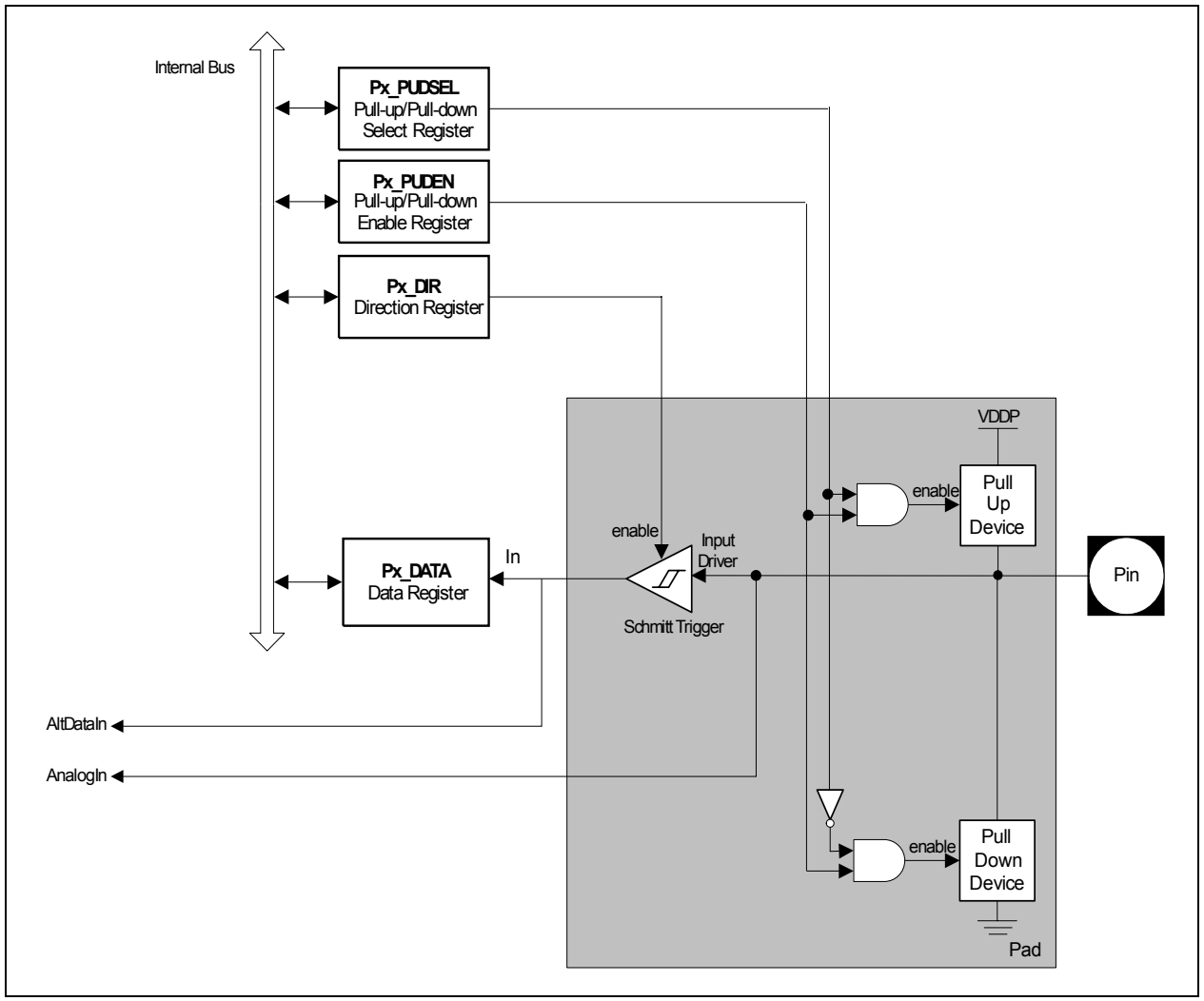


Figure 20 General Structure of Input Port

fractional divider) for generating a wide range of baud rates based on its input clock f_{PCLK}, see **Figure 30**.

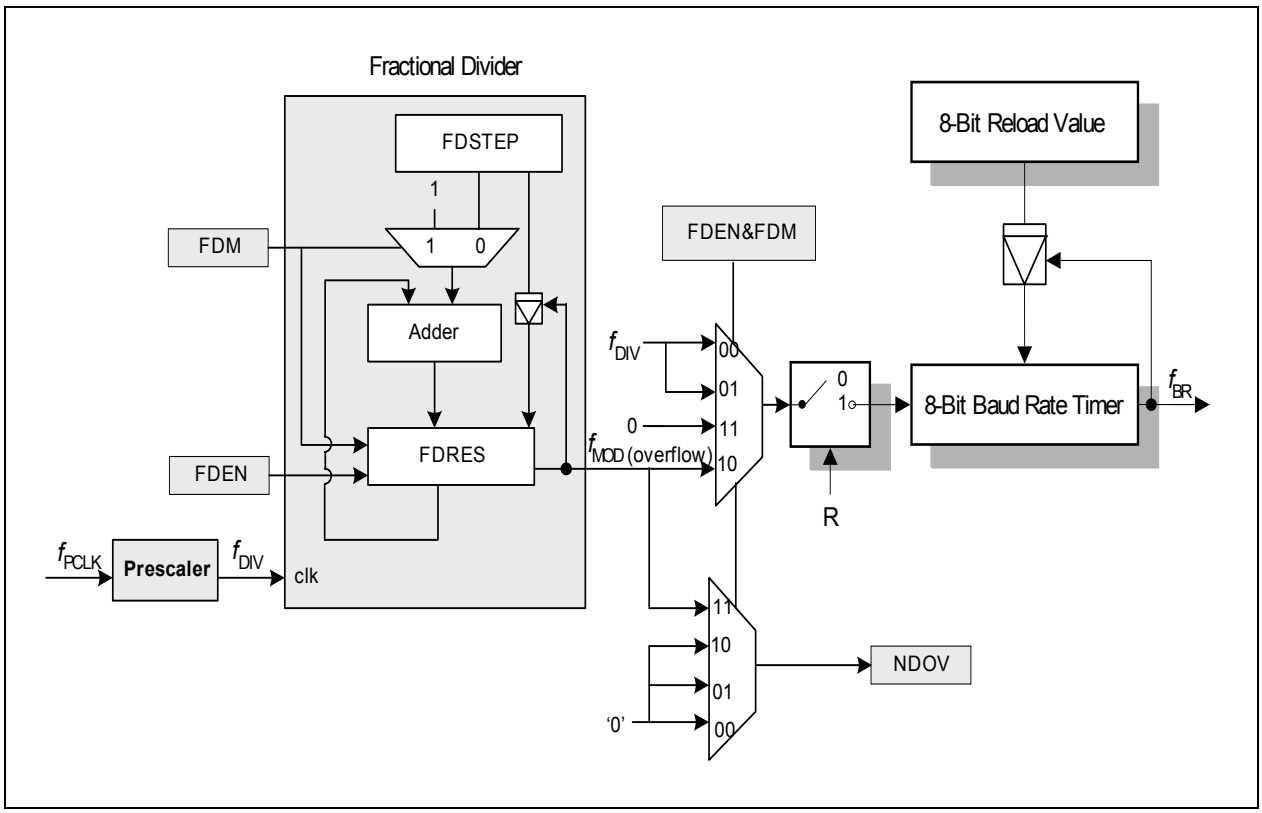


Figure 30 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider (f_{MOD}) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler (f_{DIV}) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate (f_{BR}) value is dependent on the following parameters:

- Input clock f_{PCLK}
- Prescaling factor (2^{BRPRE}) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
  (to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR_VALUE) for the baud rate timer defined by register BG

3.15 LIN Protocol

The UART module can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature, which consists of the hardware logic for Break and Synch Byte detection, provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

Note: The LIN baud rate detection feature is available for use only with UART. To use UART1 for LIN communication, software has to be implemented to detect the Break and Synch Byte.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in **Figure 31**. The frame consists of the:

- Header, which comprises a Break (13-bit time low), Synch Byte (55_H), and ID field
- Response time
- Data bytes (according to UART protocol)
- Checksum

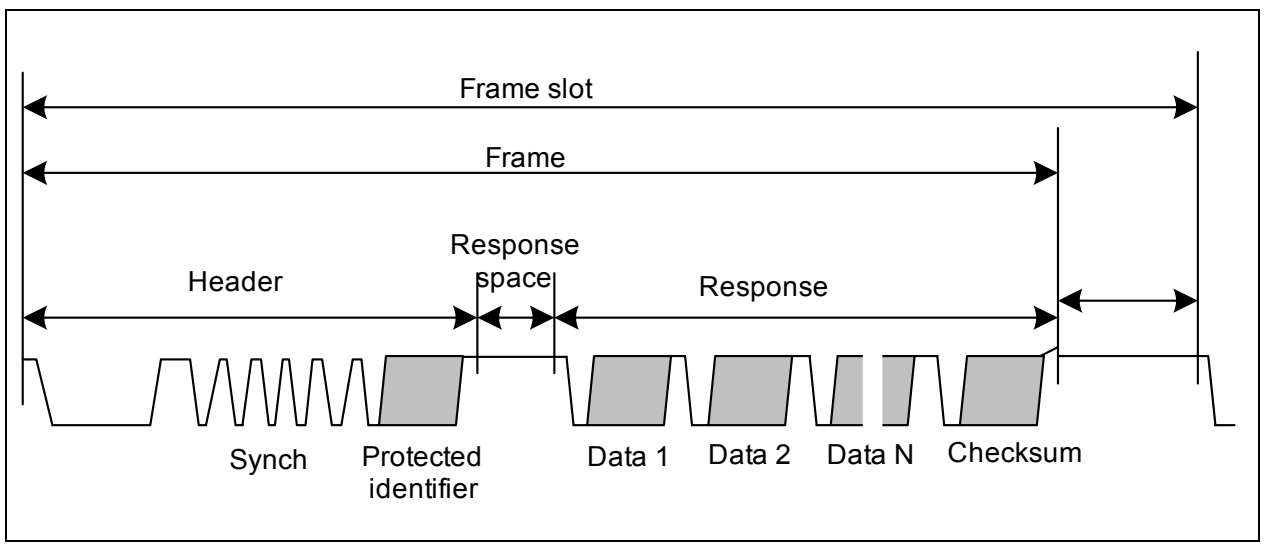


Figure 31 Structure of LIN Frame

3.15.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information

3.22 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

Features

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in **Figure 37**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG[1)], which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC886/888 has been started in OCDS mode.

1) The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).
User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.

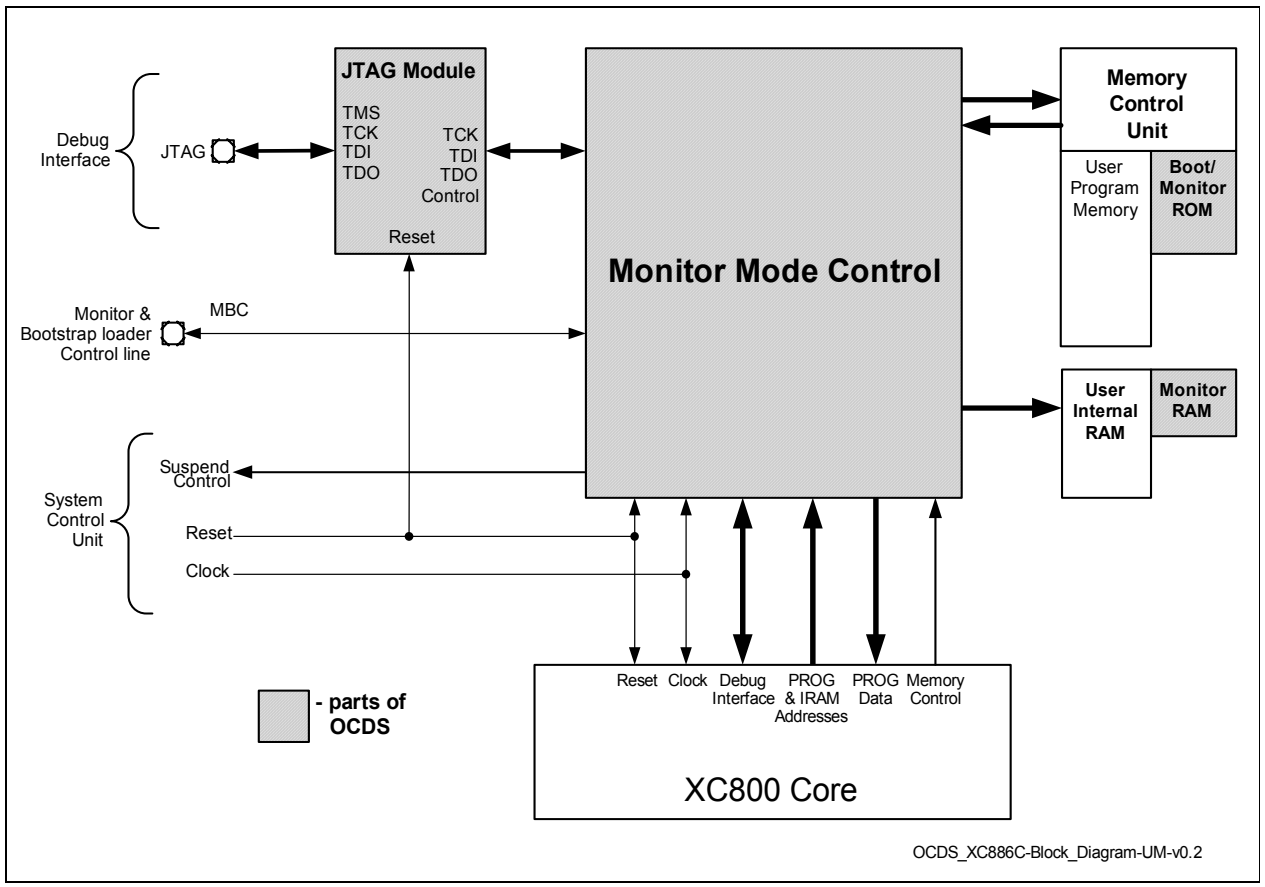


Figure 37 OCDS Block Diagram

3.22.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode 04_H), and the same is also true immediately after reset.

The JTAG ID register contents for the XC886/888 Flash devices are given in **Table 35**.

Table 35 JTAG ID Summary

Device Type	Device Name	JTAG ID
Flash	XC886/888*-8FF	$1012\ 0083_H$
	XC886/888*-6FF	$1012\ 5083_H$
ROM	XC886/888*-8RF	$1013\ C083_H$
	XC886/888*-6RF	$1013\ D083_H$

Note: The asterisk (*) above denotes all possible device configurations.

Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	**AB-Step**	**AC-Step**
XC888CM-6RFA 5V	22891503_H	-	-
XC886C-6RFA 5V	22891542_H	-	-
XC888C-6RFA 5V	22891543_H	-	-
XC886-6RFA 5V	22891562_H	-	-
XC888-6RFA 5V	22891563_H	-	-

4.2.4 Power Supply Current

Table 41, **Table 42**, **Table 43** and **Table 44** provide the characteristics of the power supply current in the XC886/888.

Table 41 Power Supply Current Parameters (Operating Conditions apply; V_{DDP} = 5V range)

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ.[1]	max.[2]		
V_{DDP} = 5V Range					
Active Mode	I_{DDP}	27.2	32.8	mA	Flash Device[3]
		24.3	29.8	mA	ROM Device[3]
Idle Mode	I_{DDP}	21.1	25.3	mA	Flash Device[4]
		18.2	21.6	mA	ROM Device[4]
Active Mode with slow-down enabled	I_{DDP}	14.1	17.0	mA	Flash Device[5]
		11.9	14.3	mA	ROM Device[5]
Idle Mode with slow-down enabled	I_{DDP}	11.7	15.0	mA	Flash Device[6]
		9.7	11.9	mA	ROM Device[6]

1) The typical I_{DDP} values are periodically measured at T_A = + 25 °C and V_{DDP} = 5.0 V.

2) The maximum I_{DDP} values are measured under worst case conditions (T_A = + 125 °C and V_{DDP} = 5.5 V).

3) I_{DDP} (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz(set by on-chip oscillator of 9.6 MHz and NDIV in PLL_CON to 1001_B), $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

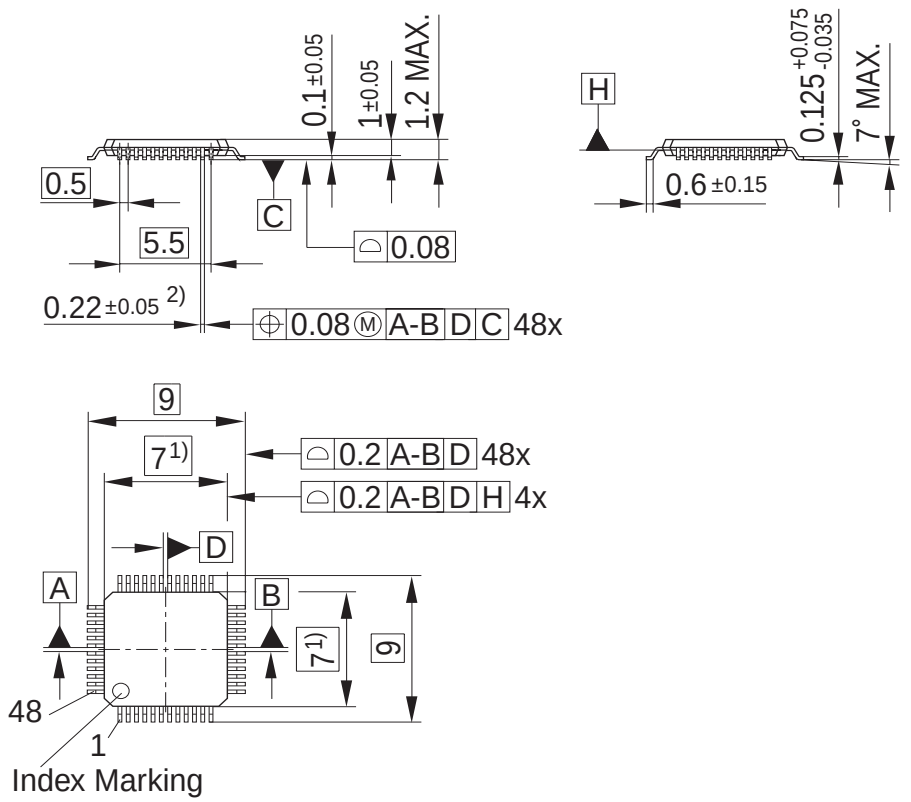
4) I_{DDP} (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

5) I_{DDP} (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 8 MHz by setting CLKREL in CMCON to 0110_B, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

6) I_{DDP} (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 8 MHz by setting CLKREL in CMCON to 0110_B, $\overline{\text{RESET}}$ = V_{DDP}, no load on ports.

5.2 Package Outline

Figure 48 shows the package outlines of the XC886.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

GPP09237

Figure 48 PG-TQFP-48 Package Outline

5.3 Quality Declaration

Table 2 shows the characteristics of the quality parameters in the XC886/888.

Table 2 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	-	2000	V	Conforming to EIA/JESD22-A114-B[1)]
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM}	-	500	V	Conforming to JESD22-C101-C[1)]

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

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