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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	24KB (24K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc888-6ffa-5v-ac

Summary of Features

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
 - PLL loss-of-lock detection
- Power saving modes
 - slow-down mode
 - idle mode
 - power-down mode with wake-up capability via RXD or EXINT0
 - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Six ports
 - Up to 48 pins as digital I/O
 - 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Four 16-bit timers
 - Timer 0 and Timer 1 (T0 and T1)
 - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- Software libraries to support floating point and MDU calculations
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Capture/compare unit for PWM signal generation (CCU6)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
 - 1 Kbyte of monitor ROM (part of the 12-Kbyte Boot ROM)
 - 64 bytes of monitor RAM
- Packages:
 - PG-TQFP-48
 - PG-TQFP-64
- Temperature range T_A :
 - SAF (-40 to 85 °C)
 - SAK (-40 to 125 °C)

General Device Information
2.4 Pin Definitions and Functions

The functions and default states of the XC886/888 external pins are provided in [Table 3](#).

Table 3 Pin Definitions and Functions

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P0		I/O		Port 0 Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, Timer 2, Timer 21, MultiCAN and SSC.
P0.0	11/17		Hi-Z	<div>TCK_0 JTAG Clock Input</div> <div>T12HR_1 CCU6 Timer 12 Hardware Run Input</div> <div>CC61_1 Input/Output of Capture/Compare channel 1</div> <div>CLKOUT_0 Clock Output</div> <div>RXDO_1 UART Transmit Data Output</div>
P0.1	13/21		Hi-Z	<div>TDI_0 JTAG Serial Data Input</div> <div>T13HR_1 CCU6 Timer 13 Hardware Run Input</div> <div>RXD_1 UART Receive Data Input</div> <div>RXDC1_0 MultiCAN Node 1 Receiver Input</div> <div>COUT61_1 Output of Capture/Compare channel 1</div> <div>EXF2_1 Timer 2 External Flag Output</div>
P0.2	12/18		PU	<div>CTRAP_2 CCU6 Trap Input</div> <div>TDO_0 JTAG Serial Data Output</div> <div>TXD_1 UART Transmit Data Output/Clock Output</div> <div>TXDC1_0 MultiCAN Node 1 Transmitter Output</div>
P0.3	48/63		Hi-Z	<div>SCK_1 SSC Clock Input/Output</div> <div>COUT63_1 Output of Capture/Compare channel 3</div> <div>RXDO1_0 UART1 Transmit Data Output</div>

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P0.4	1/64		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
				TXD1_0	UART1 Transmit Data Output/Clock Output
P0.5	2/1		Hi-Z	MRST_1	SSC Master Receive Input/Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				T2EX1_1	Timer 21 External Trigger Input
				RXD1_0	UART1 Receive Data Input
				COUT62_1	Output of Capture/Compare channel 2
P0.6	–/2		PU	GPIO	
P0.7	47/62		PU	CLKOUT_1	Clock Output

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, Timer 2, Timer 21, MultiCAN and SSC.
P1.0	26/34		PU	RXD_0 UART Receive Data Input T2EX Timer 2 External Trigger Input RXDC0_0 MultiCAN Node 0 Receiver Input
P1.1	27/35		PU	EXINT3 External Interrupt Input 3 T0_1 Timer 0 Input TDO_1 JTAG Serial Data Output TXD_0 UART Transmit Data Output/Clock Output TXDC0_0 MultiCAN Node 0 Transmitter Output
P1.2	28/36		PU	SCK_0 SSC Clock Input/Output
P1.3	29/37		PU	MTSR_0 SSC Master Transmit Output/Slave Receive Input TXDC1_3 MultiCAN Node 1 Transmitter Output
P1.4	30/38		PU	MRST_0 SSC Master Receive Input/ Slave Transmit Output EXINT0_1 External Interrupt Input 0 RXDC1_3 MultiCAN Node 1 Receiver Input
P1.5	31/39		PU	CCPOS0_1 CCU6 Hall Input 0 EXINT5 External Interrupt Input 5 T1_1 Timer 1 Input EXF2_0 Timer 2 External Flag Output RXDO_0 UART Transmit Data Output

General Device Information

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P2		I		Port 2 Port 2 is an 8-bit general purpose input-only port. It can be used as alternate functions for the digital inputs of the JTAG and CCU6. It is also used as the analog inputs for the ADC.
P2.0	14/22		Hi-Z	CCPOS0_0 CCU6 Hall Input 0 EXINT1_0 External Interrupt Input 1 T12HR_2 CCU6 Timer 12 Hardware Run Input TCK_1 JTAG Clock Input CC61_3 Input of Capture/Compare channel 1 AN0 Analog Input 0
P2.1	15/23		Hi-Z	CCPOS1_0 CCU6 Hall Input 1 EXINT2_0 External Interrupt Input 2 T13HR_2 CCU6 Timer 13 Hardware Run Input TDI_1 JTAG Serial Data Input CC62_3 Input of Capture/Compare channel 2 AN1 Analog Input 1
P2.2	16/24		Hi-Z	CCPOS2_0 CCU6 Hall Input 2 CTRAP_1 CCU6 Trap Input CC60_3 Input of Capture/Compare channel 0 AN2 Analog Input 2
P2.3	19/27		Hi-Z	AN3 Analog Input 3
P2.4	20/28		Hi-Z	AN4 Analog Input 4
P2.5	21/29		Hi-Z	AN5 Analog Input 5
P2.6	22/30		Hi-Z	AN6 Analog Input 6
P2.7	25/33		Hi-Z	AN7 Analog Input 7

General Device Information
Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
P3		I/O		Port 3 Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CCU6 Hall Input 1 CC60_0 Input/Output of Capture/Compare channel 0 RXDO1_1 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CCU6 Hall Input 0 CC61_2 Input/Output of Capture/Compare channel 1 COUT60_0 Output of Capture/Compare channel 0 TXD1_1 UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 CCU6 Hall Input 2 RXDC1_1 MultiCAN Node 1 Receiver Input RXD1_1 UART1 Receive Data Input CC61_0 Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 Output of Capture/Compare channel 1 TXDC1_1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 Input/Output of Capture/Compare channel 2 RXDC0_1 MultiCAN Node 0 Receiver Input T2EX1_0 Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 Output of Capture/Compare channel 2 EXF21_0 Timer 21 External Flag Output TXDC0_1 MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	CTRAP_0 CCU6 Trap Input

General Device Information

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function
V_{DDP}	7, 17, 43/ 7, 25, 55	—	—	I/O Port Supply (3.3 or 5.0 V) Also used by EVR and analog modules. All pins must be connected.
V_{SSP}	18, 42/26, 54	—	—	I/O Port Ground All pins must be connected.
V_{DDC}	6/6	—	—	Core Supply Monitor (2.5 V)
V_{SSC}	5/5	—	—	Core Supply Ground
V_{AREF}	24/32	—	—	ADC Reference Voltage
V_{AGND}	23/31	—	—	ADC Reference Ground
XTAL1	4/4	I	Hi-Z	External Oscillator Input (backup for on-chip OSC, normally NC)
XTAL2	3/3	O	Hi-Z	External Oscillator Output (backup for on-chip OSC, normally NC)
TMS	10/16	I	PD	Test Mode Select
RESET	41/53	I	PU	Reset Input
MBC¹⁾	44/58	I	PU	Monitor & BootStrap Loader Control
NC	—/56, 57	—	—	No Connection

1) An external pull-up device in the range of 4.7 k Ω to 100 k Ω . is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.

Functional Description
Table 5 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
A8 _H	IEN0 Reset: 00 _H Interrupt Enable Register 0	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
		Type	rw	r	rw	rw	rw	rw	rw	rw
B8 _H	IP Reset: 00 _H Interrupt Priority Register	Bit Field	0		PT2	PS	PT1	PX1	PT0	PX0
		Type	r		rw	rw	rw	rw	rw	rw
B9 _H	IPH Reset: 00 _H Interrupt Priority High Register	Bit Field	0		PT2H	PSH	PT1H	PX1H	PT0H	PX0H
		Type	r		rw	rw	rw	rw	rw	rw
D0 _H	PSW Reset: 00 _H Program Status Word Register	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	P
		Type	rwh	rwh	rw	rw	rw	rwh	rw	rh
E0 _H	ACC Reset: 00 _H Accumulator Register	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
E8 _H	IEN1 Reset: 00 _H Interrupt Enable Register 1	Bit Field	ECCIP 3	ECCIP 2	ECCIP 1	ECCIP 0	EXM	EX2	ESSC	EADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F0 _H	B Reset: 00 _H B Register	Bit Field	B7	B6	B5	B4	B3	B2	B1	B0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F8 _H	IP1 Reset: 00 _H Interrupt Priority 1 Register	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
		Type	rw	rw	rw	rw	rw	rw	rw	rw
F9 _H	IPH1 Reset: 00 _H Interrupt Priority 1 High Register	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSC H	PADC H
		Type	rw	rw	rw	rw	rw	rw	rw	rw

3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 MDU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 1										
B0 _H	MDUSTAT Reset: 00_H MDU Status Register	Bit Field	0					BSY	IERR	IRDY
		Type	r					rh	rwh	rwh
B1 _H	MDUCON Reset: 00_H MDU Control Register	Bit Field	IE	IR	RSEL	STAR T	OPCODE			
		Type	rw	rw	rw	rwh	rw			
B2 _H	MD0 Reset: 00_H MDU Operand Register 0	Bit Field	DATA							
		Type	rw							
B2 _H	MR0 Reset: 00_H MDU Result Register 0	Bit Field	DATA							
		Type	rh							
B3 _H	MD1 Reset: 00_H MDU Operand Register 1	Bit Field	DATA							
		Type	rw							

Functional Description

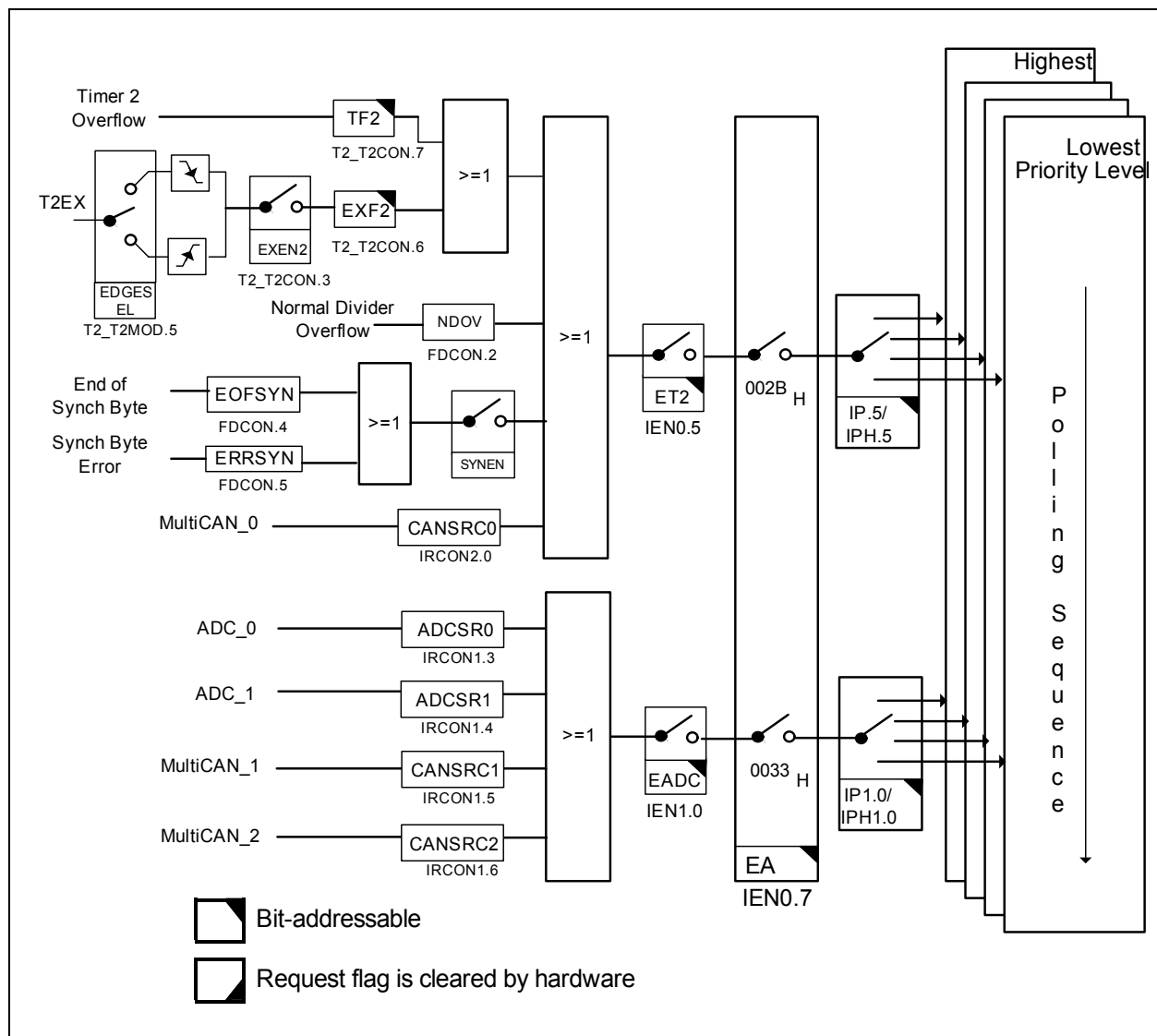


Figure 15 Interrupt Request Sources (Part 2)

Functional Description

- 1) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
- 2) OSC is bypassed in MultiCAN BSL mode
- 3) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC886/888. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

Features

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support

The CGU consists of an oscillator circuit and a PLL. In the XC886/888, the oscillator can be from either of these two sources: the on-chip oscillator (9.6 MHz) or the external oscillator (4 MHz to 12 MHz). The term “oscillator” is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default. The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

Functional Description

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for 30_H count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from 0000_H to the value obtained from the concatenation of WDTWINB and 00_H.

After being serviced, the WDT continues counting up from the value (<WDTREL> * 2⁸). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, P_{WDT} , between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}} \quad (3.4)$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period P_{WDT} between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see [Figure 29](#). This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.

Functional Description

The following formulas calculate the final baud rate without and with the fractional divider respectively:

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \quad \text{where } 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1) > 1 \quad (3.5)$$

$$\text{baud rate} = \frac{f_{\text{PCLK}}}{16 \times 2^{\text{BRPRE}} \times (\text{BR_VALUE} + 1)} \times \frac{\text{STEP}}{256} \quad (3.6)$$

The maximum baud rate that can be generated is limited to $f_{\text{PCLK}}/32$. Hence, for a module clock of 24 MHz, the maximum achievable baud rate is 0.75 MBaud.

Standard LIN protocol can support a maximum baud rate of 20 kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20 kHz to 115.2 kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

Table 30 lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 24 MHz is used.

Table 30 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000 _B)	78 (4E _H)	0.17 %
9600 Baud	1 (BRPRE=000 _B)	156 (9C _H)	0.17 %
4800 Baud	2 (BRPRE=001 _B)	156 (9C _H)	0.17 %
2400 Baud	4 (BRPRE=010 _B)	156 (9C _H)	0.17 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 31** lists the resulting deviation errors from generating a baud rate of 115.2 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

3.15 LIN Protocol

The UART module can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature, which consists of the hardware logic for Break and Synch Byte detection, provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

Note: The LIN baud rate detection feature is available for use only with UART. To use UART1 for LIN communication, software has to be implemented to detect the Break and Synch Byte.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in [Figure 31](#). The frame consists of the:

- Header, which comprises a Break (13-bit time low), Synch Byte (55_H), and ID field
- Response time
- Data bytes (according to UART protocol)
- Checksum

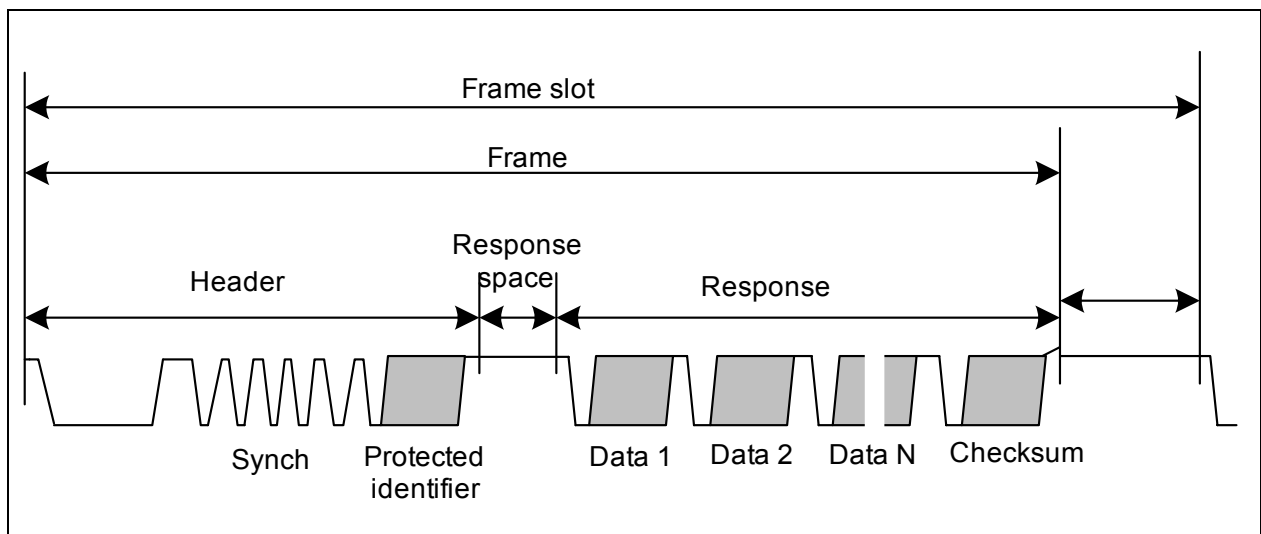


Figure 31 Structure of LIN Frame

3.15.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information

3.19 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

Timer T12 Features

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Generation of center-aligned and edge-aligned PWM
- Supports single-shot mode
- Supports many interrupt request sources
- Hysteresis-like control mode

Timer T13 Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Supports single-shot mode

Additional Features

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The block diagram of the CCU6 module is shown in [Figure 33](#).

Functional Description

- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
 - allocated (assigned) to any CAN node
 - configured as transmit or receive object
 - setup to handle frames with 11-bit or 29-bit identifier
 - counted or assigned a timestamp via a frame counter
 - configured to remote monitoring mode
- Advanced Acceptance Filtering:
 - Each message object provides an individual acceptance mask to filter incoming frames.
 - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
 - Message objects can be grouped into 4 priority classes.
 - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
 - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
 - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
 - The Message objects are organized in double chained lists.
 - List reorganizations may be performed any time, even during full operation of the CAN nodes.
 - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
 - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
 - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
 - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
 - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

Functional Description
Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	AB-Step	AC-Step
XC886-6FFA 3V3	-	095D1562 _H	0B5D1562 _H
XC888-6FFA 3V3	-	095D1563 _H	0B5D1563 _H
XC886CLM-8FFA 5V	-	09900102 _H	0B900102 _H
XC888CLM-8FFA 5V	-	09900103 _H	0B900103 _H
XC886LM-8FFA 5V	-	09900122 _H	0B900122 _H
XC888LM-8FFA 5V	-	09900123 _H	0B900123 _H
XC886CLM-6FFA 5V	-	09951502 _H	0B951502 _H
XC888CLM-6FFA 5V	-	09951503 _H	0B951503 _H
XC886LM-6FFA 5V	-	09951522 _H	0B951522 _H
XC888LM-6FFA 5V	-	09951523 _H	0B951523 _H
XC886CM-8FFA 5V	-	09980102 _H	0B980102 _H
XC888CM-8FFA 5V	-	09980103 _H	0B980103 _H
XC886C-8FFA 5V	-	09980142 _H	0B980142 _H
XC888C-8FFA 5V	-	09980143 _H	0B980143 _H
XC886-8FFA 5V	-	09980162 _H	0B980162 _H
XC888-8FFA 5V	-	09980163 _H	0B980163 _H
XC886CM-6FFA 5V	-	099D1502 _H	0B9D1502 _H
XC888CM-6FFA 5V	-	099D1503 _H	0B9D1503 _H
XC886C-6FFA 5V	-	099D1542 _H	0B9D1542 _H
XC888C-6FFA 5V	-	099D1543 _H	0B9D1543 _H
XC886-6FFA 5V	-	099D1562 _H	0B9D1562 _H
XC888-6FFA 5V	-	099D1563 _H	0B9D1563 _H

ROM Devices

XC886CLM-8RFA 3V3	22400502 _H	-	-
XC888CLM-8RFA 3V3	22400503 _H	-	-
XC886LM-8RFA 3V3	22400522 _H	-	-
XC888LM-8RFA 3V3	22400523 _H	-	-
XC886CLM-6RFA 3V3	22411502 _H	-	-
XC888CLM-6RFA 3V3	22411503 _H	-	-

4.2.2 Supply Threshold Characteristics

Table 39 provides the characteristics of the supply threshold in the XC886/888.

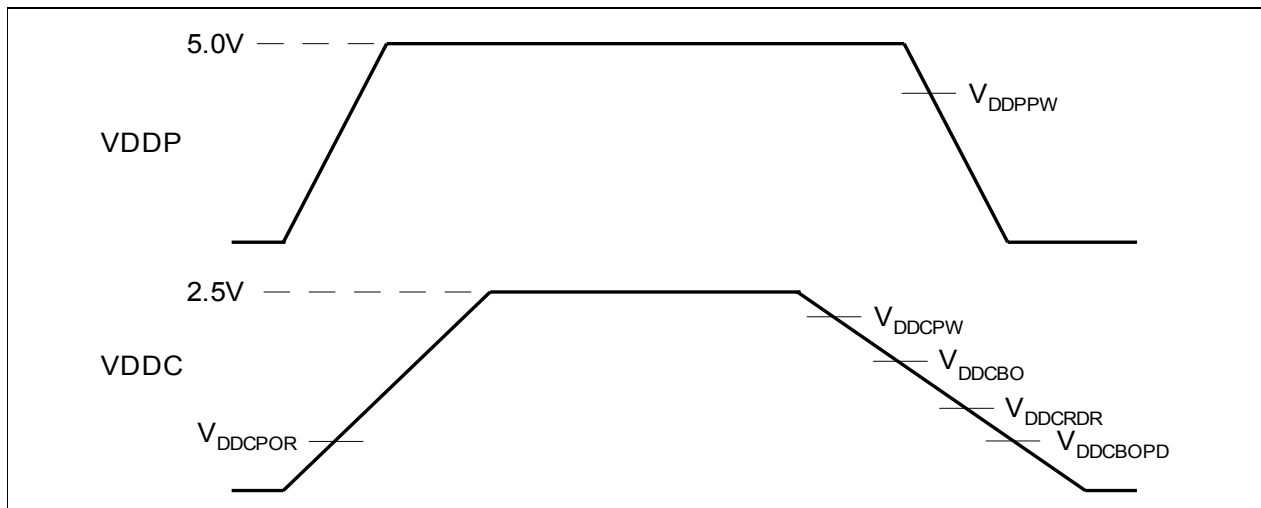


Figure 38 Supply Threshold Parameters

Table 39 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
V_{DDC} prewarning voltage ¹⁾	V_{DDCPW}	CC	2.2	2.3	2.4	V
V_{DDC} brownout voltage in active mode ¹⁾	V_{DDCBO}	CC	2.0	2.1	2.2	V
RAM data retention voltage	V_{DDCRDR}	CC	0.9	1.0	1.1	V
V_{DDC} brownout voltage in power-down mode ²⁾	$V_{DDCBOPD}$	CC	1.3	1.5	1.7	V
V_{DDP} prewarning voltage ³⁾	V_{DDPPW}	CC	3.4	4.0	4.6	V
Power-on reset voltage ²⁾⁴⁾	V_{DDCPOR}	CC	1.3	1.5	1.7	V

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V.
Detection must be disabled for external power supply of 3.3V.

4) The reset of EVR is extended by 300 μ s typically after the VDDC reaches the power-on reset voltage.

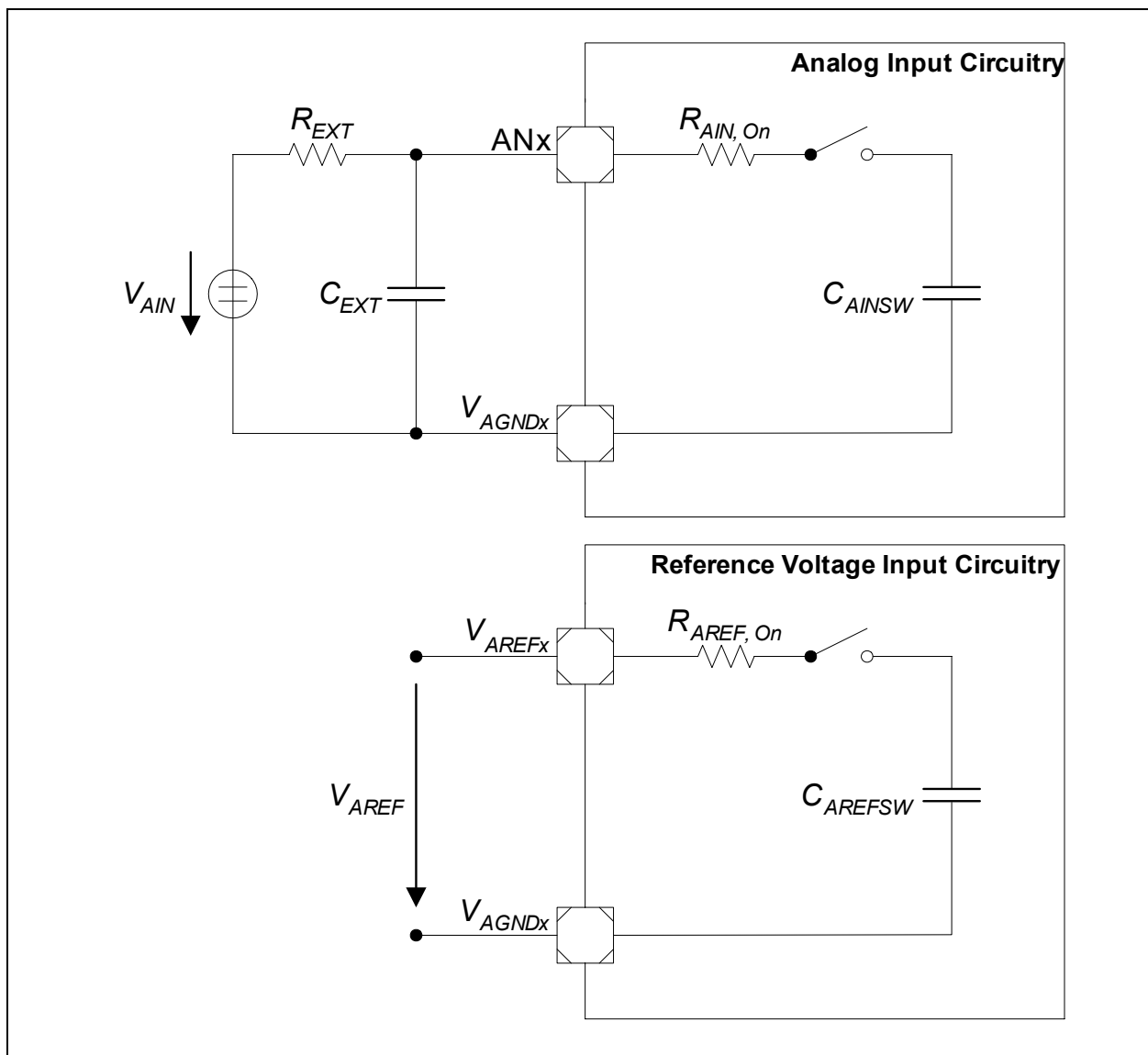


Figure 39 **ADC Input Circuits**

Electrical Parameters

4.3.2 Output Rise/Fall Times

Table 45 provides the characteristics of the output rise/fall times in the XC886/888.

Table 45 Output Rise/Fall Times Parameters (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
V_{DDP} = 5V Range					
Rise/fall times	t_R, t_F	–	10	ns	20 pF. ¹⁾²⁾³⁾
V_{DDP} = 3.3V Range					
Rise/fall times	t_R, t_F	–	10	ns	20 pF. ¹⁾²⁾⁴⁾

1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) Additional rise/fall time valid for $C_L = 20pF - 100pF @ 0.125 ns/pF$.

4) Additional rise/fall time valid for $C_L = 20pF - 100pF @ 0.225 ns/pF$.

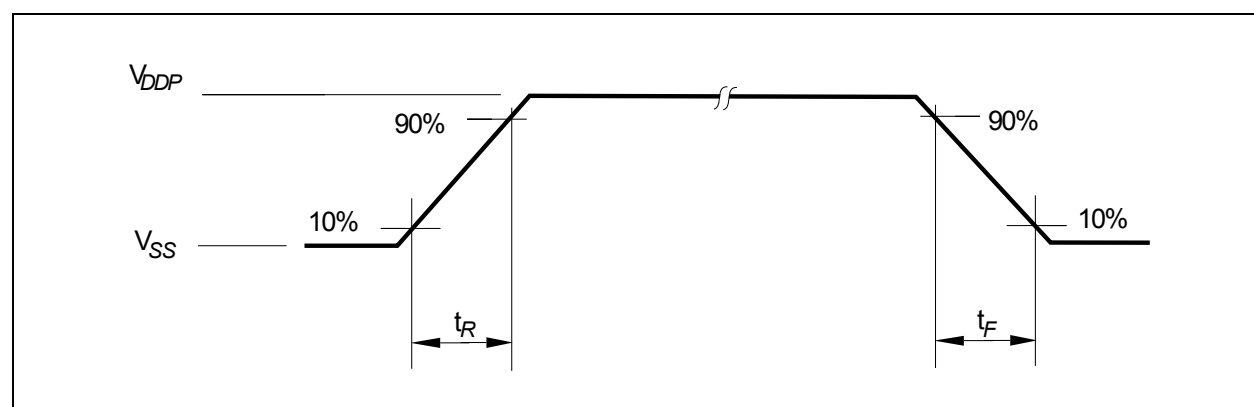


Figure 43 Rise/Fall Times Parameters

Figure 49 shows the package outlines of the XC888.

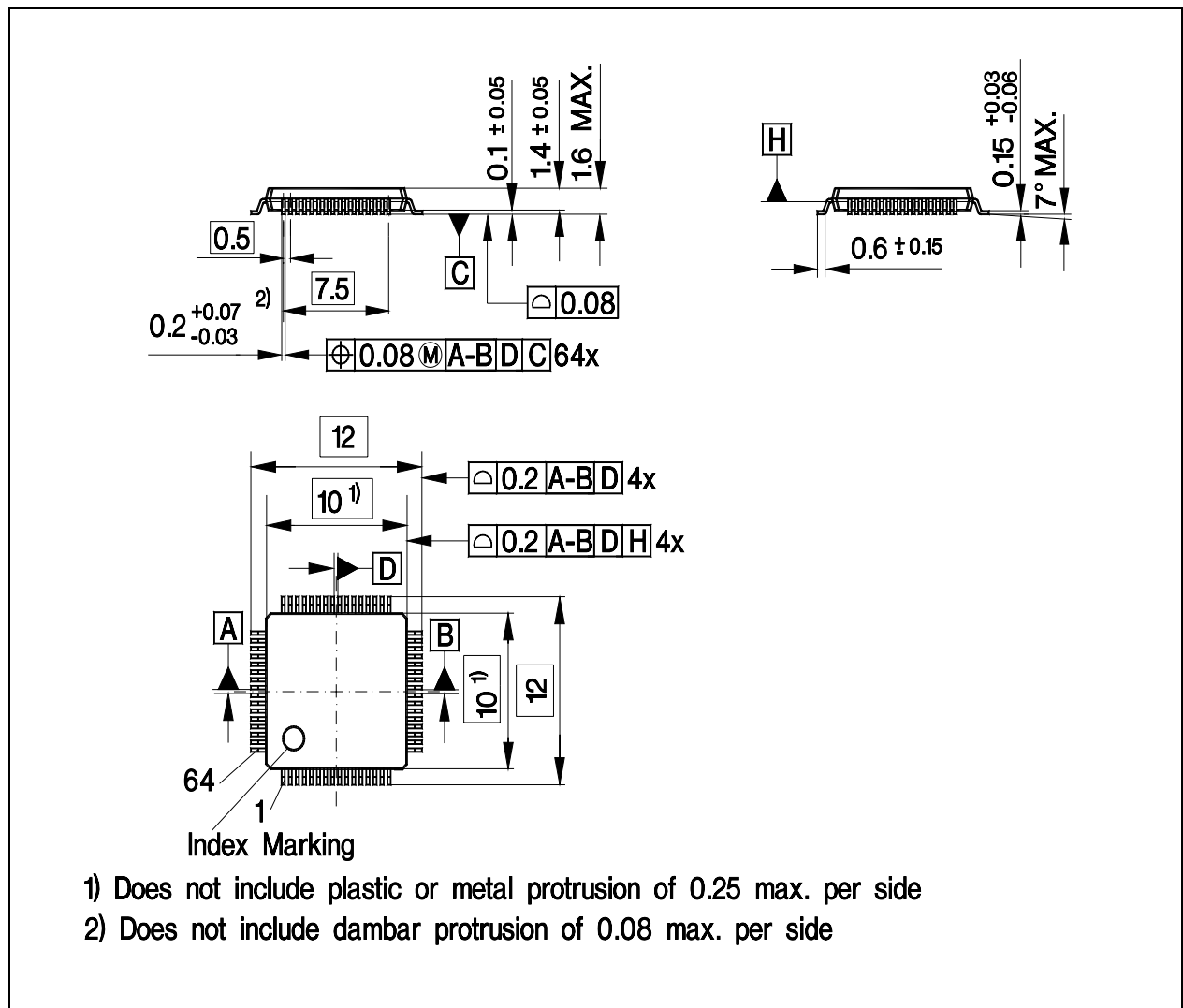


Figure 49 PG-TQFP-64 Package Outline