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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	PG-TQFP-64
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc888-8ffi-5v-ac

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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XC886/888CLM

General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function	
P3		I/O		Port 3 Port 3 is an 8 I/O port. It ca for CCU6, U/	B-bit bidirectional general purpose on be used as alternate functions ART1, Timer 21 and MultiCAN.
P3.0	35/43		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output
P3.1	36/44		Hi-Z	CCPOS0_2 CC61_2 COUT60_0	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare
				TXD1_1	UART1 Transmit Data Output/Clock Output
P3.2	37/49		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1
P3.3	38/50		Hi-Z	COUT61_0 TXDC1_1	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output
P3.4	39/51		Hi-Z	CC62_0 RXDC0_1 T2EX1_0	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input
P3.5	40/52		Hi-Z	COUT62_0 EXF21_0 TXDC0_1	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output
P3.6	33/41		PD	CTRAP 0	CCU6 Trap Input

Table 3Pin Definitions and Functions (cont'd)



General Device Information

Table 3Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function	
P3.7	34/42		Hi-Z	EXINT4 COUT63_0	External Interrupt Input 4 Output of Capture/Compare channel 3



XC886/888CLM

General Device Information

Symbol	Pin Number (TQFP-48/64)	Туре	Reset State	Function
V _{DDP}	7, 17, 43/ 7, 25, 55	-	_	I/O Port Supply (3.3 or 5.0 V) Also used by EVR and analog modules. All pins must be connected.
V _{SSP}	18, 42/26, 54	-	-	I/O Port Ground All pins must be connected.
V _{DDC}	6/6	-	-	Core Supply Monitor (2.5 V)
V _{SSC}	5/5	_	-	Core Supply Ground
V _{AREF}	24/32	_	-	ADC Reference Voltage
V _{AGND}	23/31	_	-	ADC Reference Ground
XTAL1	4/4	I	Hi-Z	External Oscillator Input (backup for on-chip OSC, normally NC)
XTAL2	3/3	0	Hi-Z	External Oscillator Output (backup for on-chip OSC, normally NC)
TMS	10/16	I	PD	Test Mode Select
RESET	41/53	1	PU	Reset Input
MBC ¹⁾	44/58	I	PU	Monitor & BootStrap Loader Control
NC	-/56, 57	_	_	No Connection

Table 3Pin Definitions and Functions (cont'd)

1) An external pull-up device in the range of 4.7 k Ω to 100 k Ω . is required to enter user mode. Alternatively MBC can be tied to high if alternate functions (for debugging) of the pin are not utilized.



SYSCON0

Functional Description

System Control Register 0 Reset Value: 04 7 5 4 3 2 1 0 6 IMODE 1 RMAP 0 0 0 r r r r rw rw

Field	Bits	Туре	Description
RMAP	0	rw	 Interrupt Node XINTR0 Enable 0 The access to the standard SFR area is enabled 1 The access to the mapped SFR area is enabled
1	2	r	Reserved Returns 1 if read; should be written with 1.
0	[7:5], 3,1	r	Reserved Returns 0 if read; should be written with 0.

Note: The RMAP bit should be cleared/set by ANL or ORL instructions.

3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC886/888 has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in **Figure 9**.



Table 14CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
Fe _H	CCU6_CMPSTATL Reset: 00 _H Compare State Register Low	Bit Field	0	CC63 ST	CC POS2	CC POS1	CC POS0	CC62 ST	CC61 ST	CC60 ST
		Туре	r	rh	rh	rh	rh	rh	rh	rh
FF _H	CCU6_CMPSTATH Reset: 00 _H Compare State Register High	Bit Field	T13IM	COUT 63PS	COUT 62PS	CC62 PS	COUT 61PS	CC61 PS	COUT 60PS	CC60 PS
		Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 1									
C8 _H	SCON Reset: 00 _H	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
	Serial Channel Control Register	Туре	rw	rw	rw	rw	rw	rwh	rwh	rwh
C9 _H	SBUF Reset: 00 _H	Bit Field				V	۹L			
	Serial Data Buffer Register	Туре				rv	vh			
CA _H	BCON Reset: 00 _H	Bit Field		()			BRPRE		R
	Baud Rate Control Register	Туре	r				rw			rw
св _Н	BG Reset: 00 _H	Bit Field	BR_VALUE							
	Baud Rate Timer/Reload Register	Туре	rwh							
сс _Н	FDCON Reset: 00 _H	Bit Field			0			NDOV	FDM	FDEN
	Fractional Divider Control Register	Туре		r			rwh	rw	rw	
CD _H	FDSTEP Reset: 00 _H	Bit Field	STEP							
	Fractional Divider Reload Register	Туре	rw							
CeH	FDRES Reset: 00 _H	Bit Field				RES	ULT			
	Fractional Divider Result Register	Туре		rh						





Figure 11 Flash Bank Sectorization

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

3.3.2 Parallel Read Access of P-Flash

To enhance system performance, the P-Flash banks are configured for parallel read to allow two bytes of linear code to be read in 4 x CCLK cycles, compared to 6 x CCLK cycles if serial read is performed. This is achieved by reading two bytes in parallel from a P-Flash bank pair within the 3 x CCLK cycles access time and storing them in a cache. Subsequent read from the cache by the CPU does not require a wait state and can be completed within 1 x CCLK cycle. The result is the average instruction fetch time from the P-Flash banks is reduced and thus, the MIPS (Mega Instruction Per Second) of the system is increased.

However, if the parallel read feature is not desired due to certain timing constraints, it can be disabled by calling the parallel read disable subroutine.



3.3.3 Flash Programming Width

For the P-Flash banks, a programmed wordline (WL) must be erased before it can be reprogrammed as the Flash cells can only withstand one gate disturb. This means that the entire sector containing the WL must be erased since it is impossible to erase a single WL.

For the D-Flash bank, the same WL can be programmed twice before erasing is required as the Flash cells are able to withstand two gate disturbs. This means if the number of data bytes that needs to be written is smaller than the 32-byte minimum programming width, the user can opt to program this number of data bytes (x; where x can be any integer from 1 to 31) first and program the remaining bytes (32 - x) later. Hence, it is possible to program the same WL, for example, with 16 bytes of data two times (see **Figure 12**)



Figure 12 D-Flash Programming

Note: When programming a D-Flash WL the second time, the previously programmed Flash memory cells (whether 0s or 1s) should be reprogrammed with 0s to retain its original contents and to prevent "over-programming".





Figure 15 Interrupt Request Sources (Part 2)



If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for $30_{\rm H}$ count, after which the system is reset (assert WDTRST).

The WDT has a "programmable window boundary" which disallows any refresh during the WDT's count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_{\rm H}$ to the value obtained from the concatenation of WDTWINB and $00_{\rm H}$.

After being serviced, the WDT continues counting up from the value ($\langle WDTREL \rangle * 2^8$). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{\rm PCLK}/2$ or $f_{\rm PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, $P_{\rm WDT}$, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}}$$

(3.4)

If the Window-Boundary Refresh feature of the WDT is enabled, the period $P_{\rm WDT}$ between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 29**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.



Table 51 Deviation Error for OART with Tactional Divider enabled								
f _{pclk}	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error				
24 MHz	1	10 (A _H)	197 (C5 _H)	+0.20 %				
12 MHz	1	6 (6 _H)	236 (EC _H)	+0.03 %				
8 MHz	1	4 (4 _H)	236 (EC _H)	+0.03 %				
6 MHz	1	3 (3 _H)	236 (EC _H)	+0.03 %				

Table 31 Deviation Error for UART with Fractional Divider enabled

3.13.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 baud rate=
$$\frac{2^{\text{SMOD}} \times f_{\text{PCLK}}}{32 \times 2 \times (256 - \text{TH1})}$$

(3.7)

3.14 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see **Figure 30**). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock f_{MOD} that is 1/n of the input clock f_{DIV} , where n is defined by 256 - STEP. The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP}$$

(3.8)



3.15 LIN Protocol

The UART module can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature, which consists of the hardware logic for Break and Synch Byte detection, provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

Note: The LIN baud rate detection feature is available for use only with UART. To use UART1 for LIN communication, software has to be implemented to detect the Break and Synch Byte.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multipleslave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in **Figure 31**. The frame consists of the:

- Header, which comprises a Break (13-bit time low), Synch Byte (55_H), and ID field
- Response time
- Data bytes (according to UART protocol)
- Checksum



Figure 31 Structure of LIN Frame

3.15.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information



XC886/888CLM

Functional Description



Figure 32 SSC Block Diagram



3.21 Analog-to-Digital Converter

The XC886/888 includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at Port 2.

Features

- Successive approximation
- 8-bit or 10-bit resolution (TUE of ± 1 LSB and ± 2 LSB, respectively)
- Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- · Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- · Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- · Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

3.21.1 ADC Clocking Scheme

A common module clock f_{ADC} generates the various clock signals used by the analog and digital parts of the ADC module:

- f_{ADCA} is input clock for the analog part.
- f_{ADCI} is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock f_{ADCA} to generate a correct duty cycle for the analog components.
- f_{ADCD} is input clock for the digital part.

The internal clock for the analog part f_{ADCI} is limited to a maximum frequency of 10 MHz. Therefore, the ADC clock prescaler must be programmed to a value that ensures f_{ADCI} does not exceed 10 MHz. The prescaler ratio is selected by bit field CTC in register



GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.



Figure 35 ADC Clocking Scheme

For module clock f_{ADC} = 24 MHz, the analog clock f_{ADCI} frequency can be selected as shown in **Table 34**.

Table 34	f _{ADCI} Frequency Selection
----------	---------------------------------------

$\frac{f_{ADC}}{Module Clock f_{ADC}}$	СТС	Prescaling Ratio	Analog Clock f_{ADCI}
24 MHz	00 _B	÷ 2	12 MHz (N.A)
	01 _B	÷ 3	8 MHz
	10 _B	÷ 4	6 MHz
	11 _B (default)	÷ 32	750 kHz

As $f_{\rm ADCI}$ cannot exceed 10 MHz, bit field CTC should not be set to $00_{\rm B}$ when $f_{\rm ADC}$ is 24 MHz. During slow-down mode where $f_{\rm ADC}$ may be reduced to 12 MHz, 6 MHz etc., CTC can be set to $00_{\rm B}$ as long as the divided analog clock $f_{\rm ADCI}$ does not exceed 10 MHz.



3.22 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- · Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

Features

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in **Figure 37**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG¹⁾, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC886/888 has been started in OCDS mode.

¹⁾ The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).

User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.



3.23 Chip Identification Number

The XC886/888 identity (ID) register is located at Page 1 of address $B3_{H}$. The value of ID register is 09_{H} for Flash devices and 22_{H} for ROM devices. However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET_CHIP_INFO
- Bootstrap loader (BSL) mode A

Table 36 lists the chip identification numbers of available XC886/888 Flash and ROM device variants.

Product Variant	Chip Identification Number						
	AA-Step	AB-Step	AC-Step				
Flash Devices		·					
XC886CLM-8FFA 3V3	-	09500102 _H	0B500102 _H				
XC888CLM-8FFA 3V3	-	09500103 _H	0B500103 _H				
XC886LM-8FFA 3V3	-	09500122 _H	0B500122 _H				
XC888LM-8FFA 3V3	-	09500123 _H	0B500123 _H				
XC886CLM-6FFA 3V3	-	09551502 _H	0B551502 _H				
XC888CLM-6FFA 3V3	-	09551503 _H	0B551503 _H				
XC886LM-6FFA 3V3	-	09551522 _H	0B551522 _H				
XC888LM-6FFA 3V3	-	09551523 _н	0B551523 _H				
XC886CM-8FFA 3V3	-	09580102 _H	0B580102 _H				
XC888CM-8FFA 3V3	-	09580103 _H	0B580103 _H				
XC886C-8FFA 3V3	-	09580142 _H	0B580142 _H				
XC888C-8FFA 3V3	-	09580143 _H	0B580143 _H				
XC886-8FFA 3V3	-	09580162 _H	0B580162 _H				
XC888-8FFA 3V3	-	09580163 _H	0B580163 _H				
XC886CM-6FFA 3V3	-	095D1502 _H	0B5D1502 _H				
XC888CM-6FFA 3V3	-	095D1503 _H	0B5D1503 _H				
XC886C-6FFA 3V3	-	095D1542 _H	0B5D1542 _H				
XC888C-6FFA 3V3	-	095D1543 _H	0B5D1543 _H				

Table 36 Chip Identification Number



Electrical Parameters

4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC886/888 can be subjected to without permanent damage.

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T _A	-40	125	°C	under bias
Storage temperature	T _{ST}	-65	150	°C	1)
Junction temperature	TJ	-40	150	°C	under bias ¹⁾
Voltage on power supply pin with respect to $V_{\rm SS}$	V _{DDP}	-0.5	6	V	1)
Voltage on any pin with respect to $V_{\rm SS}$	V _{IN}	-0.5	V _{DDP} + 0.5 or max. 6	V	whichever is lower ¹⁾
Input current on any pin during overload condition	I _{IN}	-10	10	mA	1)
Absolute sum of all input currents during overload condition	$\Sigma I_{IN} $	_	50	mA	1)

Table 4-1	Absolute	Maximum	Rating	Parameters
-----------	----------	---------	--------	-------------------

1) Not subjected to production test, verified by design/characterization.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.



Electrical Parameters

Table 42 Power Down Current (Operating Conditions apply; $V_{DDP} = 5V$ range					
Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. ¹⁾	max. ²⁾		
$V_{\rm DDP}$ = 5V Range		·			
Power-Down Mode	I _{PDP}	1	10	μA	$T_{A} = + 25 \ ^{\circ}C^{3)4)}$
		-	30	μA	$T_{A} = + 85 \ ^{\circ}C^{4)5)}$
1) The typical V_{res} values are measured at $V_{\text{res}} = 5.0 \text{ V}$					

Power Down Current (Operating Conditions apply: U able 10 - E (1 - C)

1) The typical I_{PDP} values are measured at V_{DDP} = 5.0 V.

2) The maximum I_{PDP} values are measured at V_{DDP} = 5.5 V.

3) I_{PDP} has a maximum value of 200 μ A at T_A = + 125 °C.

4) I_{PDP} is measured with: RESET = V_{DDP} , V_{AGND} = V_{SS} , RXD/INT0 = V_{DDP} ; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.

5) Not subjected to production test, verified by design/characterization.



Electrical Parameters

4.3.7 SSC Master Mode Timing

Table 51 provides the characteristics of the SSC timing in the XC886/888.

Table 51	SSC Master Mode Timing	(Operating Conditions	apply; $CL = 50 pF$)
	U		

Parameter	Symbol		Limit Values		Unit	Test
			min.	max.		Conditions
SCLK clock period	t ₀	CC	2*T _{SSC}	_	ns	1)2)
MTSR delay from SCLK	t ₁	CC	0	8	ns	2)
MRST setup to SCLK 飞∟	<i>t</i> ₂	SR	24	-	ns	2)
MRST hold from SCLK	<i>t</i> ₃	SR	0	-	ns	2)

1) $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$. When $f_{CPU} = 24$ MHz, $t_0 = 83.3$ ns. T_{CPU} is the CPU clock period.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.



Figure 52 SSC Master Mode Timing