# Infineon Technologies - SAK-XC888CM-8FFI 5V AC Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XC800 |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, SSI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.75K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | PG-TQFP-64 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/sak-xc888cm-8ffi-5v-ac |

Never stop thinking

# 8-Bit

# XC886/888CLM

## 8-Bit Single Chip Microcontroller

## Data Sheet

V1.2 2009-07

Microcontrollers

### XC886/888 Variant Devices

The XC886/888 product family features devices with different configurations, program memory sizes, package options, power supply voltage, temperature and quality profiles (Automotive or Industrial), to offer cost-effective solutions for different application requirements.

The list of XC886/888 device configurations are summarized in **Table 1**. For each configuration, 2 types of packages are available:

- PG-TQFP-48, which is denoted by XC886 and;
- PG-TQFP-64, which is denoted by XC888.

**Table 1 Device Configuration**

| Device Name | CAN Module | LIN BSL Support | MDU Module |
|---|---|---|---|
| XC886/888 | No | No | No |
| XC886/888C | Yes | No | No |
| XC886/888CM | Yes | No | Yes |
| XC886/888LM | No | Yes | Yes |
| XC886/888CLM | Yes | Yes | Yes |

*Note: For variants with LIN BSL support, only LIN BSL is available regardless of the availability of the CAN module.*

From these 10 different combinations of configuration and package type, each are further made available in many sales types, which are grouped according to device type, program memory sizes, power supply voltage, temperature and quality profile (Automotive or Industrial), as shown in **Table 2**.

**Table 2 Device Profile**

| Sales Type | Device Type | Program Memory (Kbytes) | Power Supply (V) | Temp-erature (°C) | Quality Profile |
|---|---|---|---|---|---|
| SAK-XC886*/888*-8FFA 5V | Flash | 32 | 5.0 | -40 to 125 | Automotive |
| SAK-XC886*/888*-6FFA 5V | Flash | 24 | 5.0 | -40 to 125 | Automotive |
| SAF-XC886*/888*-8FFA 5V | Flash | 32 | 5.0 | -40 to 85 | Automotive |
| SAF-XC886*/888*-6FFA 5V | Flash | 24 | 5.0 | -40 to 85 | Automotive |
| SAF-XC886*/888*-8FFI 5V | Flash | 32 | 5.0 | -40 to 85 | Industrial |
| SAF-XC886*/888*-6FFI 5V | Flash | 24 | 5.0 | -40 to 85 | Industrial |

## 2.3 Pin Configuration

The pin configuration of the XC886, which is based on the PG-TQFP-48 package, is shown in **Figure 4**, while that of the XC888, which is based on the PG-TQFP-64 package, is shown in **Figure 5**.

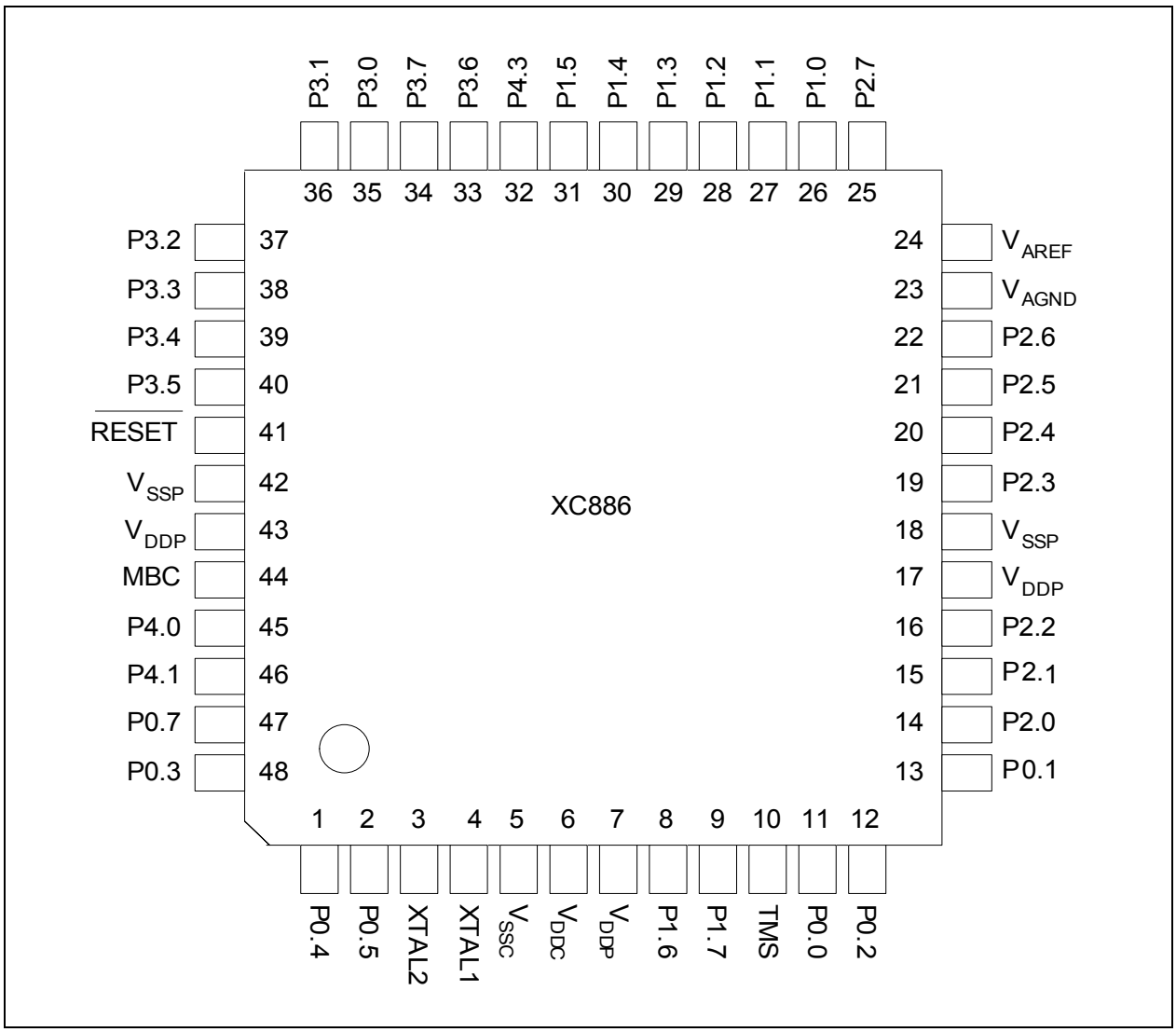



**Figure 4 XC886 Pin Configuration, PG-TQFP-48 Package** (top view)

**Table 3 Pin Definitions and Functions** (cont'd)

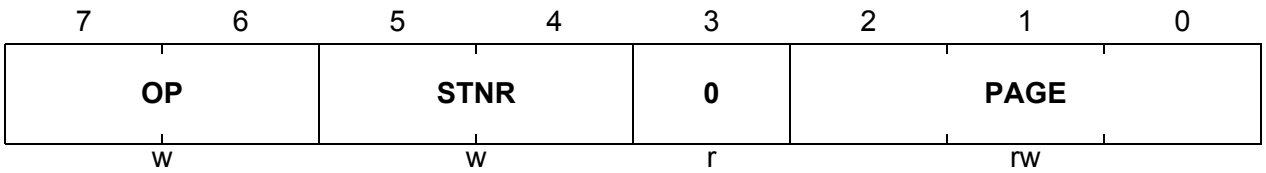
| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function | |
|---|---|---|---|---|---|
| P0.4 | 1/64 | | Hi-Z | MTSR_1 | SSC Master Transmit Output/ Slave Receive Input |
| | | | | CC62_1 | Input/Output of Capture/Compare channel 2 |
| | | | | TXD1_0 | UART1 Transmit Data Output/Clock Output |
| P0.5 | 2/1 | | Hi-Z | MRST_1 | SSC Master Receive Input/Slave Transmit Output |
| | | | | EXINT0_0 | External Interrupt Input 0 |
| | | | | T2EX1_1 | Timer 21 External Trigger Input |
| | | | | RXD1_0 | UART1 Receive Data Input |
| | | | | COUT62_1 | Output of Capture/Compare channel 2 |
| P0.6 | –/2 | | PU | GPIO | |
| P0.7 | 47/62 | | PU | CLKOUT_1 | Clock Output |

**Table 3 Pin Definitions and Functions** (cont'd)

| Symbol | Pin Number (TQFP-48/64) | Type | Reset State | Function | |
|---|---|---|---|---|---|
| **P4** | | I/O | | **Port 4**<br>Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, Timer 21 and MultiCAN. | |
| P4.0 | 45/59 | | Hi-Z | RXDC0_3<br>CC60_1 | MultiCAN Node 0 Receiver Input<br>Output of Capture/Compare channel 0 |
| P4.1 | 46/60 | | Hi-Z | TXDC0_3<br><br>COUT60_1 | MultiCAN Node 0 Transmitter Output<br>Output of Capture/Compare channel 0 |
| P4.2 | –/61 | | PU | EXINT6_1<br>T21_0 | External Interrupt Input 6<br>Timer 21 Input |
| P4.3 | 32/40 | | Hi-Z | EXF21_1<br>COUT63_2 | Timer 21 External Flag Output<br>Output of Capture/Compare channel 3 |
| P4.4 | –/45 | | Hi-Z | CCPOS0_3<br>T0_0<br>CC61_4 | CCU6 Hall Input 0<br>Timer 0 Input<br>Output of Capture/Compare channel 1 |
| P4.5 | –/46 | | Hi-Z | CCPOS1_3<br>T1_0<br>COUT61_2 | CCU6 Hall Input 1<br>Timer 1 Input<br>Output of Capture/Compare channel 1 |
| P4.6 | –/47 | | Hi-Z | CCPOS2_3<br>T2_0<br>CC62_2 | CCU6 Hall Input 2<br>Timer 2 Input<br>Output of Capture/Compare channel 2 |
| P4.7 | –/48 | | Hi-Z | $\overline{\text{CTRAP}}$_3<br>COUT62_2 | CCU6 Trap Input<br>Output of Capture/Compare channel 2 |

The page register has the following definition:

**MOD_PAGE**
**Page Register for module MOD** **Reset Value: $00_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **PAGE** | [2:0] | rw | **Page Bits**<br>When written, the value indicates the new page.<br>When read, the value indicates the currently active page. |
| **STNR** | [5:4] | w | **Storage Number**<br>This number indicates which storage bit field is the target of the operation defined by bit field OP.<br>If OP = $10_B$,<br>the contents of PAGE are saved in STx before being overwritten with the new value.<br>If OP = $11_B$,<br>the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored.<br><br>00 ST0 is selected.<br>01 ST1 is selected.<br>10 ST2 is selected.<br>11 ST3 is selected. |

| Field | Bits | Type | Description |
|---|---|---|---|
| **OP** | [7:6] | w | **Operation**<br>0X Manual page mode. The value of STNR is ignored and PAGE is directly written.<br>10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR.<br>11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR. |
| **0** | 3 | r | **Reserved**<br>Returns 0 if read; should be written with 0. |

### 3.2.3 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected bits (i.e., protected bits) using the PASSWD register. When the bit field MODE is $11_B$, writing $10011_B$ to the bit field PASS opens access to writing of all protected bits, and writing $10101_B$ to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with $98_H$ or $A8_H$. It can only be changed when bit field PASS is written with $11000_B$, for example, writing $D0_H$ to PASSWD register disables the bit protection scheme.

Note that access is opened for maximum 32 CCLKs if the “close access” password is not written. If “open access” password is written again before the end of 32 CCLK cycles, there will be a recount of 32 CCLK cycles. The protected bits include the N- and K-Divider bits, NDIV and KDIV; the Watchdog Timer enable bit, WDTEN; and the power-down and slow-down enable bits, PD and SD.

**Table 14 CCU6 Register Overview** (cont'd)

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $FE_H$ | **CCU6_CMPSTATL Reset: $00_H$** Compare State Register Low | Bit Field | 0 | CC63 ST | CC POS2 | CC POS1 | CC POS0 | CC62 ST | CC61 ST | CC60 ST |
| | | Type | r | rh | rh | rh | rh | rh | rh | rh |
| $FF_H$ | **CCU6_CMPSTATH Reset: $00_H$** Compare State Register High | Bit Field | T13IM | COUT 63PS | COUT 62PS | CC62 PS | COUT 61PS | CC61 PS | COUT 60PS | CC60 PS |
| | | Type | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |

### 3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

**Table 15 UART1 Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 1 | | | | | | | | | | |
| **$C8_H$** | **SCON Reset: $00_H$** Serial Channel Control Register | Bit Field | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |
| | | Type | rw | rw | rw | rw | rw | rwh | rwh | rwh |
| $C9_H$ | **SBUF Reset: $00_H$** Serial Data Buffer Register | Bit Field | VAL | | | | | | | |
| | | Type | rwh | | | | | | | |
| $CA_H$ | **BCON Reset: $00_H$** Baud Rate Control Register | Bit Field | 0 | | | | BRPRE | | | R |
| | | Type | r | | | | rw | | | rw |
| $CB_H$ | **BG Reset: $00_H$** Baud Rate Timer/Reload Register | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rwh | | | | | | | |
| $CC_H$ | **FDCON Reset: $00_H$** Fractional Divider Control Register | Bit Field | 0 | | | | | NDOV | FDM | FDEN |
| | | Type | r | | | | | rwh | rw | rw |
| $CD_H$ | **FDSTEP Reset: $00_H$** Fractional Divider Reload Register | Bit Field | STEP | | | | | | | |
| | | Type | rw | | | | | | | |
| $CE_H$ | **FDRES Reset: $00_H$** Fractional Divider Result Register | Bit Field | RESULT | | | | | | | |
| | | Type | rh | | | | | | | |

### 3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 16 SSC Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 | | | | | | | | | | |
| $A9_H$ | **SSC_PISEL** **Reset: $00_H$** Port Input Select Register | Bit Field | 0 | | | | | CIS | SIS | MIS |
| | | Type | r | | | | | rw | rw | rw |
| $AA_H$ | **SSC_CONL** **Reset: $00_H$** Control Register Low Programming Mode | Bit Field | LB | PO | PH | HB | BM | | | |
| | | Type | rw | rw | rw | rw | rw | | | |
| $AA_H$ | **SSC_CONL** **Reset: $00_H$** Control Register Low Operating Mode | Bit Field | 0 | | | | BC | | | |
| | | Type | r | | | | rh | | | |
| $AB_H$ | **SSC_CONH** **Reset: $00_H$** Control Register High Programming Mode | Bit Field | EN | MS | 0 | AREN | BEN | PEN | REN | TEN |
| | | Type | rw | rw | r | rw | rw | rw | rw | rw |
| $AB_H$ | **SSC_CONH** **Reset: $00_H$** Control Register High Operating Mode | Bit Field | EN | MS | 0 | BSY | BE | PE | RE | TE |
| | | Type | rw | rw | r | rh | rwh | rwh | rwh | rwh |
| $AC_H$ | **SSC_TBL** **Reset: $00_H$** Transmitter Buffer Register Low | Bit Field | TB_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |
| $AD_H$ | **SSC_RBL** **Reset: $00_H$** Receiver Buffer Register Low | Bit Field | RB_VALUE | | | | | | | |
| | | Type | rh | | | | | | | |
| $AE_H$ | **SSC_BRL** **Reset: $00_H$** Baud Rate Timer Reload Register Low | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |
| $AF_H$ | **SSC_BRH** **Reset: $00_H$** Baud Rate Timer Reload Register High | Bit Field | BR_VALUE | | | | | | | |
| | | Type | rw | | | | | | | |

### 3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 17 CAN Register Overview**

| Addr | Register Name | Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| RMAP = 0 | | | | | | | | | | |
| **$D8_H$** | **ADCON** **Reset: $00_H$** CAN Address/Data Control Register | Bit Field | V3 | V2 | V1 | V0 | AUAD | | BSY | RWEN |
| | | Type | rw | rw | rw | rw | rw | | rh | rw |
| $D9_H$ | **ADL** **Reset: $00_H$** CAN Address Register Low | Bit Field | CA9 | CA8 | CA7 | CA6 | CA5 | CA4 | CA3 | CA2 |
| | | Type | rwh | rwh | rwh | rwh | rwh | rwh | rwh | rwh |
| $DA_H$ | **ADH** **Reset: $00_H$** CAN Address Register High | Bit Field | 0 | | | | CA13 | CA12 | CA11 | CA10 |
| | | Type | r | | | | rwh | rwh | rwh | rwh |

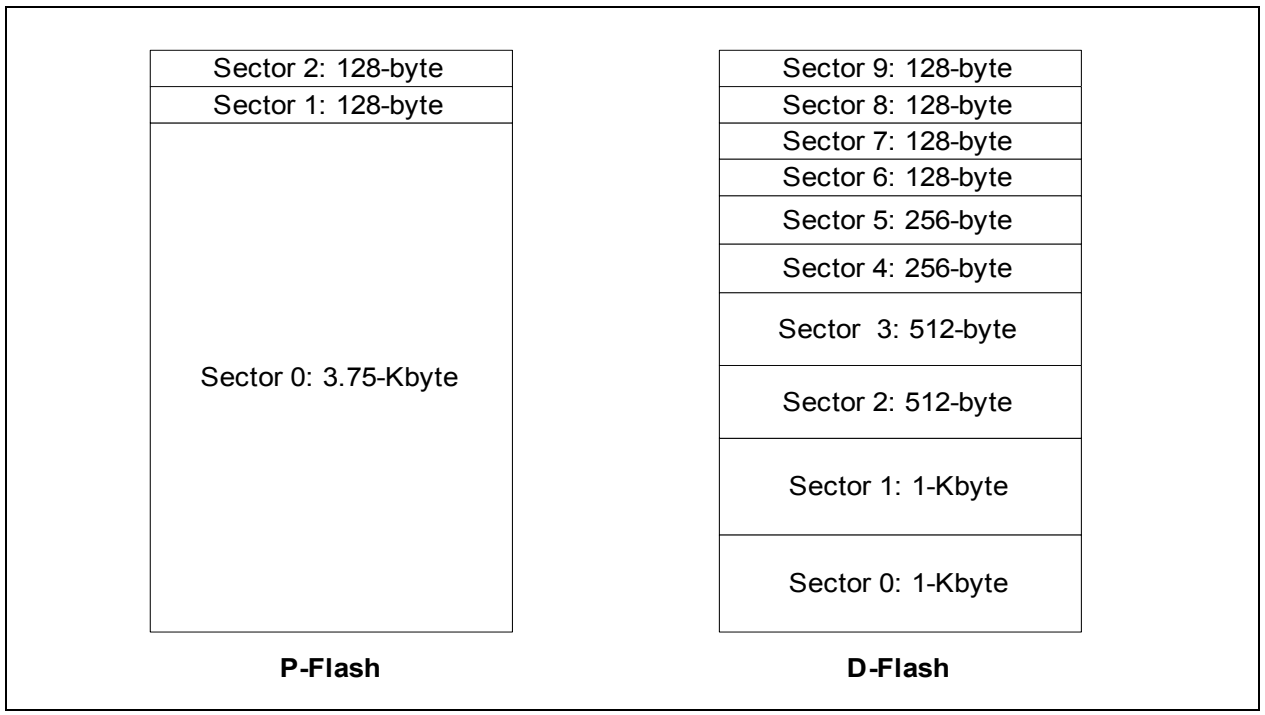



**Figure 11 Flash Bank Sectorization**

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

### 3.3.2 Parallel Read Access of P-Flash

To enhance system performance, the P-Flash banks are configured for parallel read to allow two bytes of linear code to be read in 4 x CCLK cycles, compared to 6 x CCLK cycles if serial read is performed. This is achieved by reading two bytes in parallel from a P-Flash bank pair within the 3 x CCLK cycles access time and storing them in a cache. Subsequent read from the cache by the CPU does not require a wait state and can be completed within 1 x CCLK cycle. The result is the average instruction fetch time from the P-Flash banks is reduced and thus, the MIPS (Mega Instruction Per Second) of the system is increased.

However, if the parallel read feature is not desired due to certain timing constraints, it can be disabled by calling the parallel read disable subroutine.

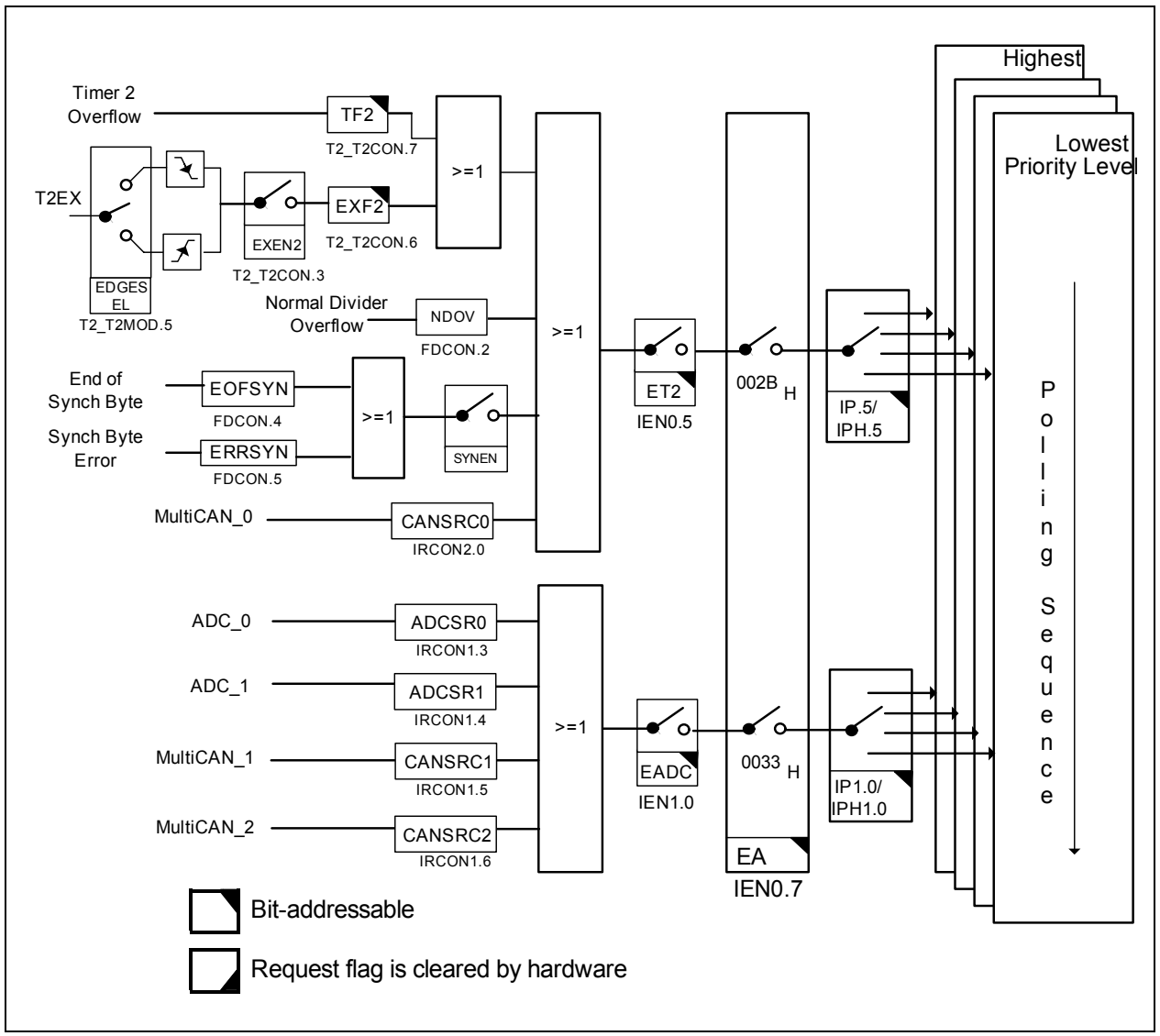



**Figure 15 Interrupt Request Sources (Part 2)**

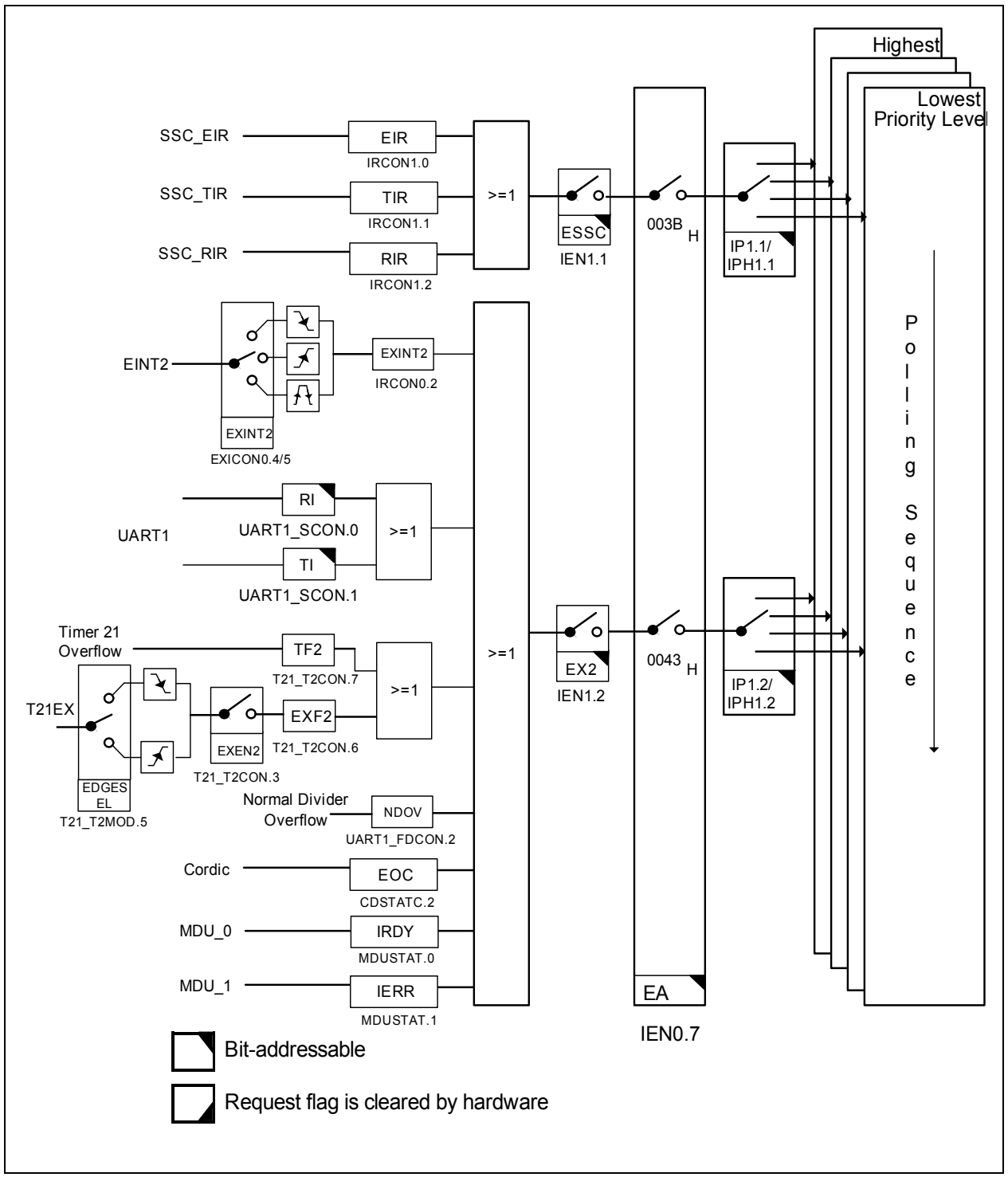



**Figure 16 Interrupt Request Sources (Part 3)**

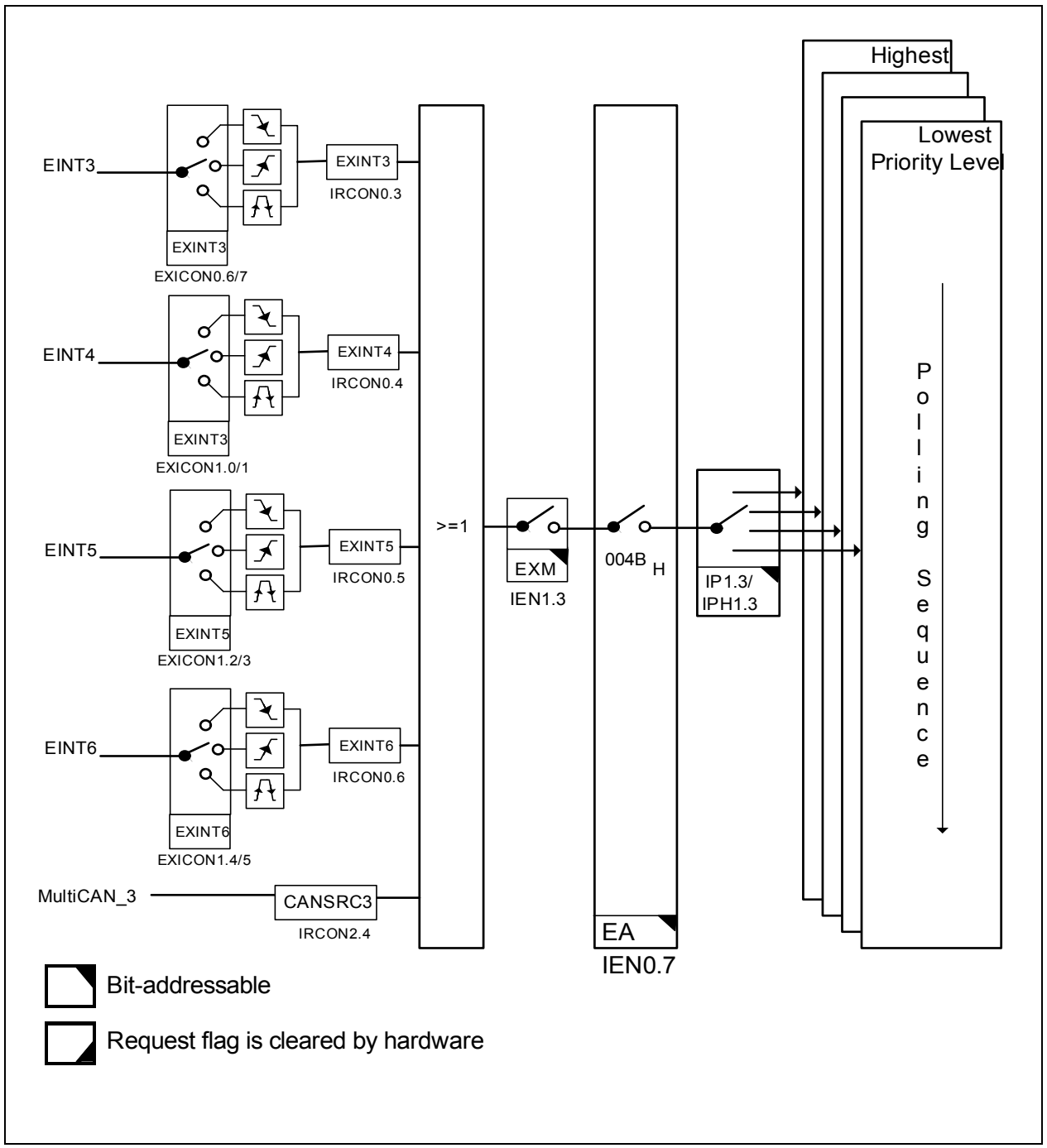



**Figure 17 Interrupt Request Sources (Part 4)**

If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for $30_H$ count, after which the system is reset (assert WDTRST).

The WDT has a “programmable window boundary” which disallows any refresh during the WDT’s count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from $0000_H$ to the value obtained from the concatenation of WDTWINB and $00_H$.

After being serviced, the WDT continues counting up from the value (<WDTREL> * $2^8$). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either $f_{PCLK}/2$ or $f_{PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period, $P_{WDT}$, between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} = \frac{2^{(1 + WDTIN \times 6)} \times (2^{16} - WDTREL \times 2^8)}{f_{PCLK}} \quad (3.4)$$

If the Window-Boundary Refresh feature of the WDT is enabled, the period $P_{WDT}$ between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 29**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.

## 3.16 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

### Features

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 8 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

**Figure 32** shows the block diagram of the SSC.

GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.

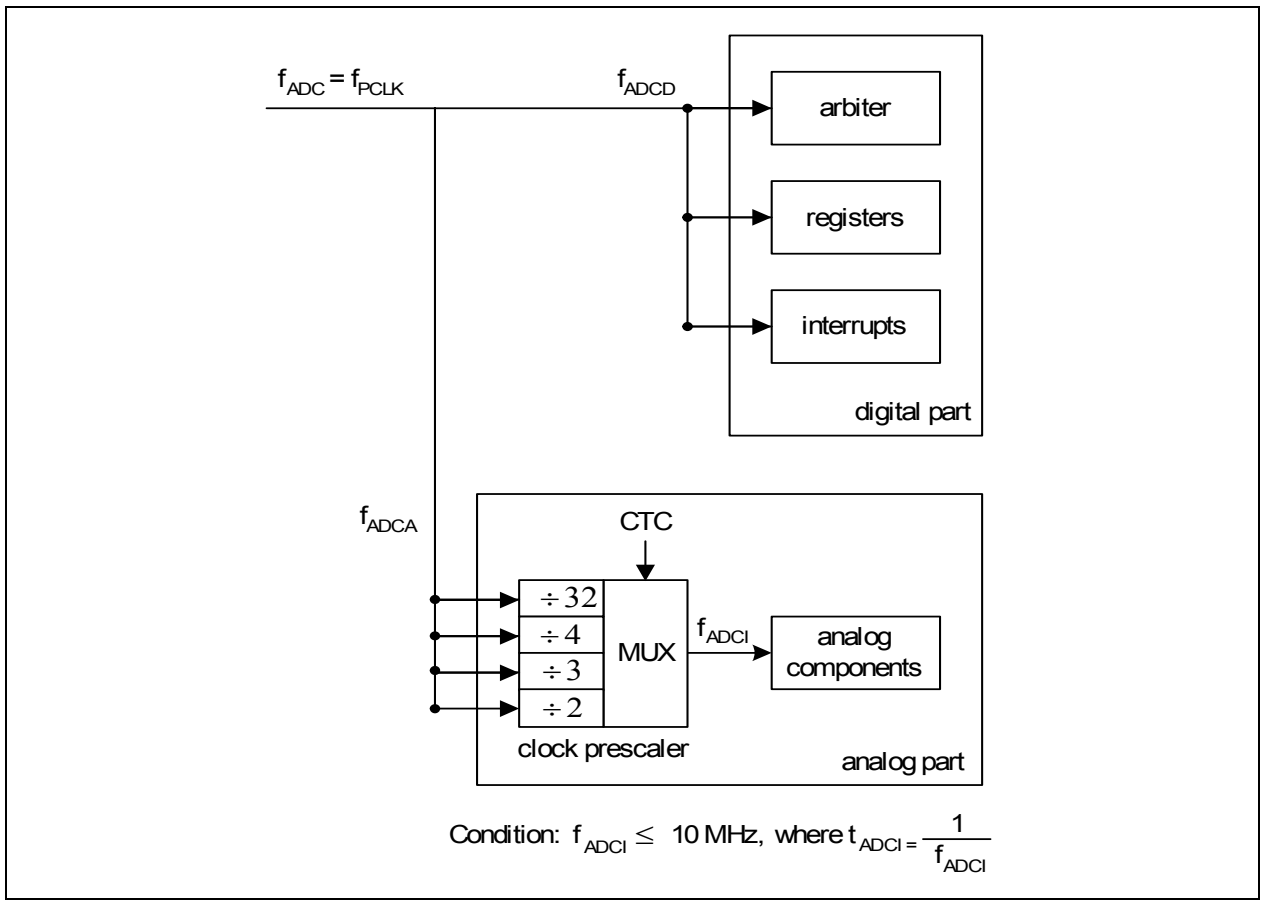



**Figure 35 ADC Clocking Scheme**

For module clock $f_{ADC}$ = 24 MHz, the analog clock $f_{ADCI}$ frequency can be selected as shown in **Table 34**.

**Table 34 $f_{ADCI}$ Frequency Selection**

| Module Clock $f_{ADC}$ | CTC | Prescaling Ratio | Analog Clock $f_{ADCI}$ |
|---|---|---|---|
| 24 MHz | $00_B$ | ÷ 2 | 12 MHz (N.A) |
| | $01_B$ | ÷ 3 | 8 MHz |
| | $10_B$ | ÷ 4 | 6 MHz |
| | $11_B$ (default) | ÷ 32 | 750 kHz |

As $f_{ADCI}$ cannot exceed 10 MHz, bit field CTC should not be set to $00_B$ when $f_{ADC}$ is 24 MHz. During slow-down mode where $f_{ADC}$ may be reduced to 12 MHz, 6 MHz etc., CTC can be set to $00_B$ as long as the divided analog clock $f_{ADCI}$ does not exceed 10 MHz.

**Table 36 Chip Identification Number** (cont'd)

| Product Variant | Chip Identification Number | | |
|---|---|---|---|
| | AA-Step | AB-Step | AC-Step |
| XC886LM-6RFA 3V3 | $22411522_H$ | - | - |
| XC888LM-6RFA 3V3 | $22411523_H$ | - | - |
| XC886CM-8RFA 3V3 | $22480502_H$ | - | - |
| XC888CM-8RFA 3V3 | $22480503_H$ | - | - |
| XC886C-8RFA 3V3 | $22480542_H$ | - | - |
| XC888C-8RFA 3V3 | $22480543_H$ | - | - |
| XC886-8RFA 3V3 | $22480562_H$ | - | - |
| XC888-8RFA 3V3 | $22480563_H$ | - | - |
| XC886CM-6RFA 3V3 | $22491502_H$ | - | - |
| XC888CM-6RFA 3V3 | $22491503_H$ | - | - |
| XC886C-6RFA 3V3 | $22491542_H$ | - | - |
| XC888C-6RFA 3V3 | $22491543_H$ | - | - |
| XC886-6RFA 3V3 | $22491562_H$ | - | - |
| XC888-6RFA 3V3 | $22491563_H$ | - | - |
| XC886CLM-8RFA 5V | $22800502_H$ | - | - |
| XC888CLM-8RFA 5V | $22800503_H$ | - | - |
| XC886LM-8RFA 5V | $22800522_H$ | - | - |
| XC888LM-8RFA 5V | $22800523_H$ | - | - |
| XC886CLM-6RFA 5V | $22811502_H$ | - | - |
| XC888CLM-6RFA 5V | $22811503_H$ | - | - |
| XC886LM-6RFA 5V | $22811522_H$ | - | - |
| XC888LM-6RFA 5V | $22811523_H$ | - | - |
| XC886CM-8RFA 5V | $22880502_H$ | - | - |
| XC888CM-8RFA 5V | $22880503_H$ | - | - |
| XC886C-8RFA 5V | $22880542_H$ | - | - |
| XC888C-8RFA 5V | $22880543_H$ | - | - |
| XC886-8RFA 5V | $22880562_H$ | - | - |
| XC888-8RFA 5V | $22880563_H$ | - | - |
| XC886CM-6RFA 5V | $22891502_H$ | - | - |

**Table 36 Chip Identification Number** (cont'd)

| Product Variant | Chip Identification Number | | |
|---|---|---|---|
| | **AA-Step** | **AB-Step** | **AC-Step** |
| XC888CM-6RFA 5V | $22891503_H$ | - | - |
| XC886C-6RFA 5V | $22891542_H$ | - | - |
| XC888C-6RFA 5V | $22891543_H$ | - | - |
| XC886-6RFA 5V | $22891562_H$ | - | - |
| XC888-6RFA 5V | $22891563_H$ | - | - |

## 4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

### 4.2.1 Input/Output Characteristics

**Table 38** provides the characteristics of the input/output pins of the XC886/888.

**Table 38 Input/Output Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| **$V_{DDP}$ = 5 V Range** | | | | | | |
| Output low voltage | $V_{OL}$ | CC | – | 1.0 | V | $I_{OL}$ = 15 mA |
| | | | – | 1.0 | V | $I_{OL}$ = 5 mA, current into all pins > 60 mA |
| | | | – | 0.4 | V | $I_{OL}$ = 5 mA, current into all pins ≤ 60 mA |
| Output high voltage | $V_{OH}$ | CC | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -15 mA |
| | | | $V_{DDP}$ - 1.0 | – | V | $I_{OH}$ = -5 mA, current from all pins > 60 mA |
| | | | $V_{DDP}$ - 0.4 | – | V | $I_{OH}$ = -5 mA, current from all pins ≤ 60 mA |
| Input low voltage on port pins (all except P0.0 & P0.1) | $V_{ILP}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on P0.0 & P0.1 | $V_{ILP0}$ | SR | -0.2 | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on $\overline{\text{RESET}}$ pin | $V_{ILR}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input low voltage on TMS pin | $V_{ILT}$ | SR | – | 0.3 × $V_{DDP}$ | V | CMOS Mode |
| Input high voltage on port pins (all except P0.0 & P0.1) | $V_{IHP}$ | SR | 0.7 × $V_{DDP}$ | – | V | CMOS Mode |
| Input high voltage on P0.0 & P0.1 | $V_{IHP0}$ | SR | 0.7 × $V_{DDP}$ | $V_{DDP}$ | V | CMOS Mode |

# 5 Package and Quality Declaration

**Chapter 5** provides the information of the XC886/888 package and reliability section.

## 5.1 Package Parameters

**Table 1** provides the thermal characteristics of the package used in XC886 and XC888.

**Table 1 Thermal Characteristics of the Packages**

| Parameter | Symbol | | Limit Values | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| **PG-TQFP-48 (XC886)** | | | | | | |
| Thermal resistance junction case | $R_{TJC}$ | CC | - | 13 | K/W | 1)2) |
| Thermal resistance junction lead | $R_{TJL}$ | CC | - | 32.5 | K/W | 1)2) |
| **PG-TQFP-64 (XC888)** | | | | | | |
| Thermal resistance junction case | $R_{TJC}$ | CC | - | 12.6 | K/W | 1)2) |
| Thermal resistance junction lead | $R_{TJL}$ | CC | - | 33.4 | K/W | 1)2) |

1) The thermal resistances between the case and the ambient ($R_{TCA}$) , the lead and the ambient ($R_{TLA}$) are to be combined with the thermal resistances between the junction and the case ($R_{TJC}$), the junction and the lead ($R_{TJL}$) given above, in order to calculate the total thermal resistance between the junction and the ambient ($R_{TJA}$). The thermal resistances between the case and the ambient ($R_{TCA}$), the lead and the ambient ($R_{TLA}$) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the $R_{TJA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{TJA}$ can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two thermal resistances (junction lead and lead ambient), or
b) by taking all four resistances into account, depending on the precision needed.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.