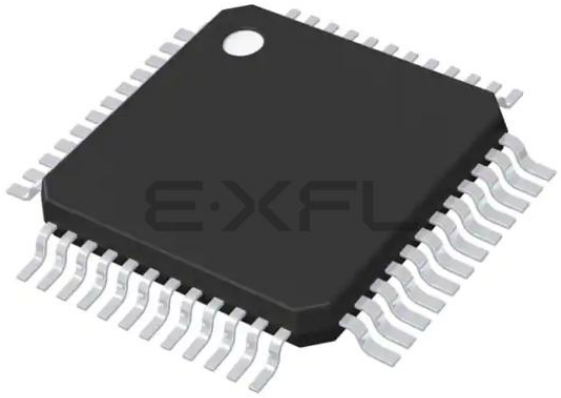

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XC800
Core Size	8-Bit
Speed	24MHz
Connectivity	SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.75K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	PG-TQFP-48
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc8868ffi5vackxuma1

Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - PLL loss-of-lock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINT0
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Six ports
  - Up to 48 pins as digital I/O
  - 8 pins as digital/analog input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- Software libraries to support floating point and MDU calculations
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Capture/compare unit for PWM signal generation (CCU6)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 12-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Packages:
  - PG-TQFP-48
  - PG-TQFP-64
- Temperature range T_A:
  - SAF (-40 to 85 °C)
  - SAK (-40 to 125 °C)

Table 3 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (TQFP-48/64)	Type	Reset State	Function	
P5		I/O		**Port 5** Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1 and JTAG.	
P5.0	–/8		PU	EXINT1_1	External Interrupt Input 1
P5.1	–/9		PU	EXINT2_1	External Interrupt Input 2
P5.2	–/12		PU	RXD_2	UART Receive Data Input
P5.3	–/13		PU	TXD_2	UART Transmit Data Output/Clock Output
P5.4	–/14		PU	RXDO_2	UART Transmit Data Output
P5.5	–/15		PU	TDO_2 TXD1_2	JTAG Serial Data Output UART1 Transmit Data Output/ Clock Output
P5.6	–/19		PU	TCK_2 RXDO1_2	JTAG Clock Input UART1 Transmit Data Output
P5.7	–/20		PU	TDI_2 RXD1_2	JTAG Serial Data Input UART1 Receive Data Input

3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range 80_H to FF_H. All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

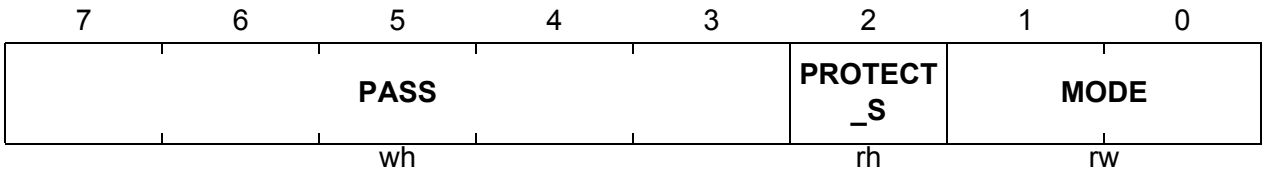
3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range 80_H to FF_H, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address $8F_H$. To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 8**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

3.2.3.1 Password Register

PASSWD
Password Register **Reset Value: 07_H**



Field	Bits	Type	Description
MODE	[1:0]	rw	**Bit Protection Scheme Control Bits** 00 Scheme disabled - direct access to the protected bits is allowed. 11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default) Others:Scheme Enabled. These two bits cannot be written directly. To change the value between 11_B and 00_B, the bit field PASS must be written with 11000_B; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	**Bit Protection Signal Status Bit** This bit shows the status of the protection. 0 Software is able to write to all protected bits. 1 Software is unable to write to any protected bits.
PASS	[7:3]	wh	**Password Bits** The Bit Protection Scheme only recognizes three patterns. 11000_B Enables writing of the bit field MODE. 10011_B Opens access to writing of all protected bits. 10101_B Closes access to writing of all protected bits

Table 9 WDT Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
BE_H	**WDTL** **Reset: 00_H** Watchdog Timer Register Low	Bit Field	WDT							
		Type	rh							
BF_H	**WDTH** **Reset: 00_H** Watchdog Timer Register High	Bit Field	WDT							
		Type	rh							

3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

Table 10 Port Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0										
$B2_H$	**PORT_PAGE** **Reset: 00_H** Page Register	Bit Field	OP		STNR		0	PAGE		
		Type	w		w		r	rw		
RMAP = 0, PAGE 0										
80_H	**P0_DATA** **Reset: 00_H** P0 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_DIR** **Reset: 00_H** P0 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_DATA** **Reset: 00_H** P1 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_DIR** **Reset: 00_H** P1 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_DATA** **Reset: 00_H** P5 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_DIR** **Reset: 00_H** P5 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A0_H$	**P2_DATA** **Reset: 00_H** P2 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_DIR** **Reset: 00_H** P2 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_DATA** **Reset: 00_H** P3 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_DIR** **Reset: 00_H** P3 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_DATA** **Reset: 00_H** P4 Data Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_DIR** **Reset: 00_H** P4 Direction Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 10 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP = 0, PAGE 1										
80_H	**P0_PUDSEL Reset: FF_H** P0 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_PUDEN Reset: $C4_H$** P0 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_PUDSEL Reset: FF_H** P1 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_PUDEN Reset: FF_H** P1 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_PUDSEL Reset: FF_H** P5 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
93_H	**P5_PUDEN Reset: FF_H** P5 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A0_H$	**P2_PUDSEL Reset: FF_H** P2 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$A1_H$	**P2_PUDEN Reset: 00_H** P2 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B0_H$	**P3_PUDSEL Reset: BF_H** P3 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$B1_H$	**P3_PUDEN Reset: 40_H** P3 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C8_H$	**P4_PUDSEL Reset: FF_H** P4 Pull-Up/Pull-Down Select Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
$C9_H$	**P4_PUDEN Reset: 04_H** P4 Pull-Up/Pull-Down Enable Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
RMAP = 0, PAGE 2										
80_H	**P0_ALTSEL0 Reset: 00_H** P0 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
86_H	**P0_ALTSEL1 Reset: 00_H** P0 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
90_H	**P1_ALTSEL0 Reset: 00_H** P1 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
91_H	**P1_ALTSEL1 Reset: 00_H** P1 Alternate Select 1 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw
92_H	**P5_ALTSEL0 Reset: 00_H** P5 Alternate Select 0 Register	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
		Type	rw	rw	rw	rw	rw	rw	rw	rw

Table 18 OCDS Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
EC_H	**MMWR2** **Reset: 00_H** Monitor Work Register 2	Bit Field	MMWR2							
		Type	rw							

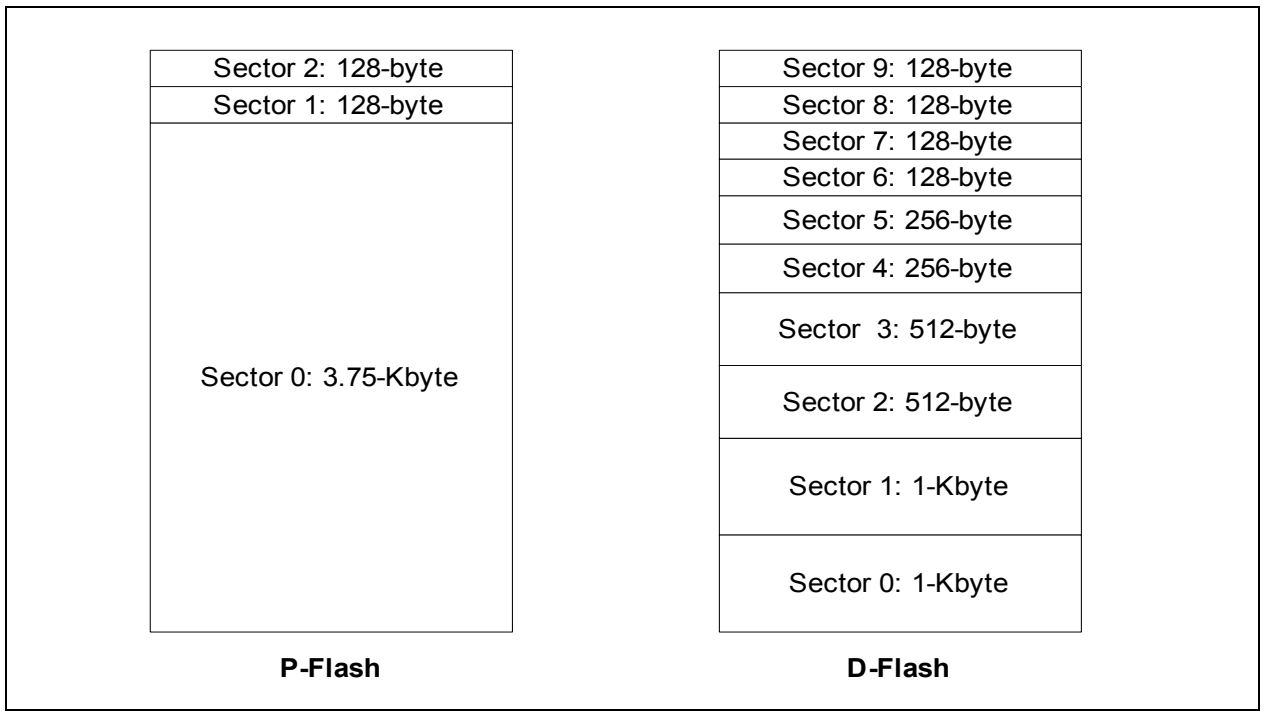


Figure 11 Flash Bank Sectorization

The internal structure of each Flash bank represents a sector architecture for flexible erase capability. The minimum erase width is always a complete sector, and sectors can be erased separately or in parallel. Contrary to standard EPROMs, erased Flash memory cells contain 0s.

The D-Flash bank is divided into more physical sectors for extended erasing and reprogramming capability; even numbers for each sector size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.

3.3.2 Parallel Read Access of P-Flash

To enhance system performance, the P-Flash banks are configured for parallel read to allow two bytes of linear code to be read in 4 x CCLK cycles, compared to 6 x CCLK cycles if serial read is performed. This is achieved by reading two bytes in parallel from a P-Flash bank pair within the 3 x CCLK cycles access time and storing them in a cache. Subsequent read from the cache by the CPU does not require a wait state and can be completed within 1 x CCLK cycle. The result is the average instruction fetch time from the P-Flash banks is reduced and thus, the MIPS (Mega Instruction Per Second) of the system is increased.

However, if the parallel read feature is not desired due to certain timing constraints, it can be disabled by calling the parallel read disable subroutine.

3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC886/888 interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in **Table 20**.

Table 20 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC886/888	Enable Bit	SFR
NMI	0073_H	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash NMI	NMIFLASH	
		VDDC Prewarning NMI	NMIVDD	
		VDDP Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003_H	External Interrupt 0	EX0	IEN0
XINTR1	$000B_H$	Timer 0	ET0	
XINTR2	0013_H	External Interrupt 1	EX1	
XINTR3	$001B_H$	Timer 1	ET1	
XINTR4	0023_H	UART	ES	
XINTR5	$002B_H$	T2	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		
		LIN		

Table 20 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC886/888	Enable Bit	SFR
XINTR6	0033_H	MultiCAN Nodes 1 and 2	EADC	IEN1
		ADC[1:0]		
XINTR7	$003B_H$	SSC	ESSC	
XINTR8	0043_H	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	$004B_H$	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		MultiCAN Node 3		
XINTR10	0053_H	CCU6 INP0	ECCIP0	
		MultiCAN Node 4		
XINTR11	$005B_H$	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063_H	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	$006B_H$	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		

3.5 Parallel Ports

The XC886 has 34 port pins organized into five parallel ports, Port 0 (P0) to Port 4 (P4), while the XC888 has 48 port pins organized into six parallel ports, Port 0 (P0) to Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. Ports P0, P1, P3, P4 and P5 are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected. Port P2 is an input-only port, providing general purpose input functions, alternate input functions for the on-chip peripherals, and also analog inputs for the Analog-to-Digital Converter (ADC).

Bidirectional Port Features

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals

Input Port Features

- Configurable input driver
- Configurable pull-up/pull-down devices
- Receive of data through digital input (general purpose input)
- Alternate input for on-chip peripherals
- Analog input for ADC module

3.9 Power Saving Modes

The power saving modes of the XC886/888 provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see **Figure 27**) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

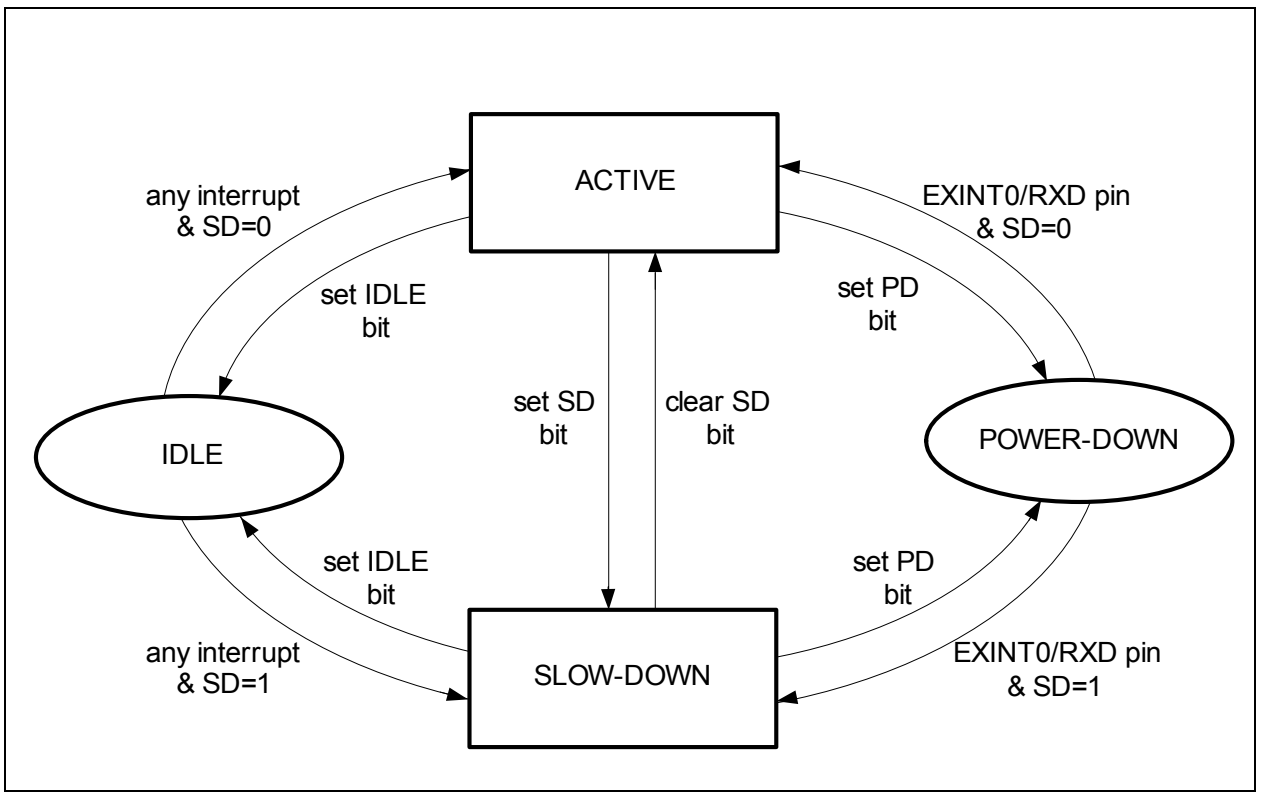


Figure 27 Transition between Power Saving Modes

3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC886/888 system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC886/888 will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

Features

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of $f_{PCLK}/2$ or $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of $f_{PCLK}/2$ or $f_{PCLK}/128$. This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. **Figure 28** shows the block diagram of the WDT unit.

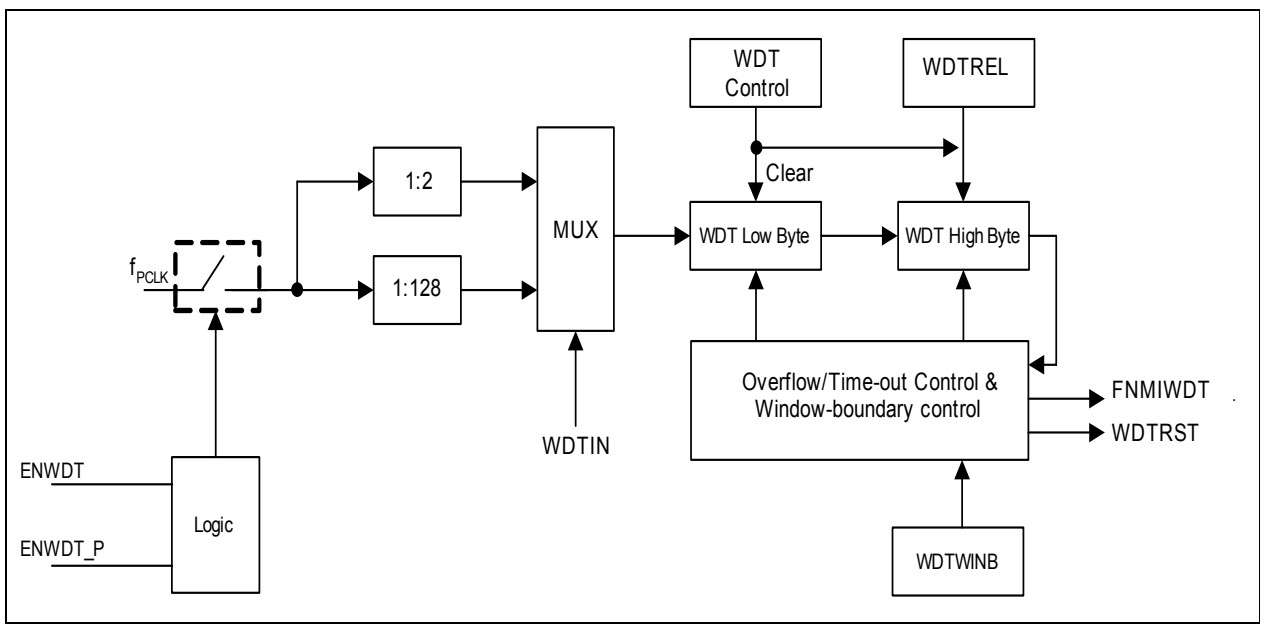


Figure 28 WDT Block Diagram

Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	**AB-Step**	**AC-Step**
XC886-6FFA 3V3	-	$095D1562_H$	$0B5D1562_H$
XC888-6FFA 3V3	-	$095D1563_H$	$0B5D1563_H$
XC886CLM-8FFA 5V	-	09900102_H	$0B900102_H$
XC888CLM-8FFA 5V	-	09900103_H	$0B900103_H$
XC886LM-8FFA 5V	-	09900122_H	$0B900122_H$
XC888LM-8FFA 5V	-	09900123_H	$0B900123_H$
XC886CLM-6FFA 5V	-	09951502_H	$0B951502_H$
XC888CLM-6FFA 5V	-	09951503_H	$0B951503_H$
XC886LM-6FFA 5V	-	09951522_H	$0B951522_H$
XC888LM-6FFA 5V	-	09951523_H	$0B951523_H$
XC886CM-8FFA 5V	-	09980102_H	$0B980102_H$
XC888CM-8FFA 5V	-	09980103_H	$0B980103_H$
XC886C-8FFA 5V	-	09980142_H	$0B980142_H$
XC888C-8FFA 5V	-	09980143_H	$0B980143_H$
XC886-8FFA 5V	-	09980162_H	$0B980162_H$
XC888-8FFA 5V	-	09980163_H	$0B980163_H$
XC886CM-6FFA 5V	-	$099D1502_H$	$0B9D1502_H$
XC888CM-6FFA 5V	-	$099D1503_H$	$0B9D1503_H$
XC886C-6FFA 5V	-	$099D1542_H$	$0B9D1542_H$
XC888C-6FFA 5V	-	$099D1543_H$	$0B9D1543_H$
XC886-6FFA 5V	-	$099D1562_H$	$0B9D1562_H$
XC888-6FFA 5V	-	$099D1563_H$	$0B9D1563_H$
ROM Devices			
XC886CLM-8RFA 3V3	22400502_H	-	-
XC888CLM-8RFA 3V3	22400503_H	-	-
XC886LM-8RFA 3V3	22400522_H	-	-
XC888LM-8RFA 3V3	22400523_H	-	-
XC886CLM-6RFA 3V3	22411502_H	-	-
XC888CLM-6RFA 3V3	22411503_H	-	-

Table 36 Chip Identification Number (cont'd)

Product Variant	Chip Identification Number		
	AA-Step	AB-Step	AC-Step
XC886LM-6RFA 3V3	22411522_H	-	-
XC888LM-6RFA 3V3	22411523_H	-	-
XC886CM-8RFA 3V3	22480502_H	-	-
XC888CM-8RFA 3V3	22480503_H	-	-
XC886C-8RFA 3V3	22480542_H	-	-
XC888C-8RFA 3V3	22480543_H	-	-
XC886-8RFA 3V3	22480562_H	-	-
XC888-8RFA 3V3	22480563_H	-	-
XC886CM-6RFA 3V3	22491502_H	-	-
XC888CM-6RFA 3V3	22491503_H	-	-
XC886C-6RFA 3V3	22491542_H	-	-
XC888C-6RFA 3V3	22491543_H	-	-
XC886-6RFA 3V3	22491562_H	-	-
XC888-6RFA 3V3	22491563_H	-	-
XC886CLM-8RFA 5V	22800502_H	-	-
XC888CLM-8RFA 5V	22800503_H	-	-
XC886LM-8RFA 5V	22800522_H	-	-
XC888LM-8RFA 5V	22800523_H	-	-
XC886CLM-6RFA 5V	22811502_H	-	-
XC888CLM-6RFA 5V	22811503_H	-	-
XC886LM-6RFA 5V	22811522_H	-	-
XC888LM-6RFA 5V	22811523_H	-	-
XC886CM-8RFA 5V	22880502_H	-	-
XC888CM-8RFA 5V	22880503_H	-	-
XC886C-8RFA 5V	22880542_H	-	-
XC888C-8RFA 5V	22880543_H	-	-
XC886-8RFA 5V	22880562_H	-	-
XC888-8RFA 5V	22880563_H	-	-
XC886CM-6RFA 5V	22891502_H	-	-

4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC886/888 can be subjected to without permanent damage.

Table 4-1 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	125	°C	under bias
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	under bias1)
Voltage on power supply pin with respect to V_{SS}	V_{DDP}	-0.5	6	V	1)
Voltage on any pin with respect to V_{SS}	V_{IN}	-0.5	V_{DDP} + 0.5 or max. 6	V	whichever is lower1)
Input current on any pin during overload condition	I_{IN}	-10	10	mA	1)
Absolute sum of all input currents during overload condition	$\Sigma\|I_{IN}\|$	–	50	mA	1)

1) Not subjected to production test, verified by design/characterization.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pin with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 38 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Input high voltage at XTAL1	V_{IHX}	SR	0.7 × V_{DDC}	V_{DDC} + 0.5	V	
Pull-up current	I_{PU}	SR	–	-5	µA	$V_{IHP,min}$
			-50	–	µA	$V_{ILP,max}$
Pull-down current	I_{PD}	SR	–	5	µA	$V_{ILP,max}$
			50	–	µA	$V_{IHP,min}$
Input leakage current	I_{OZ1}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 125°C$ [2]
Input current at XTAL1	I_{ILX}	CC	- 10	10	µA	
Overload current on any pin	I_{OV}	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	SR	–	25	mA	[3]
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[4]
Maximum current per pin (excluding V_{DDP} and V_{SS})	I_M SR	SR	–	15	mA	
Maximum current for all pins (excluding V_{DDP} and V_{SS})	$\Sigma\|I_M\|$	SR	–	90	mA	
Maximum current into V_{DDP}	I_{MVDDP}	SR	–	120	mA	[3]
Maximum current out of V_{SS}	I_{MVSS}	SR	–	120	mA	[3]

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. TMS pin and $\overline{\text{RESET}}$ pin have internal pull devices and are not included in the input leakage current characteristic.

3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

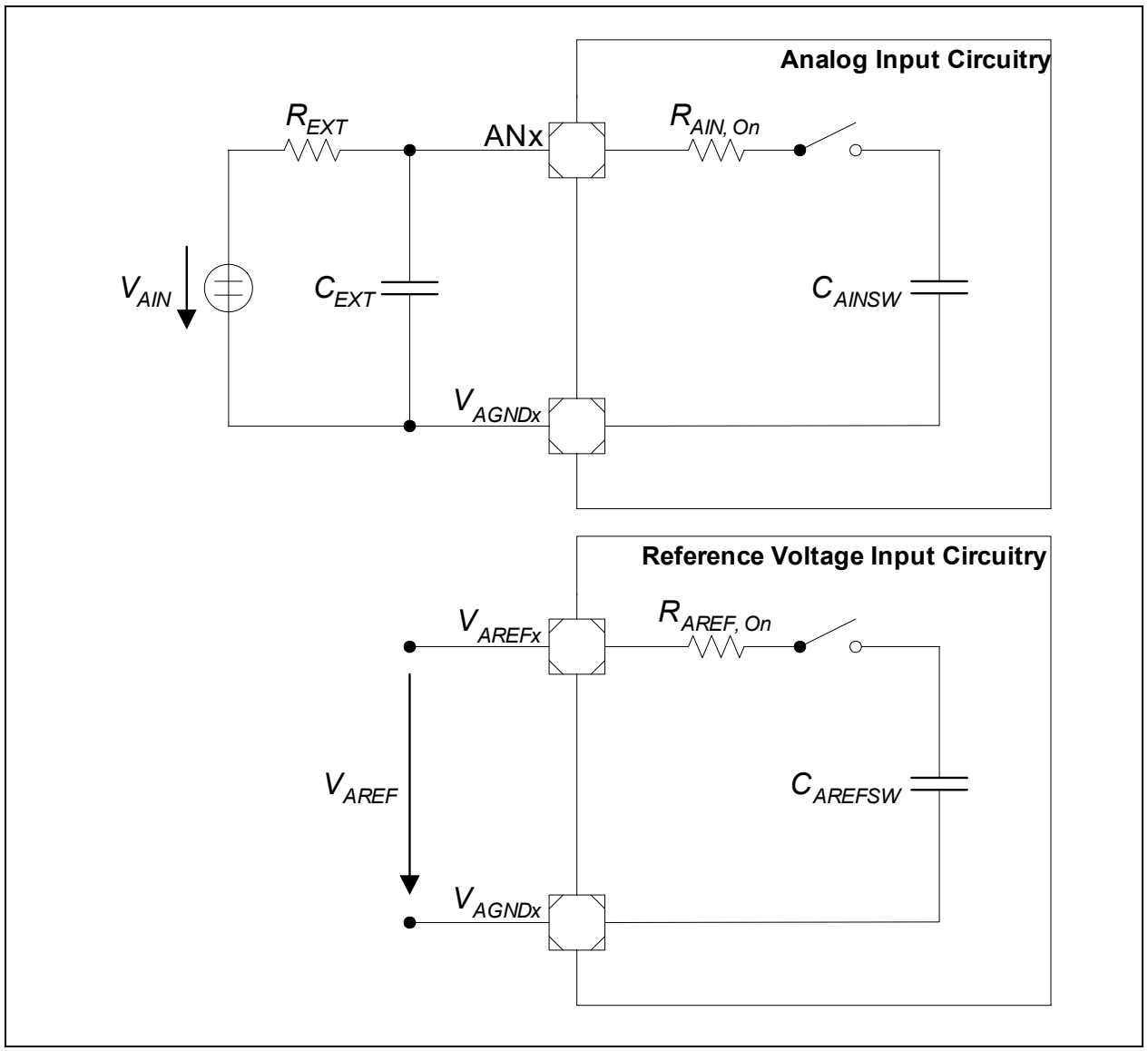


Figure 39 ADC Input Circuits

4.3.5 External Clock Drive XTAL1

Table 48 shows the parameters that define the external clock supply for XC886/888. These timing parameters are based on the direct XTAL1 drive of clock input signals. They are not applicable if an external crystal or ceramic resonator is considered.

Table 48 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Oscillator period	t_{osc}	SR	83.3	250	ns	1)2)
High time	t_1	SR	25	-	ns	2)3)
Low time	t_2	SR	25	-	ns	2)3)
Rise time	t_3	SR	-	20	ns	2)3)
Fall time	t_4	SR	-	20	ns	2)3)

1) The clock input signals with 45-55% duty cycle are used.

2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

3) The clock input signal must reach the defined levels V_{ILX} and V_{IHX}.

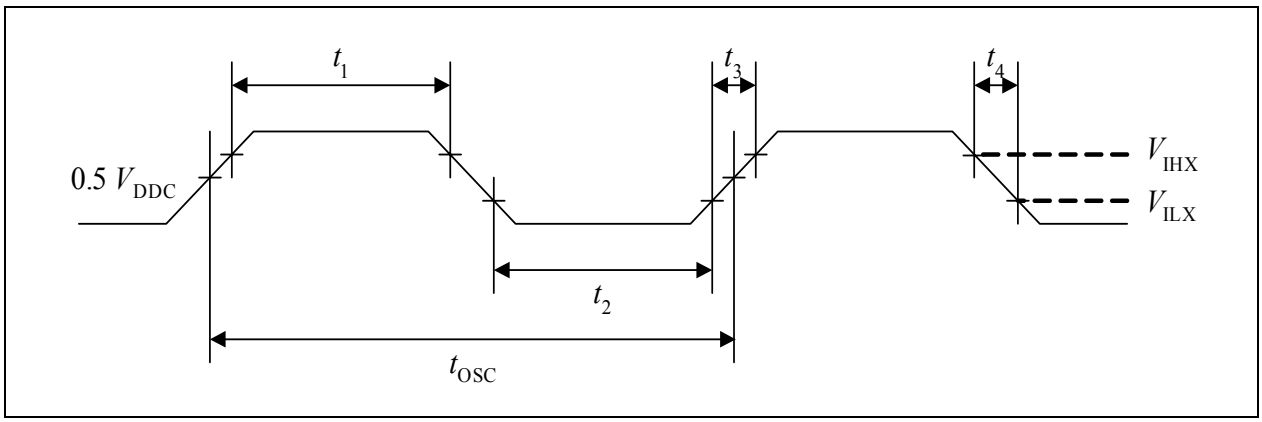
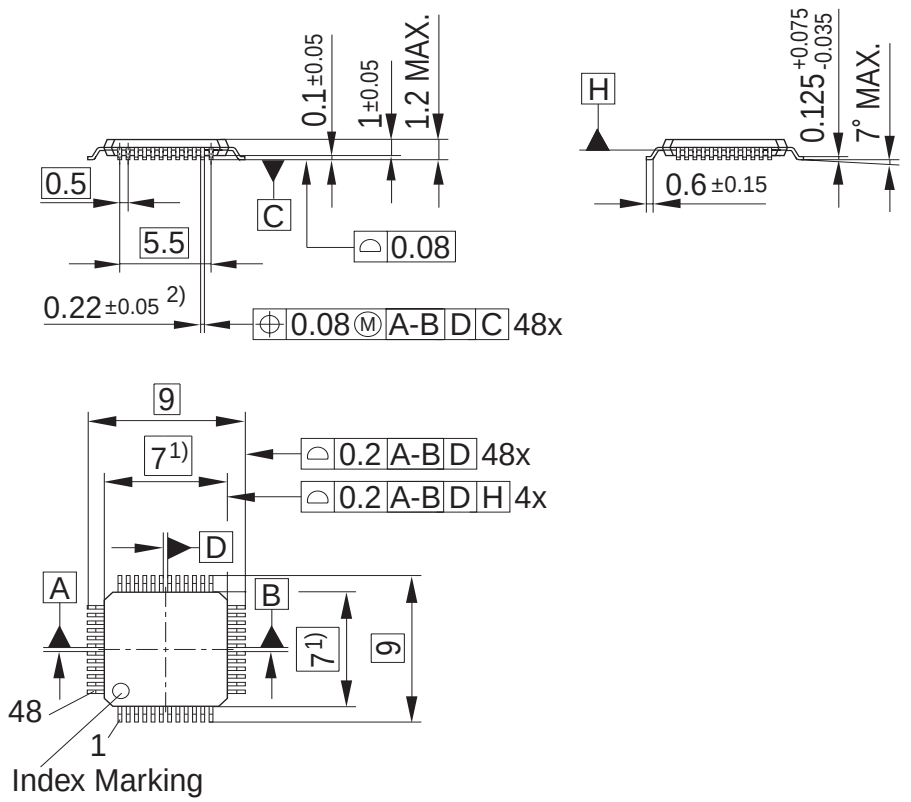


Figure 45 External Clock Drive XTAL1

5.2 Package Outline

Figure 48 shows the package outlines of the XC886.



1) Does not include plastic or metal protrusion of 0.25 max. per side
2) Does not include dambar protrusion of 0.08 max. per side

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Figure 48 PG-TQFP-48 Package Outline